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A DC Circuit Model of Distributed Diodes on Active Substrate Boards for CAD Tools

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Abstract—In the past few years, a new type of circuit board, named here as active substrate board (ASB), was introduced over circuit applications of diodes. Unlike a traditional printed circuit board (PCB), an ASB has its substrate made of a semiconductor. The inability of the traditional integrated circuit (IC) technology to integrate wavelength dependent radio frequency (RF) components triggered the advent of ASBs. These boards draw desirable features from IC as well as PCB technologies. Unprecedented challenges came up in modeling the different devices fabricated on an ASB owing to their large sizes and the presence of wideband microwaves. So far, modeling the effect of large sizes and ambient microwaves on DC bias of diodes have not been considered in scientific literature. Furthermore, the state of the art numerical simulators are unable to imitate the behavior of such diodes observed over measurements. Here, a semi-analytical, circuit model of distributed diodes on ASB is presented that is fairly accurate in predicting the actual behavior of the diodes. The model also opines a novel phenomenon where microwaves affect the DC characteristics of diodes with added resistances.

Index Terms—ASB, Diode circuit modeling, distributed diode, eddy currents, microwaves

I. INTRODUCTION

THE Integrated Circuit technologies are being used to make various RF circuits since long [1], however, some key radio frequency devices like distributed antennas and filters could not be yet integrated inside an IC chip owing to their sizes being dependent on the wavelength of electromagnetic waves that they process. Some technologies like system in package (SIP) [2] integrate wavelength dependent components on the packages instead of fabricating them on the chips; due to the complexity in modeling and fabrication, such devices are not very popular; as a result, the advantage of device scaling of ICs could not be fully utilized even in the present state of the art RF circuits. RF circuits mostly remain hybrid where RF ICs are discretely put together in PCBs that have printed antennas, filters, couplers etc [3]. From the perspective of RF circuit boards, an obvious bottleneck is the circuit miniaturization or scaling. Another problem arising at board levels is that of mismatches/losses encountered between

soldered components and transmission lines of the PCBs. The concept of ASB replaces the traditional dielectric substrate of a PCB with a semiconductor [4]. Conventional semiconductor substrates pose heavy losses to high frequency electromagnetic waves making them inefficient for microwave transmissions. In the past several years, high resistivity semiconductors have shown promise in microwave transmissions [5, 6]. Our ASBs use these high resistivity or semi-insulating substrates to avoid microwave losses. These semiconductor substrates are also high in relative permittivity that allows higher device scaling capabilities. Therefore, ASBs are good candidates for RF circuits that demand device scaling, low losses and low power operation.

The upcoming sections begin with the description of the distributed diode integrated in an ASB and its DC measurements. Thereafter, a semi-analytical DC model of the diode is developed for understanding the underlying physics behind the measured results and for its usage in different circuit designs or computer aided design (CAD) tools.

II. THE DISTRIBUTED DIODE

A. Topology of the Diode

Fig. 1 shows different views of a typical distributed diode to be used in shunt configuration for microwave applications [7].

Fig. 1. (a) The three dimensional and the (b) cross sectional view of a distributed diode integrated in an active substrate board (ASB)

On top of a high resistivity silicon (HR-Si), Boron doped P-Type substrate, phosphorus doped N^+ region is layered to form a N^+P junction. Without loss of generality, the type of doped regions may be interchanged to form a P^+N junction as well. Over the N^+ doped area and below the substrate, conductive layers of aluminum are formed as shown in the figure. In absence of a forward bias, microwaves may flow in or out of the ASB as shown in Fig. 1(a). A forward bias applied to the diode, shown in Fig. 1(b), attenuates the microwave flow. This kind of device is fabricated using the standard foundry of semiconductor process technology. The purpose of

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integrating devices like diodes and transistors on ASBs is to use the latter as microwave transmission lines and for the fabrication of passive devices at places where functional active devices are not required. Thus, this kind of an arrangement serves the dual purpose of an integrated circuit and a printed circuit board. ASBs are many times smaller than the usual PCBs attributed to the much higher dielectric permittivities of the former than the latter. Since large sized portions of ASBs function as diode and/or transistor devices, we named these devices as distributed devices due to their sizes being comparable to the wavelength of the microwaves to be processed through them. Additionally, usual semiconductor devices may be called lumped devices for their negligibly small dimensions compared to the wavelengths in consideration.

B. Structural, Material and Electrical Specifications of the Diode

Substrate/ Bulk:

i. Height: $h = 675\mu\text{m}$ ii. Material: Boron doped P type, High Resistivity Silicon iii. Resistivity: $\rho = 2.5 \times 10^3 \Omega\text{-cm}$ iv. P type Doping Concentration: $5 \times 10^{12} \text{cm}^{-3}$ v. Dielectric Constant: 11.7 vi. Microstrip Line Impedance: 50Ω vii. Microstrip Line width: $W_{\text{ms}} = 0.56\text{mm}$

Distributed Diode:

i. Doped area lengths L_n : $L_1 = 0.56\text{mm}$, $L_2 = 5\text{mm}$, $L_3 = 10\text{mm}$, $L_4 = 20\text{mm}$ ii. Phosphorus, N+ dopants: 10^{20}cm^{-3} iii. Depth: $1\mu\text{m}$ iv. Doped area width, W_n : $W = 0.56\text{mm}$ v. Voltage range: 0.0 volts to 3.0 volts v. $\mu_p = 500 \text{cm}^2/\text{V-s}$ vi. $\mu_n = 1500 \text{cm}^2/\text{V-s}$

C. The DC Measurements

The DC bias measurements of distributed diodes on ASBs were first reported in [8]. These boards have so far been used in microwave circuits only and are therefore subject to an inevitable presence of wideband electromagnetic waves (0.1-10 GHz) with 1mW power. In the present setup of measurements, the forward bias, voltage current (V-I) characteristics from four different boards are drawn at a temperature of 25°C .

Fig. 2 Top view of the boards. (a) $L_1 = 0.56 \text{ mm}$. (b) $L_2 = 5 \text{ mm}$. (c) $L_3 = 10 \text{ mm}$. (d) $L_4 = 20 \text{ mm}$.

These boards differ in the lengths, L_n (where $n = 1$ to 4), of the top doped layer while their widths, W_n : $W = 0.56\text{mm}$, remain same for all as shown in Fig. 2. Also, the microstrip and doped area widths correspond to characteristics impedance of the transmission line for best possible impedance matching during microwave operations. The DC measurements of voltage and current for all the boards are shown in Fig. 3. The DC sources use RF Chokes (not shown here) to prevent themselves from

RF contamination. These V-I characteristics show some distinct features which cannot be recreated using the available diode models. For examples, the shift in cut-in voltages, change in slopes of the V-I curves, overlap of some V-I curves etc. with respect to the changes in L_n s are yet to be understood. Therefore, a diode model must be developed that can explain the underlying physics behind the changes in the curves and also cater to designing of different diodes on ASBs.

D. The Limitations of Measurement

The measurements are made using Tektronix-Keithley 2400, a source and measurement unit (SMU). Due to the low power handling capability of the instrument, either the voltage or the current needs to be restricted for the measurements to remain under the allowable power ceiling. So, the maximum current ceiling is chosen as 250 mA. The same power ceiling restricts the measurements in reverse bias as well; i.e. the peak inversion voltage (PIV) cannot be reached.

Fig. 3 Measured V-I characteristics of diodes with different doped lengths.

III. DEVELOPMENT OF THE DC MODEL

Ever since the proposition of Shockley's ideal diode equation [9], decades of research outcomes in device modeling culminated in creation of a computer simulation program with integrated circuit emphasis (SPICE) [10], it took main stage in circuit simulations of various active devices. In context of P-N junction modeling, the ideal diode equation with the ideality factor η was almost sufficient except in the cases of current saturations due to high injection phenomenon at higher voltages. The prediction of this saturation current comes from the solution of generalized diode equation which are mostly approximate [11], an exact solution uses the mathematical Lambert W-function [12]. Unfortunately, none of these models could be generalized to characterize the DC behavior of our 3D distributed diodes with background eddy currents. Apparently, the V-I characteristics observed in Fig. 3 not only calls for a new formulation to fit multiple curves but also for the proposition of some new underlying physical phenomena. Thus, the task in hand is to model all the traits of the observed curves in form of equations that are based on physics. However, given the fact that even the simplest equation for diodes, the Shockley's equation (2), requires an empirical factor η with values determined heuristically, realization of a

model completely based on analytical physics is not a realistic goal, especially, when the complexity of the problem is far more than that of the simple diode. So, our model takes a semi-analytical approach where the developed equations are intuitively based on physics and many new empirical factors are proposed with their values fine tuned over several trials to fit the given curves.

The scope of our model is limited to DC response of distributed diodes on ASBs with or without ambient wideband microwave currents. It is also limited by the range of measurements taken. Therefore, this model may not be used as a generalized formulation for any other case. Moreover, unlike what is usual, high injection current saturation is not observed in our case despite large bulk resistances being present. As described ahead in one of the sections, we attribute this absence of high injection to the low range of voltage measurements, the large junction areas and the presence of microwave currents.

A. Reasoning the Shift in Cut-in voltages

As observed in the measurements, the cut-in voltages decrease with increase in doped lengths L_1 to L_4 . To understand this behavior, we may intuitively conceptualize the phenomenon of augmented capacitances with the increase in doped lengths, shown in Fig. 4.

Fig. 4 Increase in doped lengths modeled as parallel capacitors.

Longer lengths of L_n in a given diode shall contribute additional parallel capacitors or larger effective capacitances in the device. Increased capacitances shall affect the barrier potential and in turn decrease the cut-in voltages to lower levels as per (1) (i.e. a larger capacitance C decreases the cut-in voltage V_c) where dQ is a constant charge on the capacitor plates at a given instant. Additionally, the junction resistance decreases as L_n increases. This decrease in resistance also contributes to the decrease in cut-in voltage.

$$V_c = \frac{dQ}{C} \quad (1)$$

The change in cut-in voltages is accounted in the classical Shockley's equation, given in (2) and (3), in its junction area $A = L_n W_n$ where I_d and I_o are the forward diode current and reverse saturation current respectively. V is the voltage and rest of the symbols carry their usual meanings as described in [12,13]. The calculated V-I curves are plotted and compared with those of measurements in Fig. 5. In (2), the value of $\eta = 1.5$ is chosen to comply with the low injection phenomenon of diodes where recombination currents are formed in the junction as explained in [13]. Through different stages of

developing the model, various empirical parameters like η introduced in our model, undergo heuristic adjustments to match the calculated results with those of measurements.

Fig. 5 The lowering of cut-in voltages with increase in L_{dop} .

$$I_d = I_o \left(e^{\frac{qV}{\eta kT}} - 1 \right) \quad (2)$$

$$I_o = qA \left(\frac{D_N n_i^2}{L_N N_A} + \frac{D_P n_i^2}{L_P N_D} \right) \quad (3)$$

B. Matching the Change in Slopes

The slopes of the V-I curves from calculations differ a lot with those from measurements; i.e. in the former the slopes are almost same and the lines look parallel to each other unlike the latter case. The obvious reason of this difference may be the absence of bulk and contact resistances in our calculations. In usual practice, resistances are brought into account only using the generalized diode equation (GDE) that requires complicated calculations [11,12]. We want to avoid the solutions from GDE for the simple reason that high injection current saturation is not observed in our V-I characteristics. Therefore, a much simpler model, close to the ideal diode equation, may be sufficient for our purpose. To bring this simplicity, we propose a behavioral model shown in Fig. 6. Practically, bulk and contact resistances, R_{bs} and R_{cs} , appear in series with a diode resistance R_{ds} ; so, the usual practice is to model them in a series circuit. However, the model may be made simpler by easily transforming the series circuit into parallel such that their collective effective resistances remain same. The influence of the individual resistances may then be readily added as changes in the existing diode current shown in (4) and (5). In the parallel model, the diode, bulk and contact resistances are transformed as R_{dp} , R_{bp} and R_{cp} respectively. V , I , I_{dp} , I_{bp} and I_{cp} are the source voltage, source current, diode current, bulk current and contact current respectively in parallel. The arrow over R_{bp} shows the variability with bias, similar to the junction resistance.

$$I = I_{dp} + I_{bp} + I_{cp} \quad (4)$$

Fig. 6 The bulk and contact resistances in parallel

$$I = I_{dp} + \frac{V}{R_{bp}} + \frac{V}{R_{cp}} \quad (5)$$

Thus, this improvisation avoids the solution that requires separating the variables in the GDE. Obviously, the values of equivalent parallel resistances cannot be equal to their series counterparts. We relate the three categories of these resistances with scaling factors: S_d , S_b and S_c , as given in (6). An analysis, based on energy balance, is presented in Section VII whereby the values of the scaling factors may be determined qualitatively. R_{bs} is related to the bulk resistivity ρ with $R_{bs} = \rho h/A$ as usual where h is the substrate height and A is the junction area. It is important to note that the cross sectional area of the diode, through which the current travels, is non uniform and changes from the region of junction to that of bulk. Nevertheless, in the absence of a lateral potential difference, only a negligible increase in the effective cross sectional area, due to diffusion current and fringe fields, is assumed. Therefore, as evident from the subsequent results, the effective cross sectional area is practically equal to the junction area A in our case.

$$R_{dp} = \frac{R_{ds}}{S_d}; R_{bp} = \frac{R_{bs}}{S_b}; R_{cp} = \frac{R_{cs}}{S_c} \quad (6)$$

The final values of scaling factors are heuristically adjusted to: $S_d = 0.3003$, $S_b = 25$ and $S_c = 0.0004$ for the present case, assuming $R_{cs} = 1 \Omega$. Fig. 7 shows the calculated V-I curves after addition of bulk and contact resistances.

Fig. 7 The V-I curves after the inclusion of bulk resistance.

Since (2) is a current equation, R_d or R_{ds} should effectively appear at the denominator of V in (2). Therefore, S_d simply becomes a multiplicative factor with V in the numerator of the exponentiation thereby obtaining I_{dp} from I_d or I_{ds} . Though,

with addition of resistances, the slopes are tapered as expected, the shapes of the curves are starkly different from those of measurements. Due to the influence of the large bulk resistances, the calculated curves have much lower slopes and are mostly linear from 0 to 2V as compared to their measured counterparts.

C. Adjusting the Shape of Curves

To properly shape the calculated curves, we should primarily target to bring in non-linearity in their largely linear characteristics. The linearity may be attributed not only to the large bulk resistances but also to their constant values for a fixed geometry. In other words, the bulk resistivity is not only large but also static. Though, the static bulk resistivity is not much of an issue in diodes with small bulk regions, with large ones it is a significant concern. Particularly, we may construe that the static bulk in our calculations have resulted in the aforesaid lower slopes. We may argue, that since the junction resistivities in the forward biased diodes are dynamic, as evident from the Shockley's equation, then those of bulk should also be dynamic; after all, the junctions and bulks are made of same semiconducting materials. Therefore, unlike static resistivities of conducting materials, semiconducting materials should exhibit dynamic resistivities in general. This hypothesis of a dynamic bulk resistivity is rarely supported in the academic literatures because it is rarely needed. One research implicitly [14] supports this hypothesis by reporting a phenomenon named conductivity modulation. In conductivity modulation, the resistivity or conductivity of the bulk is said to get changed or modulated as a function of the diode current. Since our model uses a parallel bulk resistance, its resistivity, shown in (7), is modulated, or made dynamic, as a function of the diode voltage V where $V_N = V/V_o$ is the diode voltage normalized over $V_o = 1$ V. Formulation of this function may get influenced by several factors like doping concentrations, geometry, temperature and so on. Fig. 8 plots the calculated

Fig. 8 V-I curves considering dynamic bulk resistivity.

V-I curves considering dynamic bulk resistivity and compares them with the measured ones. The subscripts 'dn' and 'st' represent dynamic and static resistivities respectively. It goes without saying that ρ_{st} is the usual bulk resistivity ρ . The order m , of the normalized voltage V_N , may take non integer values as well. Addition of unity to the functions of V_N in (7) ensures

ρ_{dn} to remain equal to ρ_{st} and not infinite at zero bias voltage.

$$\rho_{dn} = \frac{\rho_{st}}{(I + V_N)^{m/(1+\sigma V_N)}} \quad (7)$$

The final estimated value of $m = 4.22$. Considering the fact that diode current cannot increase infinitely, a damping factor named σ is introduced to saturate the current by increasing the dynamic resistance at higher voltages. This factor is heuristically found to be $\sigma = 0.008$ in our case. The shapes of the calculated curves now match with those of measurements. However, the disparity between their locations is still unresolved. This is the most crucial and also the final aspect of our problem to be solved.

D. Collocating the Curves

Collocating the calculated and measured curves is not as simple as it normally seems. A meticulous look into Fig. 8 reveals that a constant shift in the calculated curves shall not be sufficient for the collocation, because, the separation between the curves in measurements are not linear; i.e. the separation between the curves of L_1 and L_2 is proportionally far larger than that between the curves of L_2 and L_3 ; surprisingly, curves of L_3 and L_4 have almost no separation, they overlap each other. Clearly, we need some new understanding to fulfill our task ahead. For this, we take a relook in to dynamics of the large diodes. Geometry of our diodes are such that the currents shall traverse more distance through top and bottom surfaces than through the height h of the substrates. We name these currents as surface traversed currents (STCs) as shown in Fig.9 (a). Additionally, the most different aspect in our diodes is the presence of background microwaves. When the diodes are on, these microwaves generate induced currents in the substrates called eddy currents. Usually microwaves can't generate non induced conducting currents. A very distinct feature of the induced currents are their opposition to their cause. Since, the current through the diodes attenuate the prevailing microwaves, we may be very sure that these currents are nothing else than eddy currents. The eddy currents become more dominant in our case because of the availability of large bulks. At this point, we ideate that the STCs and eddy currents are responsible for the variable gaps between the subsequent curves. Particularly, it would be interesting to see whether this aspect can explain the overlap of curves for the doped lengths of L_3 and L_4 . Most of the eddy current roles in device physics, reported and modeled so far, are for on-chip inductors [15-17]. To find a place for these new currents in our calculations, we propose the concept of effective length of traversal. The effective length of traversal l_e in a conductor/semiconductor may be an important factor that changes the resistance. In usual cases, the length of a conductor/semiconductor, l , is far more than the perimeter P_A of the cross sectional area ($l \gg P_A$); however, in our special case of distributed diodes, the cross sectional perimeters are far more than the lengths ($P_A \gg l$). Due to this structural difference that causes STCs and the presence of eddy currents, the diode current should traverse longer

lengths through the surfaces and volumes than through the physical lengths of the devices. Our substrates do not have structural variability in the physical length h , therefore, l_e has been made a function of fixed length h and a variable length dependent on the junction area A rather than the volume. l_e is formulated in (8). The path of the diode current under the influence of eddy currents is illustrated in Fig. 9(b)-(c). This is a rather simplistic depiction of eddy currents because the current loops may have non circular shapes and may be oriented non horizontally depending on the mode of the microwaves present in the substrate. Though, the eddy currents traverse through different areas of junction and the bulk, the effective length is only formulated with respect to the junction area using different empirically adjusted factors for convenience.

Fig. 9 (a) The STCs. (b) Under the influence of eddy currents, the helical path taken by the total current through the diode.

From what can be seen in the illustration, the total current I through the diode is imagined to be superimposed on the eddy currents in a way that it starts traversing a non-uniform helical path through the substrate. The non-uniformity is due to the asymmetry in the structure of the diode. In reality, there may be several such helical paths with different loop areas and shapes, depending on the range of frequencies and the area available to establish the eddy currents. Therefore, considering the complexity in structural, spectral and power variability of our model, the relationship between the effective length of traversal l_e and the junction area A may take the form of a general empirical relation of (8) where $A_N = A/A_0$ is the junction area normalized over an unit area of A_0 and α_o or k_o are empirical factors determined heuristically and o takes numbers from 1 to O . Except α_o , which has a dimension of length, all other empirical factors used in the model are dimensionless. In addition to the variables considered here, a variable microwave power is expected to influence α_o and changes in frequency components are expected to influence both α_o and k_o .

$$l_e = h + \alpha_1 A_N^{k_1} + \alpha_2 A_N^{k_2} + \dots \alpha_o A_N^{k_o} + \dots \alpha_O A_N^{k_O} \quad (8)$$

The order O of (8) is a positive integral value determined by

the complexity of the problem in hand. For the present case, $O=3$ was sufficient. Subsequently, the other parameters take the following values to give the final fit to the curves: $\alpha_1 = 0.95$, $k_1 = 0.55$, $\alpha_2 = 0.30$, $k_2 = 1.35$, $\alpha_3 = 18$, $k_3 = 1.95$. Fig. 10 plots the final calculated results and compares them with the measured ones. Now that our assumptions have shown concrete results, we may try giving a simplistic reason for the overlap at L₃ and L₄. As the new formula for the series bulk resistance is now $R_{bs} = \rho_{dn} l_e / A$, in case of L₃ and L₄, the surface areas in the expression of l_e become so dominant that the effect of substrate height h may be neglected; as a result, if the values of l_e and A come

Fig. 10 The final, calculated V-I curves compared with the measured results

close to each other, the dependence of the bulk resistance on physical dimensions minimizes resulting in the observed overlaps. Similarly, the non-linearity in the gaps between the subsequent curves may also be explained.

E. The Case of Pure DC

The ASBs are supposed to be used for microwave application, so, the devices made on those shall be inevitably subjected to microwaves that influence the DC VI characteristics. As discussed before, the effective length l_e shall always be dependent on eddy currents in all practical cases. Owing to its theoretical importance, changes in the l_e may be calculated in absence of eddy currents to see the effect of STC alone. For this purpose, as shown in Fig.11, we measure the DC VI characteristics of the boards again without supplying microwaves. The measurements that include microwaves were

Fig. 11 Calculated V-I curves compared to pure DC measurements

taken more than two years back as reported in [7]. In the second episode of pure DC measurements, unfortunately, the ASB pertaining to L₁ was found damaged. Therefore, for pure DC measurements, only three boards, i.e. L₂, L₃ and L₄, are available to validate our model and show the difference in the values of l_e in pure DC and DC with microwaves. The pure DC measurements indirectly endorse the robustness of our model because the values of all the empirical factors in pure DC and impure DC models remain same except for the obvious case of effective length. The effective length evaluated from the matched results for pure DC is $l_e = h + 2.35A_N^{1.35}$, this clearly indicates that the parametric pairs of α_1, k_1 and α_3, k_3 are affected by the eddy currents whereas α_2, k_2 is affected by surface currents. Therefore, in pure DC case, only the α_2, k_2 pair exists. However, in the case of microwaves, α_2 is much smaller than that of pure DC case attributed to the fact that microwave currents are more engaged in the eddy current paths than those of surface currents. It is evident from the calculations that the effective length increases and the DC current decreases as the microwaves start flowing in the substrate. This can also be observed in the measured results shown Fig. 10 and Fig.11. Consequently, microwaves contribute to an excess resistance.

IV. NUMERICAL SIMULATIONS

A. Limitations of the Simulation

Numerical simulations using a general purpose device physics simulator like ATLAS-Silvaco that incorporates various computational electronics models [18] have become the best possible way of predicting electronic device behaviors in contemporary research. Though these simulators are capable of predicting various complex behaviors down to quantum levels, they are not quite designed to handle large device sizes. This is ascribed to one of the primary focuses of electronic technology being device miniaturization. For our device modeling, this is a huge disadvantage; any attempt to make a 3D simulation of our requirement, ATLAS simulator runs out of its simulation handling size. The best 2D simulation that could be performed was on the common cross-section of our diodes shown in Fig. 1(b). Another problem is the inability of the simulator to co-simulate DC behavior of the diodes in presence of eddy currents.

B. Analyzing the Results

Fig. 12 plots the V-I characteristic obtained from the ATLAS simulation of the 2D cross sectional structure of our diodes. The reason for simulating the common cross sectional layout is to get a fair estimate of the universal behavior that may be exhibited by all the diodes in our present consideration. It will be superfluous to compare this simulation with the measurements because it neither matches them in terms of 3D structure nor in terms of the background eddy currents. However, it will be worth noticing that unlike the measured results, the result from simulation shows the classical phenomenon of high injection current saturation at higher voltages with in the low voltage range of observations.

Considering the present constraints of our simulation tools, the most appropriate theories that we can propose to support this difference are, firstly, in pure DC case, unlike simulation, the measurements have large junction areas that require much higher voltage ranges to exhibit high injection saturation. Secondly, in DC with microwaves, the high density of carriers created from high injection at any given location are rarified due to the circulating eddy currents; as a result, current saturation may be avoided for even a much larger range of voltages.

Fig. 12 2D Atlas simulation of the cross sectional layout.

V. APPLICATIONS OF THE DEVICES

The diodes modeled here have various potential applications [4], apart from the switches [8] and tunable resonators [19-21] which have already been designed, fabricated and reported, several other circuit applications like variable attenuators, tunable antennas are also proposed [4].

VI. A NUMERICAL EXAMPLE

Example: A distributed diode is designed with a doped area of 0.56 mm^2 on an ASB with doping and temperature conditions specified as above. Assuming that a current of 120 mA is required to attenuate the incoming microwaves by 20 dB if the diode is used as a switch, what should be the voltage applied to the diode terminals to cause the desired attenuation?

Solution: Fig. 12 is plotted using the formulations given

Fig. 13 V-I characteristics of the numerical example.

above and taking dimensional unit in centimeters. Equation (9) for R_{bp} is used for calculations. Substituting the values of

R_{bp} , R_{cp} and I_{dp} in (5), the V-I characteristics may be plotted as shown in Fig. 13. From Fig. 13, it may be determined that the required voltage to draw the current of 120 mA is $V = 2.17 \text{ V}$ so that an attenuation of -20 dB is caused in the switch off condition

$$R_{bp} = \frac{2500[0.0675 + 0.95(0.0056)^{0.55} + 0.30(0.0056)^{1.35} + 18(0.0056)^{1.95}]}{25(0.0056)V_N^{4.22}} \quad (9)$$

VII. THE PARALLEL CIRCUIT MODEL

The transformation of the series circuit to the parallel circuit in our model needs a careful attention. Due to the use of variable resistances similar to some of the considerations in [22], usual linear network transformations don't apply in our case. The model is purely a behavioral model, i.e. equivalent circuit model. The basis of our model is on the universal physics of potential energy (i.e. Kirchhoff's voltage law, KVL) to kinetic energy (i.e. KCL) transformation or, in other words, a transformation from (10) to (11). To replicate the behavior of variable resistances without compromising the physics, a balance between (10) and (11) is maintained in a way that each V_u of (10) is directly proportional to its I_u of (11) as given by (12). Fig. 14 shows the circuit transformation. For the circuit equivalence to hold, V_T and I_T are constrained to be same for both the circuits. If we assume that $R_{pu} = R_{su}/S_u$, then it is evident that an increase or decrease in the potential drop across a resistor of the series circuit creates an increase or decrease in the corresponding value of the scaling factor S_u in its parallel equivalence so that the energy balance is maintained.

Fig.14 The (a) series to (b) parallel circuit transformation.

$$V_T = V_1 + V_2 + \dots V_u + \dots V_U \quad (10)$$

$$I_T = I_1 + I_2 + \dots I_u + \dots I_U \quad (11)$$

$$V_u \propto I_u = \frac{V_T}{R_{pu}} = \frac{V_T S_u}{R_{su}} \quad (12)$$

Therefore, since the bulk has the highest potential drop, it has the largest value of S_u and the junction has a very small S_u because of its substantially small potential drop. For the same reason, the S_u of contact resistance is negligibly small. Unlike in the cases of junction and contact resistances, the bulk has a high dynamic range of resistance, i.e. it starts from a very high resistance at lower bias voltages and becomes a very low resistance at higher bias voltages; this large dynamic range also causes the S_u of the bulk to be large. The contact resistance of the diode has been separately modeled and not

included in the bulk because, unlike the bulk resistance, it is not variable in nature. Conclusively, the overall behavior of the diode is dominated by the bulk rather than the junction. To appreciate the difference between models of non-linear and linear devices, let us now take the example of a purely linear model of two resistors of resistance R each connected in Series. A parallel equivalent of this may easily be obtained by using two resistances of $4R$ each. Therefore, $S_u=0.25$ for each of these resistances. It may be further shown that S_u in a purely passive circuit (i.e. with no variable resistances) shall always be less than unity, whereas, in an active circuit of variable resistances S_u may become more than unity just as in the case of our bulk where $S_u=25$. Despite the variable resistance of the active junction, S_u for it remains below unity attributed to its low dynamic range of resistance and a very less potential drop. Moreover, if a variable resistance increases in a circuit, it may impose a S_u of more than unity to its neighboring resistances.

VIII. CONCLUSION

The most important aspect to conclude is the fact that the model proposed here indicates towards a novel phenomenon of an AC (i.e. microwave) affecting a DC with an added resistance. As evident, this happens due to the additional contribution of effective length from the eddy currents. The phenomenon of excess resistance is not new. For example, increase in resistance of conductors due to increase in temperature is well known. A recent research [23] points out towards an excess resistance due to electron-electron scattering in graphene. However, presence of an excess resistance due to alternating currents has never been shown before. We may conclude that the physics proposed to predict the behavior of the devices have been satisfactory, given the fact that a reasonable agreement with the measured results could be obtained without using any curve fitting tool. Despite accurate curve fitting being not the primary objective of the current research, the proposed physics had been good enough to obtain a multiple curve fitting solution using a single formulation that is difficult to obtain using the usual techniques. More accurate curve fitting may be accomplished using modern optimization algorithms [24] on a fitness function based on (8). The empirical factors of the model may be influenced by measurement errors, for example, in the case of DC with microwaves, the instrument cluster for supplying microwave may enforce additional load, though such chances are rare. Beyond the present scope of this paper, GDE may be used in conjunction with some of the aspects considered here to formulate a generalized model in future. Also, the effect of microwave single tone or narrow band power may be studied further with wave modal analysis in future.

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REFERENCES

- [1] L. E. Larson, "Integrated circuit technology options for RFICs-present status and future directions," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 3, pp. 387-399, March 1998.
- [2] S. Wi et al., "Package-Level Integrated LTCC Antenna for RF Package Application," *IEEE Transactions on Advanced Packaging*, vol. 30, no. 1, pp. 132-141, Feb. 2007.
- [3] M. A. Khater, "High-Speed Printed Circuit Boards: A Tutorial," *IEEE Circuits and Systems Magazine*, vol. 20, no. 3, pp. 34-45, 2020.
- [4] C. Quendo, R. Allanic, D. Le Berre and Y. Quéré, "Novel approaches to design tunable devices," 2017 IEEE 18th Wireless and Microwave Technology Conference (WAMICON), Cocoa Beach, FL, 2017.
- [5] Y. H. Wu et al., "Fabrication of very high resistivity Si with low loss and cross talk," *IEEE Electron Device Letters*, vol. 21, no. 9, pp. 442-444, Sept. 2000.
- [6] M. Spirito et al., "Surface-passivated high-resistivity silicon as a true microwave substrate," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 7, pp. 2340-2347, July 2005.
- [7] R. Allanic, Y. Quéré, D. Le Berre and C. Quendo, "A novel approach to co-design microwave devices with distributed switches," 2016 Asia-Pacific Microwave Conference (APMC), New Delhi, 2016.
- [8] R. Allanic et al., "Impact of the doped areas sizes in the performances of microwave SPST switches integrated in a silicon substrate," 2018 IEEE 22nd Workshop on Signal and Power Integrity (SPI), Brest, 2018.
- [9] W. Shockley, "The theory of p-n junctions in semiconductors and p-n junction transistors," *The Bell System Technical Journal*, vol. 28, no. 3, pp. 435-489, July 1949.
- [10] L. W. Nagel and D. O. Pederson, "Simulation Program with Integrated Circuit Emphasis (SPICE)," *University of California, Berkeley Technical Report No. UCB/ERL M382, April 1973*.
- [11] T. A. Fjeldly, B. - Moon and M. Shur, "Approximate analytical solution of generalized diode equation," *IEEE Transactions on Electron Devices*, vol. 38, no. 8, pp. 1976-1977, Aug. 1991.
- [12] T. C. Banwell and A. Jayakumar, "Exact analytical solution for current flow through diode with series resistance," in *Electronics Letters*, vol. 36, no. 4, pp. 291-292, 17 Feb. 2000.
- [13] K. Kano, *Semiconductor Devices*, Prentice Hall, New Jersey, 1998.
- [14] A. Barna and D. Horelick, "A simple diode model including conductivity modulation," *IEEE Transactions on Circuit Theory*, vol. 18, no. 2, pp. 233-240, March 1971.
- [15] Ban-Leong Ooi, Dao-Xian Xu, Pang-Shyan Kooi and Fu-jiang Lin, "An improved prediction of series resistance in spiral inductor modeling with eddy-current effect," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 9, pp. 2202-2206, Sept. 2002.
- [16] Kyuchul Chong, Ya-Hong Xie, Kyung-Wan Yu, Daquan Huang and M. -F. Chang, "High-performance inductors integrated on porous silicon," *IEEE Electron Device Letters*, vol. 26, no. 2, pp. 93-95, Feb. 2005.
- [17] A. Nieuwoudt, M. S. McCorquodale, R. T. Borno and Y. Massoud, "Accurate Analytical Spiral Inductor Modeling Techniques for Efficient Design Space Exploration," *IEEE Electron Device Letters*, vol. 27, no. 12, pp. 998-1001, Dec. 2006.
- [18] D. Vasileksa and S.M. Goodnick, *Computational Electronics, Synthesis Lectures On Computational Electromagnetics-6*, Morgan & Claypool Publishers, 2006.
- [19] R. Allanic, Y. Quéré, D. Le Berre and C. Quendo, "Intrinsically microwave tunable resonator designed on silicon," *Electronics Letters*, vol. 52, no. 20, pp. 1697-1699, Sep. 2016.
- [20] R. Allanic et al., "Three-State Microwave Tunable Resonator Integrating Several Active Elements on Silicon Technology in a Global Design," *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 2, pp. 141-143, Feb. 2018.
- [21] R. Allanic et al., "Continuously Tunable Resonator Using a Novel Triangular Doped Area on a Silicon Substrate," *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 12, pp. 1095-1097, Dec. 2018.

- [22] L.O Chua, "Device Modeling Via Basic Nonlinear Circuit Elements," *IEEE Transactions on Circuits and Systems*, vol. cas-27, no. 11, pp. 1014-1044, Nov. 1980
- [23] J.R Wallbank et al., "Excess Resistivity in Graphene Superlattices Caused by Umklapp Electron-Electron Scattering," *Nature Physics*, vol. 15, pp. 32-36, 2019
- [24] P. Chakravorty and D. Mandal, "Role of Boundary Dynamics in Improving Efficiency of Particle Swarm Optimization on Antenna Problems," 2015 IEEE Symposium Series on Computational Intelligence, Cape Town, 2015, pp. 1157-1163

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