A Fast Finite Sample Count Symmetric Component Extraction Method for Use in Grid Side Converters

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Abstract—The considerable increase in the number of renewable energy sources in power systems in recent years has led to the grid side converters' connection requirements being more and more strict. In order to comply with the newly arising grid codes, the synchronization unit has to provide a fast and robust response even under unbalanced and distorted line voltage. This paper proposes a new method for very fast extraction of symmetrical components. The method uses a finite number of grid voltage samples to solve a set of algebraic equations and obtain sine and cosine factors of the direct and inverse sequence components. The corresponding amplitudes and angles are then found by using $\sqrt{}$ and $\arctan$ functions. The proposed extraction algorithm requires a derivative estimation technique to estimate the frequency from the direct sequence angle. The performance of the proposed finite sample count (FSC) method is compared to the all-pass filter (APF) based synchronous reference frame phase-locked-loop (SRF PLL) in simulations and experimentally using a DSP based platform and grid emulator with analog outputs. Under the voltage dip, FSC responds within several hundreds of μs , whereas it takes around $3ms$ for the APF SRF PLL to settle.

Index Terms—All-pass filter (APF), grid-connected converters, phase locked loop (PLL), synchronization, sequence detection.

I. INTRODUCTION

THE modern power system contains a considerable amount of renewable energy sources (RES) which are connected to the grid via grid-side converters (GSC) [1]. When operating in a grid connected mode, GSC are usually current controlled [2]. During normal grid conditions they are intended to inject the maximum harvestable power in the form of sinusoidal currents [3], [4]. Therefore, they need a fast and accurate detection of the grid voltage phase angle [2], [5]. There are several important aspects of RES regarding the functioning of the system as a whole [6], [7]. Firstly, their

integration into the system usually results in a distributed generation. Secondly, since they are connected to the grid via GSC, their dynamic behaviour is by default completely different from that of conventional synchronous generators, but can be appropriately enhanced by the control applied. On the other hand, the load is also becoming more and more electronically controlled. As a consequence, strict grid connection requirements are arising for RES in order to ensure stability and availability of the grid [8]. Control of GSCs is crucial for complying with these grid codes [1]. For example, GSCs are expected to have various modes of operation, low-voltage ride through capability, specific control strategy during grid faults, capability to operate in the presence of imbalance, harmonics and DC bias, etc [1], [3], [9]. In order to enable these functionalities, in addition to line voltage phase angle, information about frequency and voltage amplitude is needed [10]. Detection of the aforementioned grid variables has to be precise, fast and robust, so that it is reliable even during abnormal grid conditions [11]. In the presence of imbalance, it is most important to have the previously discussed information about the direct sequence component [10]. However, it might be useful, or even required, to have information about the inverse sequence component as well, in order to implement the appropriate control algorithm during faults [12]–[14].

The Synchronous Reference Frame (SRF) Phase-Locked Loop (PLL) is a state-of-the-art synchronization solution for grid tied converters [3], [10], [15]. Nevertheless it suffers from poor performance under imbalanced grid conditions due to the second order harmonic oscillations in the extracted quantities, which are present as a consequence of the inverse sequence in the grid voltages [3]. Moreover, it is sensitive to harmonics and leads to unsatisfactory performance in situations where the grid is significantly distorted [15]. Different techniques have been presented to address these issues [5], [10], [12], [16]–[18]. Most of them imply the addition of some filtering method, either as an in-loop filter or as a pre-filter [14], [18]. The performance of different approaches is usually evaluated based on two criteria: disturbance rejection capability and dynamic properties [18]. Direct sequence phase, frequency and amplitude errors are of interest when the grid voltages are exposed to imbalance, DC offset, harmonics and frequency variations [15], [17]. In addition to this, the dynamic performance evaluation in terms of overshoot and settling time under phase and frequency jumps, as well as voltage dips is also criteria for comparison [17], [19]. For most of enhanced SRF

Manuscript received Month xx, 2xxx; revised Month xx, xxxx; accepted Month x, xxxx. This work was supported in part by the Ministry of Education, Science and Technological development of the Republic of Serbia under Grant TR33020. (Corresponding author: Ruzica Cvetanovic.)

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PLL methods, the disturbance rejection capability and dynamic performance are opposing goals and parameter setting come as a compromise between those two requirements [18]. The latter, i.e. fast extraction of symmetrical components, is of high importance in order for the GSC to adequately cope with the grid imbalance and comply with the ever increasing grid connection requirements [19]. The most frequently encountered disturbance for the synchronization loop is the voltage dip [19]. To the best of the author's knowledge, only a few methods have been reported in literature which result in the settling time of not more than $5ms$ when exposed to a voltage dip. Among them are delayed signal cancellation ($5ms$) [20], [21], non-nominal dq-transformation based extraction ($2ms$) [12], direct sequence detection using all-pass filters ($3ms$) [22].

This paper aims at providing a novel approach for fast extraction of symmetrical components which is based on finite number of grid voltage samples. With an assumption that grid voltage contains only direct and inverse sequence components and that frequency estimate is available, it turns out that only two samples are sufficient to obtain exact values of the direct and inverse sequence amplitudes and angles. This is accomplished via solving set of algebraic equations in $\alpha\beta$ frame to obtain cosine and sine factors of each sequence components. These are further used to determine amplitudes and angles simply by using $\sqrt{}$ and $\arctan$ functions. Since grid frequency in practice is a slow-varying variable, an adequate low-bandwidth method for its estimation from the direct sequence angle can be implemented. Settling time of the proposed Finite Sample Count (FSC) extraction algorithm is theoretically zero, but of course in practise exhibits a non-zero value defined by the execution time and time delay of anti-aliasing filters used for voltage sampling. Small settling time is the biggest advantage of the proposed finite sample count extraction approach. In addition to the introduction of new algorithm for fast extraction of symmetrical components, an overview of the all-pass filter (APF) based SRF PLL extraction is provided. The goal is to compare dynamic performance of two approaches in simulations and experimentally.

This paper is organized as follows. For the purposes of benchmarking, Section I outlines fast symmetric component extraction which is based on of the all-pass filtering approach and SRF PLL. Section II introduces concept and provides detailed explanation of the new finite sample based sequence extraction algorithm. Dynamic performances of the proposed and benchmark extraction methods are compared in MATLAB simulation in section III. Experimental validation using Typhoon HIL402 with three phase analog outputs and F28379D DSP based platform is provided in Section V. The last section concludes paper along with a proposal for the future work.

II. SRF PLL WITH APFs AS IN-LOOP FILTERS

The conventional SRF PLL relies on the dq transformation [3]. The angle used for this transformation is derived as the output of the PI controller which regulates the d axis voltage component to zero, thereby ensuring that in the steady state the grid voltage vector is aligned with the q axis [6]. However,

Fig. 1: Block diagram of SRF PLL with APFs as in-loop filters.

under unbalanced grid conditions, this approach results in an unacceptable ripple in both d and q axis voltage components [10]. The amplitude of this ripple depends on the parameter setting of the PI controller [10]. In order to minimize the effect of the undesired ripple, a common approach is to add either in-loop or pre-loop filters [18]. For most of them, the inverse sequence influence suppression capability is inversely proportional to the introduced delay [14], [18]. Thus, the parameter setting procedure comes as a compromise between the two contradictory requirements: disturbance rejection capability and dynamic performance [18]. In this section a method which assumes APF based in-loop filtering is introduced (Fig. 1), with the goal of providing benchmark extraction method for the comparison with the newly proposed FSC method (Fig. 2). Prior to explaining APF based approach, an overview of the SRF PLL operation under unbalanced grid conditions is provided.

A. SRF PLL in presence of grid imbalance

In the presence of imbalance, grid voltages can be expressed as the sum of the direct and inverse sequence components with amplitudes U^{+1} and U^{-1} and phases $\theta^{+1} = \omega t + \theta_0^{+1}$ and $\theta^{-1} = \omega t + \theta_0^{-1}$ respectively:

$$\begin{aligned} U_a(t) &= U^{+1} \cos(\theta^{+1}) + U^{-1} \cos(\theta^{-1}) \\ U_b(t) &= U^{+1} \cos(\theta^{+1} - \frac{2\pi}{3}) + U^{-1} \cos(\theta^{-1} + \frac{2\pi}{3}) \\ U_c(t) &= U^{+1} \cos(\theta^{+1} + \frac{2\pi}{3}) + U^{-1} \cos(\theta^{-1} - \frac{2\pi}{3}). \end{aligned} \quad (1)$$

where $\omega = 2\pi ft$ is the angular frequency of the grid. The Clarke transformation results in the following expressions for the voltages in the stationary $\alpha\beta$ frame:

$$\begin{aligned} U_\alpha(t) &= U^{+1} \cos(\theta^{+1}) + U^{-1} \cos(\theta^{-1}) \\ U_\beta(t) &= U^{+1} \cos(\theta^{+1} - \frac{\pi}{2}) + U^{-1} \cos(\theta^{-1} + \frac{\pi}{2}). \end{aligned} \quad (2)$$

The synchronous rotating frame transformation leads to:

$$\begin{aligned} U_d(t) &= U^{+1} \cos(\theta^{+1} - \theta_e) + U^{-1} \cos(\theta^{-1} + \theta_e) \\ U_q(t) &= U^{+1} \sin(\theta^{+1} - \theta_e) - U^{-1} \sin(\theta^{-1} + \theta_e) \end{aligned} \quad (3)$$

where θ_e is the d axis position used for Park transformation. Position of q axis is set to PLL output θ_{pll} . In the steady state PI regulator ensures that $\theta_{pll} = \theta^{+1}$. Assuming that temporarily the grid voltage advances PLL output for $\Delta\phi$, i.e. $\theta^{+1} = \Delta\phi + \theta_{pll}$, (3) becomes:

$$\begin{aligned} U_d(t) &= -U^{+1} \sin(\Delta\phi) + U^{-1} \sin(2\omega t + \theta_0^{-1} + \theta_0^{+1} - \Delta\phi) \\ U_q(t) &= U^{+1} \cos(\Delta\phi) + U^{-1} \cos(2\omega t + \theta_0^{-1} + \theta_0^{+1} - \Delta\phi). \end{aligned} \quad (4)$$

Under balanced conditions, linearization of (4) results in the d axis voltage being proportional to the angle error, and the q axis voltage being proportional to the direct sequence voltage amplitude. In the presence of imbalance however, both U_d and U_q contain oscillatory terms at twice the line frequency. This prevents the conventional SRF PLL from providing satisfactory performance under unbalanced grid circumstances.

B. Direct sequence extraction using APF

In order for the SRF PLL to be able to reject the grid voltage imbalance, fast and robust direct sequence component extraction is needed [16]. The concept of instantaneous symmetrical components can be used for this purpose, either in $\alpha\beta$ or dq reference frame [10]. In any case, a 90° phase-shift operator is required to obtain waveforms which are in quadrature with the original signal. The quadrature signals can be obtained in several different ways [17]: DSOGI PLL [16], APF PLL [22], [23], EPLL [24], [25]. In this section we introduce an approach which relies on APF based direct sequence extractor cite [22]. APF alters only phase of the input signal, by changing it for 90° at a given frequency ω_{APF} , while the magnitude remains unaltered. Transfer function of a simple APF in continuous time domain is given by:

$$G_{APF}(s) = \frac{\omega_{APF} - s}{\omega_{APF} + s}. \quad (5)$$

Even though direct sequence extractor using APFs can be implemented in both synchronous rotating and stationary reference frame, we focus on APF based extraction in the dq frame (Fig. 1), since, as shown in [22], it provides a faster response than the approach with APFs in stationary frame. Following the approach in [22], the instantaneous direct sequence voltage components in dq frame can be calculated by:

$$\begin{aligned} U_d^{+1} &= -U^{+1} \sin(\Delta\phi) = \frac{1}{2}(U_d + U_q + \overline{U_d} - \overline{U_q}) \\ U_q^{+1} &= U^{+1} \cos(\Delta\phi) = \frac{1}{2}(-U_d + U_q + \overline{U_d} + \overline{U_q}) \end{aligned} \quad (6)$$

where $\overline{U_d}$ and $\overline{U_q}$ are obtained by 90° phase shifting of U_d and U_q . Note that (6) is implemented within signal cancellation block in Fig. 1.

As it will be shown via simulation results in Section IV, SRF PLL with APF as in-loop filters enables normal operation of the PLL in the presence of imbalance. It provides fast dynamic response when exposed to the voltage dip [22]. However, as reported in [25], its performance under harmonic distortion of the utility voltage is poor. In order to enhance its harmonic rejection capability, additional low-pass filters are proposed [17], [23], [25]. Parameter setting of these filters come as a compromise between the dynamic performance and the disturbance rejection capability. A frequency adaptation of the APFs might also be considered, so that the system is immune to the frequency variations [17], [25].

APF based direct sequence extraction which will be used as a benchmark for the comparison with the newly presented FSC method assumes simple implementation shown in Fig. 1, without any additional low-pass filters or frequency adaptive methods for APFs, since this paper focuses on the dynamic performance of the direct sequence extraction.

Fig. 2: Block diagram of the novel FSC extraction.

III. NOVEL FSC EXTRACTION

This section presents a new method for fast extraction of direct and inverse sequence components. Its block diagram is shown in Fig. 2. The concept will be described in detail in the first subsection. It relies only on two samples of the utility voltages which are firstly transformed into $\alpha\beta$ frame. Assuming that the grid frequency is known, these samples are then used to solve the system of linear equations in order to obtain the direct and inverse sequence voltage magnitudes and angles. An approximate system solution will be discussed so that computation of trigonometric functions is avoided. Since FSC algorithm requires frequency estimate, a simple derivative estimation is introduced in the last subsection.

A. Algorithm derivation

Transformation of the grid voltages at time t , represented by (1), into $\alpha\beta$ frame yields (2). In the next control period, i.e. at time instant $t + \Delta t$, where $\Delta t = T_s$ and T_s is the control period, voltages in $\alpha\beta$ frame are defined by:

$$\begin{aligned} U_\alpha(t + \Delta t) &= U^{+1} \cos(\theta^{+1} + \omega\Delta t) + U^{-1} \cos(\theta^{-1} + \omega\Delta t) \\ U_\beta(t + \Delta t) &= U^{+1} \cos(\theta^{+1} + \omega\Delta t - \frac{\pi}{2}) + U^{-1} \cos(\theta^{-1} + \omega\Delta t + \frac{\pi}{2}). \end{aligned} \quad (7)$$

For the purposes of the FSC algorithm derivation, the following expressions are introduced:

$$\begin{aligned} U_c^{+1} &= U^{+1} \cos(\theta^{+1}) \\ U_s^{+1} &= U^{+1} \sin(\theta^{+1}) \\ U_c^{-1} &= U^{-1} \cos(\theta^{-1}) \\ U_s^{-1} &= U^{-1} \sin(\theta^{-1}) \end{aligned} \quad (8)$$

$$\begin{aligned} K_c &= \cos(\omega\Delta t) \\ K_s &= \sin(\omega\Delta t). \end{aligned} \quad (9)$$

With the use of trigonometric identities and by substituting (8) and (9) into (2) and (7), we arrive at the system of equations to be solved in order to obtain cosine and sine factors of each sequence component ($U_c^{+1}, U_c^{-1}, U_s^{+1}, U_s^{-1}$):

$$\begin{aligned} U_\alpha(t) &= U_c^{+1} + U_c^{-1} \\ U_\beta(t) &= U_s^{+1} + U_s^{-1} \\ U_\alpha(t + \Delta t) &= K_c U_c^{+1} - K_s U_s^{+1} + K_c U_c^{-1} - K_s U_s^{-1} \\ U_\beta(t + \Delta t) &= K_c U_s^{+1} + K_s U_c^{+1} - K_c U_s^{-1} - K_s U_c^{-1}. \end{aligned} \quad (10)$$

Assuming that K_c and K_s are known, i.e. that the ideal grid frequency estimate is available, the solution of (10) is:

$$\begin{aligned} U_c^{+1} &= \frac{1}{2}(U_\alpha(t) + \frac{1}{K_s}(U_\beta(t + \Delta t) - K_c U_\beta(t))) \\ U_s^{-1} &= -\frac{1}{2}(U_\beta(t) + \frac{1}{K_s}(U_\alpha(t + \Delta t) - K_c U_\alpha(t))) \\ U_c^{-1} &= U_\alpha(t) - U_c^{+1} \\ U_s^{+1} &= U_\beta(t) + U_s^{-1}. \end{aligned} \quad (11)$$

Once the sine and cosine factors of each sequence component are available, it is easy to determine the direct and inverse sequence component voltage amplitudes and angles:

$$\begin{aligned} U^{+1} &= \sqrt{(U_c^{+1})^2 + (U_s^{+1})^2} \\ \theta^{+1} &= \text{atan2}(U_s^{+1}, U_c^{+1}) \\ U^{-1} &= \sqrt{(U_c^{-1})^2 + (U_s^{-1})^2} \\ \theta^{-1} &= \text{atan2}(U_s^{-1}, U_c^{-1}). \end{aligned} \quad (12)$$

The derived algorithm theoretically offers the extraction of the symmetrical components with no delay. Practical implementation of the FSC algorithm includes some form of filtering in order to obtain alias-free samples. Apart from the anti-aliasing filters, execution time is another issue that introduces the non-zero settling time. Since the proposed algorithm is basically rough differentiation, it is prone to noise. This can be alleviated by employing additional digital low-pass filter with high enough cut-off frequency and has to be taken into account when designing a proper filtering scheme. Also, in order to enhance the noise immunity, the concept described in this subsection can be adjusted so that more samples are taken into account when determining the direct and inverse sequence angles and amplitudes.

B. Approximate solution

In order to avoid calculation of the sine and cosine function, with the goal of reducing computational effort, (9) can be approximated by $K_c \approx 1$ and $K_s \approx \omega \Delta t$. This yields an approximate solution of (10):

$$\begin{aligned} U_c^{+1} &= \frac{1}{2}(U_\alpha(t) + \frac{1}{\omega \Delta t}(U_\beta(t + \Delta t) - U_\beta(t))) \\ U_s^{-1} &= -\frac{1}{2}(U_\beta(t) + \frac{1}{\omega \Delta t}(U_\alpha(t + \Delta t) - U_\alpha(t))) \\ U_c^{-1} &= U_\alpha(t) - U_c^{+1} \\ U_s^{+1} &= U_\beta(t) + U_s^{-1}. \end{aligned} \quad (13)$$

The error introduced by using (13) instead of (11) in (12) will be evaluated in the next section using simulations.

Further reduction of the computational effort can be achieved by avoiding use of arctan function in (12). This can be accomplished by at first determining the quadrant for both angles of interest and then using polynomial approximation of the arcsin function. Since state-of-the art digital platforms used to implement control of GSC are mostly equipped with the dedicated hardware unit which optimizes calculation of trigonometric functions, we focus on the algorithm implementation with (12).

Fig. 3: Simulated voltage dip type C: (a) with U_b and U_c phase change (b) without U_b and U_c phase change.

C. Frequency estimation

In the previously presented derivation of the FSC algorithm, it was assumed that an ideal estimate of the grid frequency is available. Since the utility frequency is a slow varying variable, this estimation does not have to be fast. Therefore, when determining an appropriate derivative estimation algorithm, the noise immunity is a more important issue than the speed of the response. However, since the chosen frequency estimation algorithm directly impacts the response of the FSC extraction algorithm when exposed to the frequency jump, a limiting factor is the desired frequency jump settling time.

In this paper, we implement a simple derivative estimation which relies only on two samples of θ^{+1} and assumes first order low-pass filter. In order to avoid numerical issues, ωT_s is estimated rather than ω . The following expression is used for this estimation:

$$\omega T_s(z) = \frac{K(z+1)}{z - (1-2K)} \Delta \theta^{+1}(z) \quad (14)$$

where $\Delta \theta^{+1} = \theta^{+1}(t + \Delta t) - \theta^{+1}(t)$ is the increment of θ^{+1} and K is the parameter that defines the low-pass filter cut-off frequency.

IV. SIMULATION RESULTS

In order to verify conclusions drawn in the previous two sections, simulation in MATLAB Simulink environment is created. Both benchmark and proposed extraction methods are implemented with the control period T_s of $100\mu s$. Simulation is realized so that sampling scheme can be either ideal or with an addition of the anti-aliasing filters. The latter one assumes that the grid voltages are firstly driven to the first order analog

Fig. 4: Simulated SRF and APF PLL response to voltage dip in Fig. 3a: (a) amplitude; (b) frequency.

low-pass filter with 5kHz cut-off. Filtered signals are sampled at 20kHz and further digital filtering is performed via first order low-pass IIR filter with 2kHz cut-off.

Transient performance is examined by evaluating response of the system to the voltage dip type C shown in Fig. 3 [22]. The dip with 80% positive and 20% negative sequence component occurs at time instant $t = 20\text{ms}$. Note that two different cases (Fig. 3a and 3b) are considered from the point of the phase of the grid voltage at the time instant when the dip occurs, since FSC extraction transient performance will prove to be significantly dependant on this phase. In Fig. 3a phase of U_b and U_c exhibits jump, whereas in Fig. 3b phase of U_b and U_c remains the same after the dip occurs.

Fig. 4 illustrates response of the conventional SRF PLL and APF based SRF PLL to the voltage dip type C shown in Fig. 3a. According to the presented results, oscillations which are present in both amplitude and frequency in case of conventional SRF PLL are successfully eliminated by the use of APF based in-loop filtering. As seen in Fig. 4a the settling time of the APF based SRF PLL is approximately 3ms which is in agreement with the one reported in [22]. Note that parameters of PI controller in both PLLs are set so that closed loop s domain transfer function exhibits characteristic polynomial with $\omega_n = 38\text{rad/s}$ and $\zeta = 1$ [22], [26]. An ideal sampling scheme is used for obtaining results in Fig. 4.

Fig. 5 and 6 illustrate the transient response of the FSC extraction under the voltage dip in Fig. 3a and 3b respectively. Performance of the FSC method is examined for two different implementations. The first one assumes an ideal sampling scheme and an ideal frequency estimation. The results obtained with this implementation are denoted as ideal (red waveforms in Fig. 5 and 6). The second implementation corresponds to the

practical application and assumes the aforementioned filtering scheme and frequency estimation described in the previous section. Parameter K from (14) is set so that low-pass filter with the 5Hz cut-off frequency is used for the derivative estimation. The results obtained with this implementation of the FSC extraction are denoted as filtered (blue waveforms in Fig. 5 and 6). Estimated frequency is shown only for the second implementation, since in the first one, the frequency is a constant defined by the grid frequency.

In an ideal, theoretical case, variables of interest are extracted immediately after the dip occurs. In the second case, which resembles practical implementation, transient performance of FSC extraction is defined by the dynamics of filters used in the acquisition path. With the previously mentioned parameters of the filters, the direct and inverse sequence voltage amplitudes are extracted in less than 1ms . Dynamic response in Fig. 6 is characterized by a considerable overshoot which is visible in all of the extracted variables. This behaviour might trigger protection algorithms unless adequately handled. Therefore, this issue has to be taken into account when considering practical implementation of the FSC extraction.

In order to examine an error introduced by the use of the approximate (13) instead of the exact system solution (11) in FSC algorithm, extracted direct and inverse sequence voltage amplitudes in the steady state are shown in Fig. 7 for both cases. The results shown in Fig. 7 are obtained with grid voltages which contain 80% direct and 20% inverse sequence component. The approximate system solution introduces an error due to an oscillatory term at twice the line frequency. Further examination has shown that this error depends on the control period as well as on the amplitude of both sequence components. As it will be verified in the experimental setup, use of an approximate system solution do not offer significant reduction in the computation time, since state-of the art DSPs have peripherals designed for hardware optimization of trigonometric functions calculation. Taking this into account, along with the error introduced in all of the extracted variables, use of an approximate system solution is not recommended.

V. EXPERIMENTAL VALIDATION

This section provides the experimental validation of the previously discussed extraction algorithms. Typhoon HIL 402 platform is used to emulate the grid via its analog outputs. The extraction algorithms are implemented on DSP based platform with TI f28379. Data presented in this section is obtained by exporting variables of interest from DSP's RAM. Filtering and sampling scheme of the HIL outputs exactly matches the one described in section IV. The same holds for the control loop parameters of both benchmark, APF, and newly introduced, FSC, extraction method.

In order to verify statements about the execution time reduction achieved by the use of the approximate system solution (13) in the FSC extraction, computation time was measured for the implementation with (13) and (11). With the use of Trigonometric Math Unit peripheral of F28379D and Code Composer Studio optimization tools, the execution time of the algorithm which involves sine and cosine

(a)

(b)

(c)

(d)

(e)

 Fig. 5: Simulated ideal VS. filtered FSC in response to voltage dip in Fig. 3a: (a) U^{+1} ; (b) θ^{+1} ; (c) U^{-1} ; (d) θ^{-1} ; (e) f .

(a)

(b)

(c)

(d)

(e)

 Fig. 6: Simulated ideal VS. filtered FSC in response to voltage dip in Fig. 3b: (a) U^{+1} ; (b) θ^{+1} ; (c) U^{-1} ; (d) θ^{-1} ; (e) f .

Fig. 7: Simulated FSC with approximate and exact system solution: (a) U^{+1} ; (b) U^{-1} .

function computation is $2.2\mu s$, whereas the implementation which assumes linearization of K_c and K_s is executed for approximately $2\mu s$. Thus, a negligible improvement of only $200ns$ is achieved. Unless properly handled, the error which (13) introduces significantly deteriorates performance of the FSC extraction as discussed in the previous section. Taking all of the previously said into account, FSC implementation with (11) is recommended and considered further on.

APF and FSC algorithms were tested under voltage dip shown in Fig. 3a. Extracted quantities are shown in Fig. 8. Benchmark response is shown only for the direct sequence voltage amplitude, angle and frequency since APF method does not offer the inverse sequence component extraction. As seen in Fig. 8a, settling time of both extraction algorithms is in agreement with the results obtain in simulations. FSC offers significantly faster response than APF. The biggest advantage of the FSC extraction is the settling time in the range of several hundreds of μs . Presented results point out that the FSC extraction is noise sensitive. This might limit its applicability unless noise immunity is improved. Development of an adequate adaptive filtering scheme should be considered in order to reduce the noise influence on the FSC performance.

VI. CONCLUSION

This paper has presented a novel FSC approach for very fast extraction of fundamental-frequency direct and inverse components from the unbalanced utility voltages. Simulation results have shown that under the voltage dip the ideal FSC method offers an immediate extraction, whereas practical implementation results in the settling time defined by the execution time and the required anti-aliasing filters. Transient performance of the FSC is compared to the APF based SRF

Fig. 8: Experimental results for APF and FSC under voltage dip in Fig. 3a: (a) U^{+1} ; (b) θ^{+1} ; (c) U^{-1} ; (d) θ^{-1} ; (e) f .

PLL experimentally. Even though FSC is significantly faster and offers extraction within several hundreds of μs , it is more noise prone. Noise influence can be minimized via designing a proper filtering scheme and will be considered as part of future work. To address this issue, an implementation of the FSC extraction with more than two samples should also be examined, as a kind of an improved adaptive filtering. Further studies also include FSC performance evaluation in presence of harmonics and DC bias. Attenuation of the most influential harmonics by adaptive notch filters will be investigated.

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