A Floating Differential DAC Expands the Output Voltage Range for Electrochemical Measurements

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Abstract—To operate a variety of electrochemical sensors, a potentiostat requires a large output voltage range. In order to implement this with a fully integrated potentiostat, we expand the digital-to-analog converter’s (DAC) output voltage range by providing a floating reference voltage with a current mirror and two amplifiers in negative feedback configuration. A segmented 16 bit resistor string (R-string) DAC uses the floating reference voltage to generate excitation signals within the supply voltage range. We show that our floating differential DAC supports an output voltage range from 0.32 V to 2.61 V when operated at a supply voltage of 3 V. Furthermore, the static and the dynamic performance of the DAC are maintained during output voltage range expansion. These properties suggest that our DAC is suitable for integration in an electrochemical measurement system.

Index Terms—Digital-to-analog converter (DAC), electrochemical measurement, excitation signal, output voltage range, point-of-care (POC), segmented resistor string

I. INTRODUCTION

Fast, portable, and low-cost measurement solutions are needed for point-of-care (POC) diagnostics. These diagnostic methods can be based on electrochemical measurements. Electrochemical measurement techniques are performed by an electronic device called potentiostat. The potentiostat applies a differential excitation voltage V_{cell} between two electrodes of an electrochemical sensor, the working and the reference electrode. In the three electrode configuration, the control loop of the reference electrode is closed over the sensor and sample using a third, counter electrode [1]. The required voltages between the electrodes therefore depend on the electrochemical sensor and determine the required output voltage range of the potentiostat’s digital-to-analog converter (DAC).

By supporting many electrochemical sensor types, such as the microneedle-based biosensor developed in the H2020 ELSAH project [2], integrated CMOS potentiostats with a wide output voltage range foster POC diagnostics development. This can reduce production and development costs. However, up to now, potentiostats are often designed for a specific electrochemical sensor and hence, support only a limited output voltage range.

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A. State-of-the-Art Output Voltage Range Restrictions

The majority of integrated potentiostats generate the differential excitation voltage V_{cell} with a single DAC, while the second electrode is connected to a fixed potential [3]–[17]. In [18]–[21], the potential of the working electrode is fixed to half of the supply voltage range, thus limiting the output voltage range to less than half of the supply voltage. References [14], [16], [22] use one of the supply rails as a fixed potential. This limits the cell voltage to one polarity. Even potentiostat architectures with two DACs [20], [23]–[25] seem to keep one electrode during the measurement at a fixed potential.

Setting one of the potentiostat electrodes to a fixed potential limits the output voltage range of the potentiostat and therefore limits the number of supported electrochemical sensors and applications.

B. Efficient Output Voltage Range Exploitation

A DAC architecture for potentiostats comprised of two DACs presented in [26] exploits the output voltage range more efficiently than conventional architectures. The two DACs set not only the differential voltage V_{cell} , but also control the absolute electrode potential relative to the system’s ground potential during electrochemical measurements. This dynamic electrode positioning at runtime exploits the output voltage range more efficiently because all three electrodes can float within the supply voltage range.

However, signal generation with two independent DACs is complicated. Digital control of V_{cell} is inconvenient since the differential voltage and its absolute potential cannot be adjusted independently. Furthermore, both DACs require a high resolution in order to avoid significant inaccuracies. This results in hardware overhead.

We therefore propose a floating differential DAC for integrated potentiostats with dynamic electrode positioning. The DAC supports a high output voltage range, almost reaching the supply rails, and versatile excitation signal capabilities.

II. DAC DESIGN CONSIDERATIONS

In order to implement dynamic electrode positioning, as demonstrated in [26], the DAC has to be able to generate output voltages over the whole supply voltage range.

Fig. 1. DAC output voltage range comparison. The output voltage range V_{out} of a conventional DAC is limited by the reference voltage V_{ref} . Amplifying V_{ref} or the DAC output voltage expands V_{out} , but decreases the resolution. Our proposed DAC can float within the supply voltage range by adding an adjustable positioning voltage V_{pos} . The DACs resolution is available over the whole output voltage range.

Fig. 2. Block diagram of the proposed floating differential DAC. The positioning voltage V_{pos} is set by feedback (dashed line). Adding V_{pos} and the reference voltage V_{ref} generates a floating reference voltage for the DAC.

A. DAC Output Voltage Range

The output voltage range V_{out} of conventional DACs is limited by the amplitude of the reference voltage V_{ref} . Amplifying either V_{ref} or the generated output voltage expands the output voltage range, but decreases the voltage resolution as shown in Fig. 1. The resolution can be increased at the expense of hardware overhead and design complexity.

The proposed design generates a floating reference voltage V_{ref} to expand the output range. A voltage adder circuit shifts V_{ref} up by the adjustable positioning voltage V_{pos} . Fig. 1 illustrates that the DACs resolution is available over the whole output voltage range.

The block diagram of this architecture is depicted in Fig. 2. A feedback loop that controls V_{pos} realizes dynamic electrode positioning to adjust V_{cell} adequately within the supply voltage range. Adding the voltages V_{pos} and V_{ref} generates a new floating reference voltage V'_{ref} for the DAC.

B. DAC Output Signal Capabilities

Electrochemical measurement techniques differ in their excitation voltage waveform. Constant voltages, step functions as well as sinusoidal excitation signals are used.

In order to support as many electrochemical measurement techniques as possible our proposed DAC can generate all three mentioned excitation signals over a wide output voltage range.

Fig. 3. Simplified schematic of the voltage adder block. The reference voltage V_{ref} is converted into a current I_{ref} and mirrored into a second branch. Amplifier A_2 and transistor M_1 add the positioning voltage V_{pos} .

III. FLOATING DIFFERENTIAL DAC

A current mirror based adder generates the floating reference voltage for the DAC. The DAC is based on a segmented resistor string (R-string) architecture. When biased with a constant current, the voltage drops across the R-string are independent of the absolute R-string potentials. Thus, this architecture can float within the supply voltage range. In addition, R-string DACs are suitable for low power designs as required by POC diagnostic devices.

Compared to a conventional DAC, the segmented architecture reduces the number of resistors and switches. In addition, signal generation complexity can be reduced, if the first stage generates the dc component and the second stage the ac component of the excitation signal [27].

A. Voltage Adder

The simplified schematic of the voltage adder is depicted in Fig. 3. Amplifier A_1 , transistor M_1 and resistor R_1 convert the reference voltage V_{ref} into a current I_{ref} . A matched transistor pair mirrors I_{ref} into a second branch. Amplifier A_2 and transistor M_2 regulate the bottom potential of resistor R_2 to V_{pos} . The voltage drop across R_2 adds V_{ref} if R_1 and R_2 are matched. The potential of node V_{sum} becomes

$$V_{sum} = V_{ref} + V_{pos}. \quad (1)$$

Fig. 4. Simplified schematic of the segmented 16 bit floating differential DAC. Two identical 8 bit resistor string (R-string) DACs are decoupled by operational amplifiers (A_3 to A_6). The generated voltage can be buffered by amplifier A_7 or low-pass filtered by the reconstruction filter (RCF). An analog multiplexer (MUX) selects the output signals.

B. Segmented R-string DAC

The simplified schematic of the segmented 16 bit R-string DAC is depicted in Fig. 4. Amplifiers A_3 to A_6 decouple the two identical 8 bit R-string DACs. The individual DACs are comprised of 256 polysilicon resistors and two 8 bit binary decoders. Amplifier A_7 buffers dc and step signals whereas the reconstruction filter (RCF) low-pass filters and buffers sinusoidal signals. The reconstruction filter is implemented by an active 2nd-order low-pass unity-gain Sallen-Key filter and is designed for a signal bandwidth of 10 kHz. An analog multiplexer (MUX) selects the output signals.

C. Realization

Our proposed floating differential DAC is part of an integrated potentiostat [28] and manufactured in a 130 nm standard CMOS process. The DAC is designed for a supply voltage of 3 V, but can operate at supply voltages down to 2 V. Decreasing the supply voltage decreases the DACs output voltage range. The DACs reference voltage is 1.2 V.

A micrograph of the manufactured integrated potentiostat with a layout overlay is shown in Fig. 5. The layout of the DAC and the positioning circuit are shown in more detail. In total, the two circuits cover an area of approximately 0.14 mm².

Fig. 5. Micrograph of the manufactured integrated potentiostat [28] with a layout overlay. The DAC and the positioning circuit are shown in more detail. They cover an area of approximately 0.14 mm².

Fig. 6. Measured test vector for DNL and INL characterization. The plot shows the absolute electrode potentials of the working and reference electrode which define V_{cell} . Our floating DAC supports an output voltage range V_{out} from 0.32 V to 2.61 V when operated with a supply voltage of 3 V.

IV. MEASUREMENT RESULTS

We measured 10 chips to characterize the static and dynamic performance of our proposed floating differential DAC.

The transfer functions for both 8 bit R-string DACs were measured independently after each other. By varying the positioning voltage V_{pos} , the DAC was shifted within the output voltage range. The measured output voltages are shown in Fig. 6. As illustrated in Fig. 6 our floating DAC supports an output voltage range V_{out} from 0.32 V to 2.61 V when operated with a supply voltage of 3 V.

A. Static Performance

The differential nonlinearity (DNL) and integral nonlinearity (INL) performances of each R-string DAC were calculated from the measured transfer functions. Fig. 7 shows the DNL and INL as a function of the digital input code of one chip for three different values of V_{pos} and three different feedback positions of amplifier A_2 (top, middle and bottom of R_2). The measurements confirm that the dynamic positioning within the supply voltage range does not influence the static performance. Asymmetry in the layout causes the deviation between the two R-strings.

Histograms with accumulated results of 10 chips are shown in Fig. 8. Over all operating conditions the DAC achieves a DNL within -0.26 LSB and 0.15 LSB, and an INL within -0.26 LSB and 0.11 LSB. Again, the measurements confirm that our proposed floating architecture does not introduce significant nonlinearities.

B. Dynamic Performance

The signal-to-noise-and-distortion ratio (SNDR) as a function of the DAC's output frequency is plotted in Fig 9. Measurements were done for two chips, one with and the other without dynamic electrode positioning. The SNDR is nearly identical over the observed frequency range in both cases. Hence, output voltage range expansion does not influence the DAC's dynamic performance.

Sinusoidal signals with amplitudes of -6 dBFS and frequencies from 3 Hz to 10 kHz were generated for the dynamic performance characterization of the DAC. Stage 1 set the dc

Fig. 7. Measured DNL and INL performance of one chip. Red lines show results for the first and blue lines for the second R-string. Color shading distinguishes different positions in the output range as illustrated in Fig. 6.

level and stage 2 generated the ac component. The sample rate was approximately 100 kHz. The SNDR was calculated over a bandwidth of half the sample rate.

As the DAC is part of a potentiostat, the power consumption of the DAC itself cannot be measured. Post-layout simulation results estimate that the maximum power consumption is 132 μ W from a 3 V supply. The output signal frequency and the sample rate were set to 10 kHz and 100 kHz respectively.

A comparison of our design to selected potentiostats is shown in Table I. The output voltage range to supply voltage ratio of our DAC is superior.

TABLE I
COMPARISON OF SELECTED IMPLEMENTATIONS

	This work	[24]	[25]
Supply voltage (V)	3	1.8	3
Output voltage range (V)	0.32 - 2.61 ^a	-	0.2 - 2 ^a
Resolution (bit)	16	8	10

^a Measured

Fig. 8. Measured DNL and INL performance over 10 chips, for both R-string stages, first in red, second in blue. The histogram shows accumulated data while in different floating modes shifted over the output range as shown in Fig. 6.

Fig. 9. Measured SNDR of the floating differential DAC. Dynamic electrode positioning does not change the performance significantly.

V. CONCLUSION

Our floating differential DAC meets the versatile requirements of an integrated potentiostat with dynamic electrode positioning. The presented DAC expands the output voltage range compared to a conventional architecture. Output signals from 0.32 V to 2.61 V with a 16 bit resolution can be generated when operated with a supply voltage of 3 V. Measurement results show that the static and the dynamic performance of the

DAC are not influenced by the output voltage range expansion. These results enable portable and low-cost electrochemical measurement solutions for POC diagnostics.

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