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A Four-Channel Gray-Code Addressing TDM Clocked-Analog LDO for Thermo-Optic Tuning in Silicon Photonics

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Abstract—This paper presents a Gray-code addressing time-division multiplexing (TDM) clocked-analog low-dropout regulator (CLDO) that shares one controller between four output channels with only one compensation capacitor. We apply the Gray-code addressing strategy to reduce the crosstalk. We also apply the split-output amplifier structure to share the compensation capacitor for further chip area reduction. In addition, we introduce a lightweight local-generated supply to increase the dynamic range. Implemented in 130 nm CMOS process, this design has a total chip area of 0.056 mm², which is 67.5% smaller than the conventional solution with four identical LDOs. Post-layout simulation results show that the presented four-channel TDM CLDO can simultaneously track four 1 V_{pp} sinusoidal signals at different frequencies with negligible crosstalk. This TDM CLDO is a promising solution for supplying multiple thermo-optic phase shifters (TOPSs) in silicon photonics.

Index Terms—Low dropout regulator, time-division multiplexing, thermo-optic phase tuning, electronic-photonic integrated circuits, area reduction.

I. INTRODUCTION

Silicon photonics (SiPh) is attracting increasing attention in recent years for its unique benefits of high data rate, low transmission loss, wide spectrum range [1], [2], etc. Fig. 1 shows the general model of a thermo-optical tuning of silicon photonics [2]. It mainly includes four parts: photonic devices, monitors, controllers, and power management circuits. The controllers, typically driven by power management circuits (PMCs), are key modules to realize closed-loop feedback of SiPh. The scalability of thermo-optical tuning is greatly limited by the PMCs. For example, to meet the resolution requirements in the optical phased arrays (OPAs), independent tuning of hundreds even thousands TOPSs are required. In conventional designs, each TOPS is supplied by an independent power management circuit. Although the TOPS can be as small as 10 μm² [3], the power management circuit is much larger. The area mismatch between TOPSs and PMCs will limit system scalability as the number of TOPSs increases.

Hardware sharing is an effective way to reduce the total chip area of the power management circuits. The TDM CLDO based on hardware sharing is first demonstrated in [4], [5]. As shown in Fig. 2, the TDM CLDO shares one controller between N power stages. Compared with conventional designs that apply N independent LDOs, the TDM CLDO saves the chip area of $(N - 1)$ controller.

Fig. 1. A general model for the thermo-optical tuning in SiPh [2].

Many new requirements are put forth on the multi-channel supply for thermo-optic phase tuning. However, the previous TDM CLDO designs are not optimized for that purpose. The first demonstration only achieves dual-channel controller sharing [5]. In addition, the compensation capacitor in the controller cannot be shared, making it difficult to expand to more output channels. A four-channel TDM digital LDO was presented in [6]. The controller is complicated, and the total chip area is larger than its analog counterpart. The output range of previous designs is as small as 0.1 V and is not sufficient for thermo-optic phase tuning, which requires a wide output range.

In this paper, we present a four-channel TDM CLDO that is optimized for the thermo-optic phase tuning in SiPh [7]. It features small crosstalk, small chip area, and wide dynamic range. We adopt the Gray-code addressing technique to eliminate the crosstalk caused by clock timing errors. In addition, we apply a split-output amplifier structure, making it possible for compensation capacitor sharing. Furthermore, We also introduce a lightweight local generated supply (LLGS) to increase the dynamic range. The remainder of this paper is organized as follows. Section II analyzes the requirements of TOPSs on the power management circuit. Section III discusses the structure and operating principles of the presented four-channel TDM CLDO. Section IV shows simulation results. Finally, Section V draws the conclusion.

II. TOPS AND POWER MANAGEMENT CIRCUIT

The simplest TOPS can be realized by placing a resistive heater near the waveguide [3]. The heater is driven by a power

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Fig. 2. (a) Multiple independent LDOs and (b) multi-channel TDM CLDO.

Fig. 3. Structure of the four-channel Gray-code addressing TDM CLDO.

supply and it changes the temperature of the waveguide. Due to the thermo-optic effect, the effective index of the waveguide is modified, resulting in the phase change of the optical signal.

LDO is a well-developed on-chip PMC suitable for driving the TOPS. The requirements of the LDO in thermo-optical tuning are different from traditional designs. Most conventional LDOs are specifically designed for SoCs that require a well-regulated output in a wide load range [8], [9]. By contrast, the LDO in thermo-optical tuning should provide a dynamic output to a fixed resistive load. The output range should be sufficiently large, but the required maximum output power is small. Furthermore, since each TOPS requires an independent power management circuit, a large number of LDOs will be required for large-scale designs.

III. FOUR-CHANNEL TDM CLDO

Fig. 3 shows the structure of the presented TDM CLDO. The shared controller is connected with four power stages. Since the power consumption of each output channel is small, the size of the power stage in LDOs is significantly reduced. As a result, the controller dominates the chip area and sharing the controller between multiple output channels is an effective method for chip area reduction.

In this section, we first analyze different addressing strategies for channel selection. Then, we discuss the structure of the four-channel TDM CLDO in detail. Specifically, we focus

Fig. 4. Timing diagrams of the binary-code addressing technique in (a) the ideal condition and (b) the timing-error condition.

on the structure of the split-output amplifier that can share the compensation capacitor and the LLGS with a two-stage charge pump that can improve the output dynamic range. Furthermore, we build a small-signal model for stability analysis. In addition, we analyze output errors and area-reduction ratio of this design.

A. Addressing Strategies

The power stages in TDM CLDO can select different addressing strategies. Depicted in Fig. 4, binary-code addressing is a widely adopted addressing technique. Nevertheless, the timing errors of different clock signals in the binary-code addressing technique would result in spikes. As shown in Fig. 4 (b), the spikes would result in connecting the controller with CH_0 for a short period when it switches from CH_2 to CH_1 . The short period may cause stability problems. To eliminate the short period caused by the timing error, the Gray-code addressing technique is applied in our structure. The Gray-code addressing switches are realized with cascaded transfer gates. As shown in Fig. 4 (c), since there is only one-digit change at each switching moment, the timing errors of the clock signals would only shorten or lengthen the enabled period, but not introduce spikes.

B. Split-Output Amplifier

For stability concerns, compensation capacitor C_m is required in most LDO designs. The capacitor typically occupies a large area. Sharing C_m can be an effective way to further reduce the total chip area. However, C_m is usually connected between the controller and the power stage, and cannot be shared in previous designs [5].

To solve this problem, we adopt the split-output amplifier structure in [10]. Fig. 5 shows the schematic of the structure. It introduces an auxiliary output stage that has scaled-down MOS of the actual output stage. Since the auxiliary output stage does not need to switch between different power stages, the nodal

Fig. 5. Schematic of the split-output amplifier.

Fig. 6. Simulated frequency responses at different C_m .

voltage is stable. Consequently, connecting the compensation capacitor between the output of the first stage and the auxiliary stage is better for stability. We also introduce a resistor in parallel with the compensation capacitor.

Fig. 6 shows the simulated frequency responses of the TDM CLDO with different values of the shared compensation capacitor. As C_m increases from 100 fF to 1 pF, the main pole moves to the low-frequency region, and the unit-gain bandwidth reduces from 10 MHz to around 7.8 MHz. The phase margin in all situations is kept around 60° , indicating that the TDM CLDO with the split-output amplifier is always stable even if the compensation capacitor is shared between different channels.

C. Lightweight Local Generated Supply

We introduce the lightweight-local generated supply structure [11] to the TDM CLDO. As shown in Fig. 3, the LLGS enables us to provide a low voltage supply to the power stage when the required output voltage from the TOPS is low. Meanwhile, the supply voltage of the error amplifier is not influenced and can be sufficiently high to guarantee high performance.

Fig. 7 shows the schematic of the LLGS structure. The main part is a two-stage charge pump. It doubles the input voltage to

Fig. 7. Schematic of the lightweight-local generated supply (LLGS).

Fig. 8. Output of the LLGS at different charge pump frequencies.

a reasonably high value to supply the error amplifier. However, since the supply voltage of the power stage has a wide dynamic range, the output voltage of the charge pump can be even higher than the safety voltage of the transistor if the supply of the power stage is connected with the input of the charge pump directly. To solve this problem, we adopt a source follower at the input of the charge pump. Since the input of the charge pump will be determined by the reference signal rather than the supply, the LLGS can serve as the supply of the split-output amplifier over a wide dynamic range.

Fig. 8 shows the output of the LLGS at different switching frequencies. As the switching frequency increases, the output of the LLGS approaches 900 mV, which is sufficiently high for the error amplifier in the shared controller.

D. Small-Signal Analysis

To analyze the stability of the four-channel TDM CLDO, we also build the small-signal model with heavy load, as shown in Fig. 9. V_i , C_i , R_i , and g_{m_i} ($i = 1, 21, g, out$) are the nodal voltages, parasitic capacitors, output resistors, and transconductance at the first stage, the auxiliary output, the real output of the error amplifier, and the output of the LDO. To simplify the analysis, we make the following assumptions:

- Poles (zeros) are far away from each other;
- Parasitic capacitors (except C_3 that includes the parasitic capacitor at the gate of the power transistor) are much

Fig. 9. Small-signal model of the proposed TDM CLDO.

smaller than the compensation capacitor and the output capacitor.

The simplified transfer function is shown in (1), where

$$P_1 = \frac{1}{C_g R_g} \quad (2)$$

$$P_2 = \frac{1}{C_1 R_1 + C_m R_{21} + C_m R_1 (g_{m21} R_{21} + 1)} \quad (3)$$

$$P_3 = \frac{1}{C_m R_{21}} + \frac{g_{m21}}{C_1} + \frac{1}{C_1 R_1} + \frac{1}{C_1 R_{21}} \quad (4)$$

$$P_4 = \frac{1}{C_p R_p} \quad (5)$$

$$Z_1 = \frac{1}{C_m R_{21}} \quad (6)$$

E. Output Errors and Area-Reduction Ratio

Since the output cannot track the reference when the power stage is disconnected with the controller, sharing the controller would introduce output errors at all channels. The output error of the TDM CLDO is related to the number of channels N , the reference frequency f_r , and the clock frequency f_{clk} . According to the analysis in [5], the relative output error in each channel is

$$\delta V_{err} \leq 2 \sin \left(\frac{N-1}{N} \times \frac{\pi f_r}{f_{clk}} \right) \quad (7)$$

According to [12], a 4-bit resolution is sufficient for the nearly error-free operation of a 128-element 1-D OPA. As long as the clock frequency f_{clk} is larger than $100f_r$, all output channels can meet the resolution requirement theoretically. As the reference frequency can be as low as tens of kHz in TOPSSs, the clock frequency can be easily obtained, and the TDM CLDO can be extended to more channels.

To evaluate the area reduction effect of the TDM CLDO, we adopt the area reduction ratio defined in [5]

$$R_{re} = 1 - \frac{S_C + N(S_P + S_L)}{N(S_C + S_P + S_L)} = \frac{N-1}{N} \times \frac{\frac{S_C}{S_P + S_L}}{\frac{S_C}{S_P + S_L} + 1}, \quad (8)$$

where S_C , S_P , and S_L is the chip area of the controller, power stage, and the load separately. The area reduction effect becomes more evident when the controller is large or the power stage is small.

Fig. 10. Microphotograph of the four-channel TDM CLDO.

Fig. 11. Output ripples of the TDM CLDO when the supply ripple is 200 mV at 100 kHz.

IV. POST-LAYOUT SIMULATION RESULTS

Fig. 10 (a) shows the layout of the four-channel TDM CLDO in a 130nm CMOS process. The total chip area is about 0.056 mm², and the chip area of the shared controller (including the error amplifier and the LLGS) is much larger than that of the power stage of each channel. Fig. 10 (b) shows the area of the LDOs with different numbers of channels. Compared with the conventional solution, 67.5% chip area is saved in the four-channel condition.

Fig. 11 shows the outputs of the TDM CLDO when the references of all channels are fixed while the supply ripple is 200 mV at 100 kHz. The maximum voltage variance at the output is around 11.7 mV, which is equivalent to 24.7 dB

$$T(s) = \frac{V_{out}}{V_{in}} \approx - \frac{g_{m1} g_{m2} g_{mp} R_1 R_g R_p (S + Z_1)}{(S + P_1)(S + P_2)(S + P_3)(S + P_4)} \quad (1)$$

Fig. 12. Four-channel outputs of the TDM CLDO when the maximum clock switching frequency is at (a) 2 MHz, (b) 20 MHz.

Fig. 13. Maximum swing of four-channel outputs of the TDM CLDO with (a) $V_{in} = 0.6$ V, and (b) $V_{in} = 1.2$ V.

power supply rejection.

Fig. 12 shows the outputs of the TDM CLDO at four channels when the reference frequency is 100 kHz and the maximum clock switching frequency is 2 MHz and 20 MHz separately. The output errors at all channels are reduced as the clock switching frequency increases.

Fig. 13 shows the maximum swing of the TDM CLDO. The results show the TDM CLDO can work when input voltage varies from 0.6 V to 1.2 V, and that the maximum swing of output can reach 1 V.

TABLE I summarizes the performances of the presented four-channel TDM CLDO and compares it with previous LDO designs. The comparison results show that the TDM CLDO performs equally well with traditional single-channel LDO designs. Though with much larger control units, the average area per channel occupied is slightly larger than the previous dual-channels TDM CLDO design [5] for the multiplexed compensation capacitor and the increased number of channels in this design. Additionally, owing to the LLGS, the output voltage range of the proposed design can reach 1 V with 1.2 V input voltage, superior to other designs.

V. CONCLUSION

In conclusion, SiPh is a burgeoning research topic that has great potential in many applications. The large-quantity, small-power, and pure resistive features of the TOPS in SiPh put forth many new requirements on the PMC. In this work, we present a four-channel TDM CLDO that shares the controller with multiple output channels and is suitable for thermo-optical tuning in SiPh. We apply the Gray-code addressing technique to reduce the crosstalk between different channels. In addition, we also adopt the split-output amplifier that can share the compensation capacitor. Furthermore, we introduce an LLGS structure to increase the dynamic range as well. This structure can be applied to more output channels.

TABLE I
PERFORMANCE COMPARISON

	[13] JSSC'17	[14] ISSCC'17	[6] ESSCIRC'19	[5] TCAS-I'21	This work
# of ch.	1	1	4	2	4
Type	DLDO	ALDO	TDM DLDO	TDM CLDO	TDM CLDO
Tech. [nm]	65	65	65	130	130
Average area per ch. S_{ch} [μm^2]	0.158	0.016	0.271	0.012	0.014
I_O [μA]	300	32	26.25*4	43*2	10*4
V_{in} [V]	0.6-1.0	0.2-0.6	0.8-1.2	0.85-1.2	0.6-1.2
Output range [V] @input voltage [V]	0.1@0.65	0.25@0.6	0.1@1.2	0.3@1.2	1@1.2
I_{load} [mA]	50	50	50*4	20*2	40*4
C_{load} [pF]	1500	40	100*4	39*2	20*4
C_c [fF]	-	100	N.A.	200*2	100*1
$f_{tracking}$ [kHz]	50	N.A.	50	100	100
$V_{tracking}$ [mV]	100	N.A.	100	300	1000
FOM [†] [$\text{pF} \cdot \mu\text{s} \cdot \text{nm}^2 / \text{k}\Omega$]	142.2**	N.A.	54.375**	0.72	0.028

Here “-” stands for “not needed”, “N.A.” stands for “data not available”.

[†]FOM = $(C_{load} / N_{ch} \times I_O / N_{ch} \times S_{ch}) / (f_{tracking} \times V_{tracking})$ [5]

** Calculated from the results estimated from the figures

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