A Lossy Integrator with Active Bias Point

Emad Alnasser, Dobromir P. Dobrev, Tatyana D. Neycheva

Abstract—The charge-generating sensors are widely used in many applications in consumer, automotive and medical electronics. The sensor output generates a charge proportional to the applied input quantity: pressure, acceleration, strain, light, etc. Usually, charge amplifiers are used to register such signals. The charge amplifier is an integrator that integrates the input current over time. In continuous-time signal processing, a parallel resistor is used to dissipate the energy stored on the integration capacitor, and such self-zeroed integrator circuits are known as lossy integrators. To achieve low-frequency operation, when a capacitor is in the pico-farad range, a very high-ohmic resistor, in the range of giga-ohms, must be used. Such a high-ohmic resistor increases the output offset voltage to an unacceptable level. To overcome the output offset problems, a composite charge amplifier with active feedback has been introduced. This paper presents a simplified lossy integrator circuit which uses only one opamp in the feedback. The presented circuit can be easily adapted to the needed cut-off frequency and gain. It is validated by practical measurements and can benefit many applications where charge-to-voltage conversion is needed.

Index Terms—active feedback, charge amplifier, composite amplifier, input offset voltage, lossy integrator

I. INTRODUCTION

THE piezoelectric and pyroelectric sensors are charge-generating sensors widely spread in many applications in consumer, automotive and medical electronics [1-4]. They generate an output charge proportional to the applied input quantity: pressure, acceleration, strain, light, etc. The generated charge usually is registered by a readout circuit called a charge amplifier [5-22]. The charge amplifier is a low-frequency transimpedance amplifier or current-to-voltage converter characterized by its transfer impedance $Z(s)$, which is a capacitance (1).

$$Z(s) = -\frac{1}{sC_f} \quad (1)$$

In other words, it is an integrator and integrates the input current over time, thus converts the captured charge into an output voltage. To return the integration capacitor C_f to its

initial zeroed state, the stored energy must be dissipated. In continuous-time signal processing a parallel resistor, R_f is used for this purpose, and such self-zeroed integrator circuits are called lossy integrators, see Fig. 1 (a).

Fig. 1. Lossy integrators. (a) conventional circuit, (b) with “T” resistive network in the feedback.

The transfer impedance Z_{LI} of a conventional lossy integrator (LI), shown in Fig. 1 (a), is:

$$Z_{LI}(s) = -\frac{R_f}{1 + sR_fC_f} \quad (2)$$

The resistor R_f provides also a path for the input bias current of the opamp inverting input and is essential for the normal operation of the circuit. The worst-case output offset voltage V_{Loo} of the circuit from Fig. 1 (a) is given by (3).

$$V_{Loo} = R_f |I_b| + |V_{io}| \quad (3)$$

where I_b and V_{io} are the input bias current and the input offset voltage of the used opamp. The output offset voltage V_{Loo} increases by increasing the value of R_f . To achieve low-frequency operation, when the capacitor C_f is in a pico-farad range, a very high-ohmic feedback resistor R_f , in the range of giga-ohms and even tera-ohms, must be used, therefore the output offset voltage of the circuit becomes very large [2].

Implementing a voltage divider in the feedback path by a “T” resistive network, as shown in Fig. 1 (b), multiplies the voltage over the resistor R_f . Let’s denote the reciprocal value of the resistor divider gain from Fig. 1 (b) by the coefficient k , as is expressed by (4):

$$k = \frac{R_a + R_b}{R_b} \quad (4)$$

When $R_f \gg R_b \gg R_a$, the transfer impedance and the output offset of the circuit from Fig. 1 (b) become:

E. Alnasser is with NouTronics Research and Development group (founder), Abadan, Iran (corresponding author e-mail: ernalnasser@noutronics.com).

D. P. Dobrev is with Institute of Biophysics and Biomedical Engineering at the Bulgarian Academy of Sciences, Sofia, Bulgaria (e-mail: dobri@biomed.bas.bg).

T. D. Neycheva is with Institute of Biophysics and Biomedical Engineering at the Bulgarian Academy of Sciences, Sofia, Bulgaria (e-mail: tatiana@biomed.bas.bg).

$$Z_{TLI}(s) = -\frac{kR_f}{1 + skR_fC_f} \quad (5)$$

$$V_{TLI_{oo}} = k(R_f|I_b| + |V_{io}|) \quad (6)$$

It can be seen that together with R_f , the V_{io} is also multiplied by the coefficient k . To reduce the offset component due to the input current I_b , JFET or CMOS opamps are usually used [2, 21-22]. In spite of that, when R_f is very large, the currents of the input ESD protection and their temperature drift, generate an output offset voltage that is inadmissible in many precision applications [21]. In these applications, the use of costly electrometer opamps, manufactured without ESD protections and soldered with special measures against ESD events, is a well-known solution to overcome this problem.

To reduce the output offset voltage without violating the noise performance of the circuit, a composite charge amplifier has been introduced [22]. It uses active feedback to eliminate the output offset voltage. This paper presents a simplified lossy integrator circuit with only one opamp in the feedback. It is fully equivalent to the published version with three opamps. The circuit is analyzed in detail, and general guidelines for design and optimal component selection are given. The circuit is prototyped, and its operation is validated by the shown experimental results.

II. OPERATING PRINCIPLE

The main idea to cancel the integrator output offset voltage is to build a composite amplifier with active negative feedback. With the help of additional opamps, placed in the feedback, the output offset can be translated to another node in the circuit, where the offset voltage is not critical. The idea is to replace the feedback resistor R_f with an active circuit, as shown in the block diagram in Fig. 2 (a).

Fig. 2. Lossy integrators with active feedback. (a) block diagram, (b) schematic with two opamps in the feedback, (c) schematic with one opamp in the feedback.

The active feedback must transfer the low-frequency changes at the opamp output to its inverting input. It must close the negative feedback and must define the bias point at the opamp inverting input to be a virtual ground. The active feedback should exhibit high impedance for the bandwidth of interest, i.e. its action should be disconnected at the higher frequencies. In other words, the active feedback must imitate a very large inductor. A composite LI circuit with such active feedback has been introduced in [22]. Its schematic is shown in Fig. 2 (b). It achieves very low output offset voltage without using costly electrometer opamps and only by using general-purpose JFET opamps. However, its disadvantage is that the circuit uses two opamps in the feedback path. The simplified LI circuit with one opamp in the feedback is shown in Fig. 2 (c). By the U_2 action, the output offset is controlled and is eliminated from the circuit output.

III. CIRCUIT ANALYSIS

A. DC Analysis

The output offset voltage of the circuit from Fig. 2 (c) is determined by the opamp U_2 . From DC point of view, the negative feedback around the main amplifier U_1 is provided by the opamp U_2 , therefore the circuit has a stable and well-defined bias point. A simple and straight forward DC analysis shows that the worst-case output offset voltage V_{ool} of the

circuit is given by the following equation:

$$V_{ool} = R_i |I_{b2}^+ - I_{b2}^-| + |V_{io2}| \quad (7)$$

where I_{b2}^+ and I_{b2}^- are the input currents of non-inverting and inverting inputs of the U_2 respectively, and V_{io2} is the input offset voltage of the opamp U_2 . It is worthy to mention equation (7) has been obtained by assuming that the opamps have large DC open-loop gain which is a reasonable assumption. According to this assumption, both inverting and non-inverting inputs of U_2 have the same potential. Anyway, as it can be deduced from (7) the output offset voltage is very low in comparison with (3) and (5) because the value of resistor R_i is very smaller than that of the product kR_f or R_f .

By assuming $R_f \gg R_b \gg R_a$, the worst-case DC potential at node V_F can be expressed by the equation (8):

$$V_F = k(R_f |I_{b1}^-| + |V_{io1}|) \quad (8)$$

Here I_{b1} and V_{io1} are the input current of the inverting-input and input offset voltage of the opamp U_1 respectively, k is the coefficient already defined in (4).

B. AC Analysis

The AC analysis has been performed by using the equivalent signal-flow-graph diagram (SFG) which is valid for both circuits shown in Fig. 2 (b) and Fig. 2 (c). The equivalent SFG diagram is shown in Fig. 3.

Fig. 3. The equivalent SFG diagram of the circuits from Fig. 2.

The opamp inverting input is a summing node that sums the input current I_{in} and the feedback current I_β . The forward gain is given by (1). As is shown in Fig. 3, it is defined by the integration capacitor C_f . The feedback gain $\beta(s)$ is a transconductance, and is expressed by the equation (9):

$$\beta(s) = \frac{I_\beta(s)}{V_{out}(s)} = \frac{1}{kR_f} \cdot \frac{1}{1 + sR_bC_1} \cdot \frac{1 + sR_dC_i}{sR_iC_i} \quad (9)$$

The coefficient k in (9) has been discussed. For the circuits in Fig. 2 (b) and Fig. 2 (c) it is defined as follows:

$$k = \begin{cases} \frac{R_b}{R_a}, & \text{for the circuit on Fig. 2 (b)} \\ 1 + \frac{R_b}{R_a}, & \text{for the circuit on Fig. 2 (c)} \end{cases} \quad (10)$$

The loop gain is responsible for the stability of each control system with negative feedback. It must be evaluated, and when the loop gain becomes unity or 0dB, the accumulated phase lag must be lower than 135° , i.e. the worst-case phase margin of the closed-loop system must be higher than 45° , preferably higher than 65° . The open-loop gain $T_{OL}(s)$ is:

$$T_{OL}(s) = \frac{1}{skR_fC_f} \cdot \frac{1}{1 + sR_bC_1} \cdot \frac{1 + sR_dC_i}{sR_iC_i} \quad (11)$$

Equation (11) represents a chain of two cascaded integrators and a first-order low-pass filter. It is a third pole transfer function, and to have a stable closed-loop response, it must be compensated to intersect the 0dB axis with approximately -20dB/dec roll-off. This is possible only when the low-pass filter does not introduce a large phase lag, i.e. its pole must be placed to influence on higher frequencies, far away from 0dB crossover frequency. Because the two integrators have -40dB/dec roll-off, one of them should be compensated by an appropriate selected zero. Equation (11) has four time constants, defining four corner frequencies. The time constant τ_f , determines f_f , the unity-gain-frequency (UGF) of the main integrator, see (12).

$$\tau_f = kR_fC_f = \frac{1}{\omega_f} = \frac{1}{2\pi f_f} \quad (12)$$

The time constant τ_i , determines f_i , the UGF of the feedback integrator, see (13).

$$\tau_i = R_iC_i = \frac{1}{\omega_i} = \frac{1}{2\pi f_i} \quad (13)$$

The time constant τ_b determines the cutoff frequency f_b of the low-pass filter, see (14).

$$\tau_b = R_bC_1 = \frac{1}{\omega_b} = \frac{1}{2\pi f_b} \quad (14)$$

And the time constant τ_z determines the zero frequency f_z :

$$\tau_z = R_dC_i = \frac{1}{\omega_z} = \frac{1}{2\pi f_z} \quad (15)$$

The crossover frequency f_c , where $T_{OL}=1$, can be calculated by the following simple steps. Let's assume initially that the τ_z and τ_b are zero. The equivalent UGF of the two cascaded integrators f_u is in a geometric mean with f_f and f_i :

$$f_u = \sqrt{f_f f_i} \quad (16)$$

If the zero frequency f_z is selected to be n times lower than f_u :

$$f_z = \frac{f_u}{n} \quad (17)$$

The crossover frequency f_c is:

$$f_c = n f_u \quad (18)$$

The phase margin is:

$$\varphi_m = \arctan(n^2) \quad (19)$$

From equation (19) when $n=2$, the phase margin is about 76° . The -3dB high-pass cutoff frequency f_{3dB} of the closed-loop response depends on the selected phase margin and for this example it is approximately:

$$f_{3dB} \approx 0.74 f_c \quad (20)$$

To not reduce significantly the phase margin the low-pass cutoff frequency f_b should be selected to be $f_b \gg f_c$, let say it should be more than one decade higher.

An example of a practical procedure for proper component selection can be given as follows:

- select C_f for a needed closed loop-gain
- select starting values for R_f and k
- check by (8) for the possible maximum voltage at node V_F and reselect R_f and k
- from (12) calculate τ_f and f_f
- select starting values for R_i and C_i
- from (13) calculate τ_i and f_i
- from (16) calculate f_u
- set $n=2$ and from (17) and (15) calculate f_z , τ_z and R_d
- from (18) and (20) calculate f_c and f_{3dB}
- select $f_b=100f_c$ and from (14) calculate C_l
- simulate $T_{OL}(s)$ by (11) and check f_c , and φ_m
- make interactions and repeat some of the above steps if needed

For completeness, the closed-loop transimpedance gain is:

$$T_{CL}(s) = \frac{V_{out}(s)}{I_{in}(s)} = \frac{Z(s)}{1+T_{OL}(s)} \quad (21)$$

In eq. (21) $Z(s)$ and $T_{OL}(s)$ should be replaced by (1) and (11). For higher frequencies $T_{OL}(s) \approx 0$, thus $T_{CL}(s) \approx Z(s)$.

IV. SIMULATION RESULTS

A. Open-loop Gain

PSpice simulation of the magnitude and phase of the open-loop gain $T_{OL}(s)$, given by equation (11), is shown in Fig. 4.

Fig. 4. PSpice simulation of $T_{OL}(s)$.

The used component values are: $C_f=200\text{pF}$, $R_f=20\text{M}\Omega$, $C_i=4.7\text{uF}$, $R_i=3\text{M}\Omega$, $R_d=510\text{k}\Omega$, $R_a=10\text{k}\Omega$, $R_b=240\text{k}$, $C_l=470\text{n}$. The simulation proves the described procedure for component selection. The simulated $f_c=0.277\text{Hz}$, and the phase margin is $\varphi_m=76.1^\circ$. When the circuit operates as an AC amplifier, the high-pass cutoff frequency f_{3dB} of the closed-loop response, can be calculated by (20) and is $f_{3dB} \approx 0.2\text{Hz}$.

B. Frequency Response

Frequency responses of two AC amplifiers, built with an active-biased integrator (ABI) circuit from Fig. 2 (c), and a conventional LI (CLI) circuit from Fig. 1 (a), are compared by PSpice simulations. To perform the simulation, an AC-amplifier, shown in Fig. 5, is implemented by using both an ABI and a conventional CLI circuits.

Fig. 5. AC amplifier built with a LI.

It should be mentioned that the transfer functions of AC amplifiers implemented by ABI and CLI circuits are given by equations (22) and (23), respectively.

$$A_{ABI}(s) = \frac{V_{out}(s)}{V_s(s)} = sC_s T_{CL}(s) \quad (22)$$

$$A_{LI}(s) = \frac{V_{out}(s)}{V_s(s)} = sC_s Z_{LI}(s) \quad (23)$$

where $T_{CL}(s)$ and $Z_{LI}(s)$ are the closed-loop transimpedance gain given by (21) and (2). By assuming $C_s=2\text{nF}$ and the component values from the previous section for the ABI circuit from Fig. 2 (c), or $C_s=2\text{nF}$ and $R_f=4\text{G}\Omega$ for CLI circuit

from Fig. 1 (a), two AC amplifiers can be arranged to have -3dB high-pass cutoff frequency $f_{3dB} \approx 0.2\text{Hz}$, and 20dB amplification in the pass-band. The circuits are simulated by using general-purpose JFET opamps TL072, supplied by bipolar $\pm 15\text{V}$ DC voltage source. The results of the simulations are shown in Fig. 6.

Fig. 6. Frequency response of ABI and CLI amplifiers.

According to Fig. 6, it is obvious that the ABI circuit exhibits -40dB/dec high-pass roll-off, while the CLI yields only -20dB/dec. This is an important advantage for the ABI circuit.

C. Noise Performance

The ABI circuit has three bigger noise contributors. They are the noise of opamp U_1 , the noise of the high-ohmic resistor R_f and the noise of opamp U_2 . Each of them influences different bandwidths. The simulated noise gains are shown in Fig. 7. The U_2 noise is directly transferred to the output for low frequencies and DC. The noise gain of U_1 has peaking around the cutoff frequency. For higher frequencies, it is determined by the ratio of the capacitors C_s/C_f . The resistor R_f influences around the cutoff frequency. For low frequencies, its noise is canceled by U_2 , for higher frequencies by C_f .

Fig. 7. Noise gains for opamps U_1 , U_2 and resistor R_f .

(a)

(b)

Fig. 8. Integrated output noise. (a) $k=0$, $R_f=4\text{G}\Omega$, (b) $k=25$, $R_f=20\text{M}\Omega$

The integrated output noise for ABI and CLI amplifiers is shown in Fig. 8. When $k>0$ the integrated output noise of the ABI amplifier is slightly higher.

D. Transient Behavior

The transient behavior of the ABI circuit is simulated with the circuit of a current-to-voltage converter, shown in Fig. 9.

Fig. 9. Current-to-voltage converter built with an ABI.

For higher frequencies the output voltage is given theoretically by the following equation:

$$V_{out}(t) = -\frac{1}{R_s C_F} \int V_{in} dt \quad (24)$$

Fig. 10. Simulated pulse response of the circuit from Fig. 2 (c).

The ABI circuit was driven by a rectangular voltage with 2V peak-to-peak amplitude and 955.22Hz frequency. The value of the input resistor R_s is 8.2M Ω . The simulated output voltage is shown in Fig. 10. It is a triangular waveform with 319mV peak-to-peak amplitude. For opamp $V_{io}=3\text{mV}$, the simulated output offset voltage is $V_{oo}=3.011\text{mV}$.

V. EXPERIMENTAL RESULTS

A. Frequency Response

The ABI circuit has been tested experimentally in order to validate the theoretical formulas and the circuit itself. The circuit is implemented by using the component values which are described in the first item of the previous section. The TL072 opamp is used to assemble the circuit. It should be noted that the circuit is assembled on a Phenolic perforated prototype board.

Fig. 11. Measured frequency response compared with simulation.

The frequency response is measured by the circuit shown in Fig. 5. The ABI circuit was tested by sinusoidal signals with various frequencies. The measured frequency response is shown in Fig. 11. It is appended to the simulated one. The obtained results show a good agreement between experiment, theoretical analysis and PSpice simulation. It should be noted that the gain-bandwidth product of opamp TL072 is specified to 4MHz, according to the opamp datasheet.

B. Noise Performance

To evaluate the noise performance of the circuit, the noise floor of a grounded oscilloscope is compared with the observed noise at the ABI output, see Fig. 12.

Fig. 12. Measured noise. (a) observed noise of a grounded oscilloscope BW=20MHz, (b) observed noise at the ABI output BW=20MHz.

The noise floor of the oscilloscope is $V_{osc}=1.12\text{mV}_{pp}$. The measured noise at the ABI output is $V_m=1.28\text{mV}_{pp}$. The ABI peak-to-peak noise V_n can be roughly calculated by root-mean-square fashion, shown by (25):

$$V_n^2 + V_{osc}^2 = V_m^2 \quad (25)$$

Replacing the measured values for V_{osc} and V_m in (25), it can be calculated that the ABI noise is $V_n=0.62\text{mV}_{pp}$. Using a factor 6.6 sigma for peak-to-peak to rms noise conversion, it

can be calculated that the ABI rms noise is $V_n=94\mu V_{rms}$.

C. Transient Behavior

The ABI circuit has been tested by a rectangular signal generated by a function generator which is connected to the input of the circuit via $8.2M\Omega$ resistor, as is shown in Fig. 9. The input is square wave signal with 2V peak-to-peak amplitude and about 1kHz frequency. The applied input signal and the measured output voltage are shown in Fig. 13.

Fig. 13. Experimental pulse response of the circuit from Fig. 2 (c).

According to equation (24), the peak-to-peak value of the output voltage should be equal to 319mV which completely corresponds to the 320mV, obtained experimentally.

The measured output DC offset voltage of the ABI circuit is -6.5mV, while the DC offset voltage at the node V_F is equal to 154mV.

VI. CONCLUSION

Achieving low-frequency operation with conventional lossy integrators is difficult task because very high-ohmic resistors should be used. The needed resistors often are in the giga-ohm range, thus the used opamps should have very low input currents. To reduce the output offset voltage error requires the usage of special electrometer opamps with input currents in a femto-ampere range. These opamps are expensive and require special care in their implementation. From another side the high-ohmic resistors are not stable over time and lead to drift in the important circuit parameters and characteristics [4]. The presented ABI circuit overcomes all of these problems. It is built from on the shelf components and cancels the output offset voltage with popular general-purpose JFET or CMOS opamps. The proposed circuit is completely equivalent to the published version using three opamps [22]. Both circuits have the same frequency response, as their transfer functions are identical. The consequence is that the circuit with two opamps in the feedback could be successfully replaced by the new circuit which uses only one opamp in the feedback path. The following advantages of the presented circuit should be

pointed out:

- it is a simple and cost-effective solution utilizing only two general-purpose opamps
- the circuit is made from a small number of popular components; very high-ohmic resistors or special opamps are not needed
- acceptable low output offset voltage is achieved
- very low and well-defined high-pass cutoff frequency
- second-order high-pass roll-off
- stable transient behavior
- can benefit many applications where charge-to-voltage conversion is needed

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Emad Alnasser received the M.Sc. degree in Electrical Engineering from Iran University of Science and Technology (IUST), Iran, in 2007. He joined the Department of Electrical Engineering, Islamic Azad University of Abadan, Iran, as a Lecturer in 2008. He founded and established NouTronics Research and Development group which is active in the field of instrumentation and measurement by designing and manufacturing electronics instruments.

Dobromir P. Dobrev received the M.Sc. degree in Electronics and Microelectronics from the Technical University of Sofia in 1994, and the Ph.D. degree from the Centre of Biomedical Engineering at the Bulgarian Academy of Sciences, in 2000. Dr. Dobrev is an analog IC designer and has experience in the design of BJT and CMOS analog and mixed-signal integrated circuits, as well as in biosignal processing in medical electronics.

Tatyana D. Neycheva received the M.Sc. degree in Telecommunications from the Technical University of Sofia in 1995, and the Ph.D. degree from the Centre of Biomedical Engineering at the Bulgarian Academy of Sciences, in 2003. Dr. Neycheva has experience in the acquisition and digital filtration of biosignals, as well as in the firmware development and programming of embedded microprocessor systems.