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A Minimal Capacitor Modular Converter for Ultra-Dense Power Conversion

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Abstract

Modular multilevel power electronic converters are considered an increasingly critical family of converters for myriad high voltage high power applications. With the ever-growing emphasis on electrification of the economy, they play a crucial role in serving energy sources and loads whose electrical ratings go beyond the ratings of the conventional power electronic building blocks. In particular, modular multilevel converter (MMC) topology enjoy its dominance in such applications due to modularity, scalability, performance and fault-tolerance capability. However, the MMC topology design imposes low-frequency ac components on the module capacitors and thus is inhibited by the capacitor size. Capacitor sizing plays a significant role in the overall system's size, cost and reliability. This paper introduces a minimal capacitor module based topology for DC to three-phase AC conversion. The unique design feature of the module includes minimal capacitor requirement due to elimination of single-phase ac power processing requirements. Together with improved power density, reduction of capacitor size permits the use of only film capacitors thus eliminating the weakest link of the overall system. Along with the step-by-step analytical derivation of the proposed approach, the paper presents detailed simulation studies, comparative analysis and experimental results from a proof-of-concept laboratory-scale prototype.

Index Terms

Capacitor Sizing, Modular Converter, Topology.

I. INTRODUCTION

MODULAR multilevel power converters play a critical role to serve myriad applications where the electrical ratings of the sources and loads go beyond the ratings of the conventional building blocks of power converters. These class of converters provide a solution to serve several applications such as high-voltage DC conversion (HVDC) transmission systems, electric vehicle fast-charging stations, integration of battery energy storage systems, etc. where two-level converters cease to become practical. In addition to enabling many applications, other motivating factors to adopt multilevel topologies include

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improved waveform quality leading to reduced filter sizing, lower electromagnetic noise issues and, in some cases, improved fault-tolerant capabilities [1].

Multilevel topologies can be broadly classified into dc-stacked power converters and modular power converters. Although several dc-stacked topologies have been developed, neutral-point clamped and flying capacitor multilevel converters are the most studied and also commercialized [2], [3]. Due to increased complexity in control and commutation challenges arising from parasitics, these converters have not become commercially viable beyond three-level [2], [4], [5], [6]. There is continued research to address these challenges although with limited success.

In contrast to dc-stacked converters, modular multilevel converters (MMC) continue to enjoy their dominance beyond three-level conversion. Formed of series connection of several half-bridge or full-bridge modules, MMC can be scaled to countless number of levels without commutation issues [7]. Recent commercial MMC installations support 1GW, 320kV grid-scale applications [8]. Similar to other multilevel topologies, MMC enables ease of integration and improved fault-tolerance capability. However, MMC topology is inhibited by the capacitor size of the modules. Capacitor sizing plays a significant role in the overall system's size, cost and reliability. In order to limit the voltage ripple across the semiconductor devices of the modules and maintain converter operation, the capacitors are bulky [9]. The requirement of high capacitance values motivates the use of electrolytic capacitors. These electrolytic capacitors clearly dominate the overall system. Unfavorably, they are considered the weakest link of a power electronic system and significantly hurt the overall system reliability [10], [11].

There is continued research to address the capacitor sizing issues in MMC converters. Some efforts include capacitor size minimization by incorporating improved capacitor models and capacitor selection methods [12], [13]. Alternative studies propose advanced control structures for circulating current minimization to reduce the second-harmonic power oscillation to reduce capacitor size [14], [15]. Other similar approaches introduce methods to inject harmonics into the circulating current to reduce the module capacitance [16], [17], [18]. In [19], the authors derive the operating conditions which maximize the power transfer as a function of the energy storage. Unfortunately, the state-of-the-art methods still continue to use several *millifarads* of capacitors with MMC topology and these capacitors can occupy up-to 70% of the converter volume.

In contrast, this paper introduces a *minimal capacitor module* (MCM) structure which utilizes only a few *microfarads* of module capacitance. Several MCMs can be connected in series to form a DC-AC minimal

Fig. 1. Module Design in (a) State-of-the-art (b) Proposed: Minimal capacitor module.

capacitor modular converter (2MC). Together with improved power density, reduction of capacitor size permits the use of only film capacitors thus eliminating the weakest link of the overall system. The ultra-dense modular converter topology is proposed in Section II which details step-by-step converter derivation and analysis. The analytical results are supported by detailed simulation studies and experimental results of a laboratory-scale prototype in Section III-B and Section IV respectively. In Section III-A, the paper also presents results from a comparative study with MMC topology.

II. CONVERTER TOPOLOGY AND OPERATION

This section presents an innovative approach for high voltage power conversion while overcoming the challenges of the prevailing MMC topology. Details about the module structure along with its contrasting features with the state-of-the-art are provided in a step-by-step manner in the next subsection.

A. One-Phase Module Design

Figure 1a illustrates the conventional half-bridge module which forms the heart of the MMC topology. Considering the single-pole double-throw semiconductor switch, S in the figure, the switch throws are typically connected to *voltage stiff* nodes whereas the switch pole (labeled as p) is connected to a *current stiff* node. In classical approaches, the pole voltage v_p is referenced to one of the terminals of the voltage stiff node, in this case the negative terminal. In contrast, Figure 1b illustrates the proposed module design wherein the pole voltage v_p is referenced *differentially*.

With the assumption that switch state (defined by h) “1” refers to the pole connected to the throw as shown in the sub-figures and the switch state “0” connected to the other throw, the switch state tables

corresponding to the circuit are also shown in the figure. In the proposed module of Figure 1b, the operation of the switches S_1 and S_2 are synchronized. Hence, the switch state “1” (active state) and switch state “0” (zero state) result in pole voltages of V_{Cap} and zero respectively.

The conventional MMC topology utilizes series connected half-bridge modules of Figure 1a in order to derive the *arms* of the topology for the three AC phases. This paper proposes the use of the minimal capacitor half-bridge module of Figure 1b. The proposed module structure enables the integration of the three arms of the AC phases thereby enabling the use of minimal capacitors as energy storage elements within the modular topology. The key enabling feature of an *integrated arm* structure is the availability of a fully-differential connection. To elaborate, during zero-state, the output pole voltage is *fully* isolated from the module capacitor. In contrast, with the state-of-the-art module, the zero state requires the connection of the output pole to either the positive or the negative capacitor terminal, excluding the possibility for three-phase arm integration and capacitor size reduction. Further details are discussed in the remaining subsections.

B. DC-AC Converter Topology

Figure 2a illustrates the state-of-the-art modular multi-level converter topology for DC-AC power conversion. Each of the three-phase AC terminals are connected to the DC terminals via an arm comprising of series connected half-bridge modules of Figure 1a. In contrast, the half-bridge MCM modules of Figure 1b are employed to derive the proposed DC to three-phase AC modular multilevel topology as illustrated in Figure 2b. The highlighting feature of the topology is the *integrated arm* structure which is constructed using fully-differential module design discussed in the previous section.

The motivation of the proposed topology is derived from the bulky size of MMC module capacitors. Due to the topology design, each of the module capacitors of the six-arms have to process single-phase AC power individually. Hence, the capacitor size is defined by the AC power processing requirements and is bulky [12], [13], [14], [15], [16], [17], [18], [19]. On the other hand, the integrated arm structure exploits the fundamental idea that net power requirement of a three-phase AC system is constant. Hence, the integrated module design ensures that net processing power of the module capacitor is zero. This results in minimally sized module capacitor where the size is determined by factors such as switching frequency and current carrying requirements. In summary, the proposed topology eliminates the need of sizing the module capacitor per single-phase AC power requirements. A quantified analysis of this concept is presented in Section II-D. The next section presents a modulation strategy for the proposed topology.

Fig. 2. DC-AC Converter Topologies (a) State-of-the-art: Modular Multilevel Converter (MMC) (b) Proposed: Minimum Capacitor Modular Converter (2MC).

C. DC-AC Converter Operation

Similar to MMC, the electrical quantities of the terminals of the integrated module are stiff. Although the capacitor will be minimal, it will be sized to filter the high-frequency ripple content of the three-phase AC system. Hence, the conventional sine-triangle PWM modulation strategy can be adopted for the proposed topology [20]. Equation (1)-(2) characterize the duty ratios d_{k+} and d_{k-} of the top and the bottom integrated arm module switches respectively,

$$d_{k+} = \frac{0.5V_{dc} - v_k}{nV_{Cap}} = \underbrace{\frac{0.5V_{dc}}{nV_{Cap}}}_{d_{dc}} - \underbrace{\frac{\hat{V}_k \cos(\omega t - \phi_k)}{nV_{Cap}}}_{d_{ac}} \quad (1)$$

Fig. 3. Three-phase minimal capacitor module (MCM) with the proposed half-bridge configuration.

$$d_{k-} = \frac{0.5V_{dc} + v_k}{nV_{Cap}} = \underbrace{\frac{0.5V_{dc}}{nV_{Cap}}}_{d_{dc}} + \underbrace{\frac{\hat{V}_k \cos(\omega t - \phi_k)}{nV_{Cap}}}_{d_{ac}} \quad (2)$$

where, V_{dc} represents the DC voltage, n represents the number of integrated modules, v_k represents the instantaneous AC voltage (and $k = A, B, C$), $\hat{V}_k$ represents the peak AC voltage, ϕ_k represents the phase angle of the three AC phases ($0, 2\pi/3, 4\pi/3$) and V_{Cap} represents the module capacitor voltage. Other modulation strategies such as space-vector modulation may be adopted in the future to improve the DC bus voltage utilization.

D. Capacitor Sizing

The advantages of the proposed half-bridge module are readily observed with three-phase ac systems, as discussed further using Figure 3.

MMC topologies utilize series connected half-bridge circuit modules where each of the three-phases utilize their own modules with separate capacitors, as shown in Figure 1a. Hence, it may be observed that each of the phase module capacitors have to process single-phase power for the three phases *individually*. In fact, the total capacitance requirement has to meet the power processing capability of three single-phase ac systems. This is characterized using Equations (3)-(5) as discussed.

Considering one module of the arm formed by half-bridge modules, the average current through the module capacitors ($i_{C_{k+}}$) can be characterized using the duty ratios as expressed in (3). Hence,

$$\langle i_{C_{k+}} \rangle = d_{k+} \times i_{arm-k+} \quad (3)$$

where,

$$i_{arm-k+} = \frac{I_{dc}}{3} + \frac{i_k}{2} \quad (4)$$

and, d_{k+} and i_{arm-k+} represent the duty ratio and the current of the arm between the positive dc rail and one of the phases of the ac system respectively. Here, d_k is characterized in Equation (1) and Equation (4). Please note that v_k, i_k represent the voltages and currents of the three-ac phases respectively. Substituting the d_{k+} and i_{arm-k+} expressions into (1),

$$\Rightarrow \langle i_{C_k} \rangle = \frac{1}{nV_{Cap}} \left(\underbrace{\frac{V_{dc}I_{dc}}{6}}_{\text{dc term}} - \underbrace{\frac{v_k i_k}{2}}_{\omega^2 \text{ term}} + \underbrace{\frac{V_{dc}i_k}{4}}_{\omega \text{ term}} - \underbrace{\frac{v_k I_{dc}}{3}}_{\omega \text{ term}} \right) \quad (5)$$

where, ω represents the ac frequency of the three-phase system. It can be observed that the MMC approach imposes low-frequency ac currents into the dc module capacitors due to which the dc capacitances are voluminous for high-performance operation.

In contrast, the proposed half-bridge module has been designed to inherently enable an integrated module structure due to *differentially* connected pole voltages, as shown in Figure 1b. Integration of the three ac phases to a common capacitor eliminates the need of single-phase ac power processing requirements of the three phases. In fact, under balanced three-phase ac systems, $i_A + i_B + i_C = 0$. Hence, the net ac power processing requirements of the module capacitor C_{ABC} , are ideally *zero*. This results in minimally sized energy storage elements, capacitors in this case. This is characterized using equations (6)-(7) as discussed further.

$$\langle i_{C_{ABC+}} \rangle = d_{A+} \times \underbrace{\left(\frac{I_{dc}}{3} + \frac{i_A}{2} \right)}_{i_{arm-A+}} + d_{B+} \times \underbrace{\left(\frac{I_{dc}}{3} + \frac{i_B}{2} \right)}_{i_{arm-B+}} + d_{C+} \times \underbrace{\left(\frac{I_{dc}}{3} + \frac{i_C}{2} \right)}_{i_{arm-C+}} \quad (6)$$

Please note that the dc module capacitor current with the proposed approach features phase currents of the three ac phases. Substituting the d_{k+} expression into (6),

$$\Rightarrow \langle i_{C_{ABC+}} \rangle = \frac{1}{nV_{Cap}} \left(\underbrace{\frac{V_{dc}I_{dc}}{2} - \frac{v_A i_A + v_B i_B + v_C i_C}{2}}_{\text{zero per } T_{SW}} + V_{dc} \underbrace{\frac{i_A + i_B + i_C}{4}}_{\text{zero per } T_{SW}} - I_{dc} \underbrace{\frac{v_A + v_B + v_C}{3}}_{\text{zero per } T_{SW}} \right) \quad (7)$$

Under balanced three-phase ac systems, the sum of the three-phase voltages and currents are zero. Hence,

it may be concluded that the average dc module capacitor current per switching cycle is ideally *zero*. This results in minimally sized module capacitors. In conclusion, the proposed topology is designed to have minimal capacitance requirements and is appropriately titled as *minimal capacitor modular converter* (2MC). As in the case of MMC, the 2MC topology could use half-bridge or full-bridge modules based on dc and ac design specifications. This paper demonstrates the results using half-bridge modules. The simulation and experimental results confirm the analysis.

III. DESIGN ANALYSIS AND COMPARATIVE STUDY

This section derives the design equations for a DC-AC 2MC converter formed by series connected MCMs of Figure 2b. The design equations are subsequently utilized to compare the proposed approach with the state-of-the-art MMC topology using a design example.

A. Design Analysis

In addition to requiring lesser number of capacitors, the 2MC inverter topology needs lesser capacitance for the same per-unit (p.u.) power conversion. This enables the use of film capacitors as compared to electrolytic capacitors which are typically used in MMC topology due to the voluminous capacitance requirements. Hence, the 2MC inverter can be expected to have much higher lifespan as compared to MMC converters (since typically electrolytic capacitors are the bottleneck of a converter lifetime) as quantified next.

1) *Total Capacitance Requirement*: In 2MC inverter topology, the size of the integrated module capacitors will be a function of factors such as the switching frequency, voltage and current ratings imposed by the DC and AC systems, modulation technique and the number of modules. This section presents the capacitor size equation based on the simplified sine-PWM modulation technique discussed in Section II-C.

The top plot of Figure 4 illustrates example duty ratio waveforms of the top integrated arm switches for the three phases over one AC frequency cycle ($T_p = 1/f_p$). The bottom plot of the figure illustrates the switching functions over one switching cycle ($T_{SW} = 1/f_{SW}$) for the highlighted window of the duty ratios of the top plot. The selected window is for illustration purposes only and the analysis holds true for any instant of operation. The switching functions utilize symmetrical PWM output with triangular carrier waveform.

Fig. 4. Example duty ratio and switching function waveforms.

Based on the modulation strategy, the typical capacitor waveform over one switching cycle will feature distinct charge and discharge patterns based on the currents imposed by the three-phases in the integrated arm and the switching functions. The capacitor equation characterizing the voltage rise due to current flow can be quantified using $Cdv/dt = i$ (in (8)) and is illustrated for the time period $d_{ABC+}T_{SW}$. Here, $d_{ABC+}T_{SW}$ refers to the time window when all three-phases are connected to the capacitor.

$$\Delta v_{Cap}(t) = \frac{d_{ABC+} \sum_k^{A,B,C} i_{k+}}{C \times f_{SW}} \quad (8)$$

Based on Equation (4), it may be observed that the sum of the currents will be the dc current value I_{dc} . Hence, the interval $d_{ABC+}T_{SW}$ will be a charge interval for the capacitor. During the remaining intervals of the switching function, the current will be a function of the dc current and an ac current and may be a charge or a discharge interval. The charge rate will be maximum during the d_{ABC+} interval due to peak current input. The capacitor voltage rise due to the remaining intervals can be ignored, assuming unity power factor operation, since the current value will be much smaller. Equation (9) characterizes maximum dc voltage ripple.

$$\Delta v_{Cap-max} = \frac{I_{dc} \times \max[d_{ABC+}]}{C \times f_{SW}} \quad (9)$$

where, the maximum value of d_{ABC+} can be calculated using Equation (10) and is also annotated in

Figure 4.

$$\max[d_{ABC+}] = \frac{0.5V_{dc} - \hat{V}_k \cos \frac{\pi}{3}}{nV_{Cap}} \quad (10)$$

Finally, by substituting Equation (10) into Equation (9), Equation ((11)) quantifies the minimum capacitor size requirement for a voltage ripple specification r (in per units).

$$C = \frac{I_{dc} \times (V_{dc} - \hat{V}_k)}{2 \times n \times f_{SW} \times r \times V_{Cap}^2} \quad (11)$$

It may clearly be observed that the capacitor does not have to sized to process single-phase ac power. In contrast, the capacitor size is a strong function of switching frequency. Increasing the switching frequency results in dramatic reductions in capacitor size which is not feasible solution in the conventional MMC topology. Nevertheless, 2MC inverter does not require the use of high switching frequency. Moderate switching frequency will still result in dramatic capacitor size reductions since the per switching cycle average capacitor current is zero. Similar to MMC topology, 2MC inverter is a function of the DC current and voltage, AC voltage and the number of modules.

2) *Capacitor Lifetime Calculations:* Electrolytic capacitors are the weakest link in the overall power electronic system design [10], [11]. Due to reduced capacitance requirements, film capacitors can be sufficient to realize the converter design. Replacement of electrolytic technology with film technology is expected to bring lifetime improvement by at-least 1.5 orders of magnitude as derived using capacitor manufacturers' recommendations [21], [22], [23], [24]. The typical lifetime calculation equations are given by Equation (12) and Equation (13) for electrolytic and film capacitors respectively.

$$L_{op-elec} = L_{b-elec} \times k_{derating} \approx 8000 \times 1.3 \quad (12)$$

$$L_{op-film} = L_{b-film} \times \left[\frac{V_r}{V_{op}}\right]^7 \approx 10^5 \times \left[\frac{1}{0.8}\right]^7 \quad (13)$$

The first order of magnitude improvement results from base operating life of electrolytic versus film capacitors which is 8,000 hours versus 100,000 hours respectively. The second order of magnitude improvement is expected from the voltage de-rating factor. A typical safety factor margin in voltage rating of 20% is assumed irrespective of the use of capacitor technology. In the case of electrolytic

Fig. 5. Switch realization of the proposed half-bridge minimal capacitor module (MCM) with MOSFETs.

TABLE I
CONDUCTING AND BLOCKING DEVICES IN THE MCM HALF-BRIDGE CONFIGURATION

$h(t)$	Pole Voltage v_P	Conducting Device(s)		Blocking Device(s)
1	$+V_{Cap}$	Q_1, Q_2	$i_P > 0 \rightarrow T_1, T_2$ $i_P < 0 \rightarrow D_1, D_2$	T_0
0	0	Q_0	$i_P > 0 \rightarrow D_0$ $i_P < 0 \rightarrow T_0$	T_1, T_2

capacitors the voltage de-rating factor is typically <1.3 and is based on the safety margin. On the other hand, in the case of film capacitor technology, the voltage de-rating factor has a stronger influence on the film capacitor lifetime.

3) *Number of Silicon Devices*: The half-bridge module of Figure 1b can be realized using three power semiconductor switches as illustrated in Figure 5. Switch S_1 is realized using MOSFETs Q_1 and Q_0 and switch S_2 is realized using MOSFETs Q_2 and Q_0 . It may be noted that the zero state of the switches use a shared transistor i.e., Q_0 . Table I details the conducting devices based on the current direction of the pole current, i_P . Here, each device may use either the transistor's body diode or an external diode, referred to as D_z in the table, where $z = 0, 1, 2$. Equation (14) quantifies the total number of silicon semiconductor devices (N_{Si}) for the 2MC DC-AC topology,

$$N_{Si} = 2 \times n \times p \times 3 \implies N_{Si} = 18n \quad \text{when, } p = 3 \quad (14)$$

where, n refers to the number of modules per integrated arm, p refers to the number of phases of the AC system. The factor of 2 includes the devices in the top and the bottom integrated arms. The factor of 3 indicates the number of distinct devices per module per phase, also illustrated in Figure 5. Due to the unique design structure of the module, the 2MC inverter topology has higher number of silicon devices as a trade-off. However, the total VA (voltage $\times$ current) rating of the silicon devices is equivalent to MMC converters for half-bridge configuration and is discussed in the next subsection.

4) *VA Rating of Silicon Devices:* The voltage $\times$ current rating (VA) of the silicon devices play a critical role in determining the cost of the silicon devices. Table I highlights the state of the three devices based on the switching state of the half-bridge. Similar to the MMC topology, the current and the voltage rating of the silicon devices are determined the arm current and the module capacitor voltage respectively. In contrast to MMC topology, during the zero-state, devices T_1 and T_2 share the blocking module capacitor voltage. In totality, the total VA (voltage $\times$ current) rating of the silicon devices is equivalent to MMC converters for half-bridge configuration and is quantified in Equation 15,

$$VA_{per-phase} = \underbrace{V_{pu} \times A_{pu}}_{Q_0} + \underbrace{2 \times (0.5 \times V_{pu}) \times A_{pu}}_{Q_1, Q_2} = 2V_{pu}A_{pu} \quad (15)$$

where, $VA_{per-phase}$ refers to the VA rating of the per-phase half-bridge MCM module and V_{pu}, A_{pu} refer to the per-unitized voltage and current ratings respectively. The second term in the equation highlights the factor of half in the voltage rating of the two devices Q_1 and Q_2 . In order to ensure equal voltage sharing between Q_1 and Q_2 , voltage balancing technique may need to be adopted. Trade-offs exist between adding circuit complexity versus employing higher rated devices and the design implementation will depend on application specifications. Several voltage sharing schemes exist in the literature [25], [26] and are not discussed in this paper.

B. Simulation Results with Comparative Study

In order to verify the feasibility of the 2MC topology, a design example is considered for simulation results and comparative studies. Table II details the parameter list of a 8.5kV dc to 4.16kV three-phase 60Hz ac power converter. The 2MC converter design features 10 integrated MCM modules per an integrated arm with per-module dc voltage of 0.85kV. The module capacitance value is $10\mu F$ which limits the ripple voltage to within 20%. To emphasize, this capacitance is shared amongst the three phases.

TABLE II
PARAMETERS OF THE SIMULATED DC-AC DESIGN EXAMPLE

Design Variable	State-of-the-art: MMC	Proposed: 2MC
Power	1MW	
DC Voltage	8.5kV	
AC Voltage	4.16kV 3-Phase 60Hz	
Number of Levels	10	
Switching Frequency	20kHz	
Capacitance per module	$2mF$	$10\mu F$
Total Capacitance	$120mF$	$200\mu F$

TABLE III
PRELIMINARY COMPARISON RESULTS

Design Variable	State-of-the-art: MMC	Proposed: 2MC
Total Capacitance	$120mF (\times 600)$	$200\mu F$
Lifetime of capacitors*	Electrolytic: 20,000 hours	Film: 100,000 hours
Number of Silicon Devices	1 p.u.	1.5 p.u.
Voltage× Current of Silicon Devices	Equal	
*Base operating life		

On the other hand, an MMC converter design would require $2mF$ of capacitance per-phase to maintain the same ripple voltage.

Results from a simulation using PLECS platform is illustrated in Figure 6 where the voltages and currents are per-unitized over the respective DC variables. Figure 6a and Figure 6b illustrate some waveforms with MMC and 2MC topology, respectively for comparison. The simulation utilizes a simplified control sine-PWM control scheme as discussed in Section II-C wherein the duty ratios of the modules per-phase are synchronized and are illustrated by the top traces of Figure 6. The next two rows illustrate the dc and three-phase ac voltages and currents. The high quality of the output waveforms are readily observed for the two cases.

Next, dc module capacitor voltages and currents are plotted. With a d_{dc} of 50% and $n=10$, the DC module capacitors operate at 0.1p.u. The low voltage ripple of $\approx 5\%$ in-spite of a tiny DC capacitor of $3\mu F$ is readily observed. The contrasting features of the two topologies can be observed from these two waveforms. In both cases, the module capacitors are designed to have the same peak-peak ripple voltage of 20%. The module capacitor voltage and current waveforms feature low-frequency ripple in both cases. However, the MCM capacitor witnesses switching frequency ripple due to the integrated arm

Fig. 6. Simulation Results (a) State-of-the-art: Modular Multi-Level Converter (b) Proposed: Minimum Capacitor Modular Converter (2MC).

structure. Unique to the case of MCM, the capacitor size can be reduced further by increasing the switching frequency of the converter. Lastly, the average value of the module capacitor current taken per switching cycle is plotted in the bottom-most plot in order to highlight that the MCM current value approaches to zero in the absence of single-phase ac power processing requirements. Other the other hand, the MMC module capacitors have to filter the low-frequency content as illustrated in the waveform. To reiterate, while the MMC topology utilizes a total of $120mF$ capacitance per converter, the 2MC only requires $200\mu F$ to maintain the same ripple voltage. Table III summarizes the comparative analysis based on the design equations derived in Section III-A.

IV. EXPERIMENTAL RESULTS

In order to verify the proposed approach, results from a hardware based experimental prototype have been captured and presented in this section. Figure 7 shows the proof-of-concept scale laboratory working prototype for the DC-AC 2MC converter. The prototype is designed to be highly modular where one

Fig. 7. A photograph of the hardware prototype.

Fig. 8. Volume share in the laboratory prototype

printed circuit board (PCB) hosts a single-phase module. Three PCBs are stacked vertically to form a three-phase integrated module of Figure 3. The prototype consists of two modules per integrated arm.

Each PCB hosts a single DC film capacitor of $1\mu F$ (part number: Kemet-R75GI410050H0J). Hence, one three-phase MCM module consists of *only* $3\mu F$ of capacitance. The switches of Figure 5 are realized using 150V, 21A, $53m\Omega$ MOSFETs with part number of Infineon-IPD530N15N3GATMA1. Figure 8 illustrates the volume share of the electronic components in the laboratory-scale prototype. The tiny film capacitors in the proposed 2MC topology share significantly lower overall volume versus state-of-the-art where capacitors can occupy up-to significant converter volume [12], [19].

Figure 9 illustrates the experimental waveforms. The operating parameters are as follows: power throughput: 150W, DC voltage: 75V, dc duty ratio d_{dc} of 50%, peak ac duty ratio $\hat{d}_{ac}$ of 40% and switching frequency f_{SW} of 20kHz. Figure 9a shows results over a few low-frequency 60Hz ac output where the

Fig. 9. Experimental Results (a) Input dc current, Capacitor voltages of two modules from the top and the bottom arm and three-phase currents over a few 60Hz cycles (b) Switching function and the drain-source voltages of switches of one module over a few switching frequency cycles of 20kHz.

voltages and currents are per-unitized over the respective DC variables. The top plot illustrates the dc input current with mean value of 1p.u. The middle plot illustrates the DC module capacitor voltage for one of the top and the bottom arm modules. With a d_{dc} of 50% and $n=2$, the DC module capacitors operate at 0.5p.u. The low voltage ripple of $\approx 5\%$ in-spice of a tiny DC capacitor of $3\mu F$ is readily observed. The high quality of the three-phase output current can be observed in the bottom plot of the figure.

Figure 9b shows results over a few high-frequency switching cycles of 20kHz for one module of the top arm. The top plot illustrates the synchronized gate drive control signals for the top and the bottom switches (Q_1 and Q_2) of the module. The middle switch (Q_0) is driven by a complimentary signal (not shown). The next three plots illustrate the per-unitized drain to source voltage of Q_1 , Q_2 and Q_0 respectively. Q_1 and Q_2 operate synchronously and equally share the blocking voltage imposed by the DC module. Switch Q_0 shares the entire DC module capacitor voltage.

V. CONCLUSION

State-of-the-art MMC topology enjoys its dominance beyond three-level conversion. However, due to the topology design, the module capacitors are sized to process low-frequency single-phase ac power. The requirement of high capacitance values motivates the use of bulky electrolytic capacitors which have a

detrimental effect of the overall system's power density and reliability. While there is continued research to address the capacitor sizing issue, the state-of-the-art methods continue to use several *millifarads* of capacitors and these capacitors can occupy up-to 70% of the converter volume.

This paper presents an innovative approach for high voltage power conversion while overcoming the challenges of the prevailing MMC topology. The proposed DC to three-phase AC topology utilizes an integrated arm structure and exploits the fundamental idea that net power requirement of a three-phase AC system is constant. Hence, the module capacitor can be sized *minimally* where the capacitors can be only a few *microfarads*. A quantified analysis of this topology is discussed along with simulation and comparative studies. Results from a design example indicate that the proposed topology utilizes only $200\mu F$ of capacitance (versus $120mF$ in the case of MMC). Elimination of bulky capacitance requirements permits the use of film capacitors (instead of electrolytic capacitors) with at-least an order of magnitude lifetime improvement. As a trade-off, the proposed topology uses 1.5 times the number of silicon devices. However, in totality, the total VA rating of the silicon devices is equivalent to MMC converters. Results from a proof-of-concept laboratory scale prototype are also presented and verify the analytical results.

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