A Photogenerated Silicon Plasma Waveguide Switch and Variable Attenuator for Millimeter-Wave Applications

Thomas R. Jones, *Member, IEEE*, Alden Fisher, *Graduate Student Member, IEEE*
Douglas W. Barlage, *Senior Member, IEEE* and Dimitrios Peroulis, *Fellow, IEEE*

Abstract—This paper reports the design, fabrication, and measurement of a millimeter-wave solid-state π -match waveguide switch using bulk silicon micromachining. A photogenerated plasma within a silicon post is utilized as the switching element within the waveguide channel. Not only does this isolate the switch bias network from the RF signal path, but allows for tuning of the OFF-state isolation with increasing optical power for application as a variable attenuator. A measured OFF-state isolation greater than 25 dB up to 40 GHz is reported, with a measured extracted ON-state insertion loss of 0.52 dB at 35 GHz, and less than 0.88 dB across the entire band from 30–40 GHz. The proposed switch illustrates the significant potential for photogenerated silicon plasma switching of high-performance bulk micromachined millimeter-wave waveguides.

Index Terms—Waveguide, switch, photogenerated solid-state plasma, millimeter-wave, silicon micromachining, deep reactive ion etching (DRIE).

I. INTRODUCTION

MILLIMETER-WAVE switches are fundamental components of modern transceiver architectures, enabling a variety of functionality including signal routing, redundancy switching, band selection, and phase shifting. In particular, waveguide switches are typically chosen at millimeter-wave (mm-wave) frequencies and beyond due to their low insertion loss and high power handling [1]. A number of technologies for the switching element inside a waveguide have been developed, including electromechanical rotors and PIN diode switches [2]–[5], and RF MEMS and microfluidic-based switches [6]–[11]. However, most of these approaches use traditional metal-machined waveguides, thus are large, heavy, and difficult to integrate with planar microwave technology and on chip. While an integrated waveguide switch using RF MEMS was proposed in [7], self-actuation, reliability, and stiction issues limit its use for high power applications.

The optical control of microwave and mm-wave signals by photogeneration of solid-state plasma has shown promise as a high-performance switching and phase shifting technology in both planar, waveguide, and substrate integrated waveguide (SIW) technologies [12]–[14]. Not only is the bias network of the optical source isolated from the RF signal, the plasma element itself offers advantages including high power handling

with low insertion loss [15], high linearity [16], and fast switching times [17]. Applications in the literature include switches, variable attenuators, and tunable phase shifters, [13], [18], [19].

While photogenerated solid-state plasma elements have been successfully integrated into rectangular waveguide and SIW technologies, the integration and measurement of a solid-state plasma switch inside a silicon micromachined waveguide channel at mm-wave frequencies has not yet been reported. Silicon bulk micromachining technology offers benefits including high precision with micrometer tolerances, low insertion loss, and high power handling up to sub-mm-wave bands and beyond, along with excellent integration with planar technologies [20], [21]. Furthermore, silicon micromachining technology enables the fabrication of both the solid-state plasma element and the waveguide channel with the same process for complete monolithic integration.

The main objective of this paper is to explore the use of photogenerated plasma as switching elements located inside silicon micromachined waveguides for operation as shunt-based microwave switches at mm-wave frequencies. To the best of the authors' knowledge, this is the first measured implementation of its kind, and highlights the significant potential of this technology for high performance mm-wave switching applications.

The paper is organized as follows. First, section II details the principle of operation of the photogenerated silicon plasma waveguide switch, with a simplified theoretical formulation to relate the applied optical power to the photogenerated conductivity of the silicon plasma. Next, in section III, the design procedure of a π -match waveguide switch using silicon plasma elements is detailed, with a description of the fabrication process flow using silicon bulk micromachining presented in section IV. The experimental results of the fabricated prototype are then presented in section V, along with an analysis validating the theory derived in section II with measurement, and a discussion on the application of the waveguide switch as a variable attenuator. A comparison between state-of-the-art millimeter-wave waveguide switches is presented in section VI, and final conclusions are then drawn.

II. PRINCIPLE OF OPERATION

A. Fundamental Concept

In Fig. 1(a), the fundamental concept behind the proposed photogenerated solid-state plasma waveguide switch is illus-

T. R. Jones and D. W. Barlage are with the Department of Electrical and Computer Engineering, University of Alberta, AB, Canada, T6G1H9 e-mail: trjones@ualberta.ca.

A. Fisher and D. Peroulis are with Purdue University, IN, USA.

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Fig. 1. (a) Conceptual waveguide switch 3D layout, and (b) cross sectional view A'-A' of the rectangular waveguide loaded with a semiconductor post for operation as a photogenerated solid-state plasma waveguide switch and variable attenuator, with HFSS simulations of the (c) ON-state, and (d) OFF-state with increasing optical power.

trated. A semiconductor post is placed within a rectangular waveguide channel in a shunt configuration, connected from the top of the waveguide to the bottom. The post is ideally located near the center due to the peak of the fundamental $TE_{1,0}$ mode. As shown in Fig. 1(b), a small opening in the top of the waveguide allows photons from a light source with high enough energy to absorb into the semiconductor post, generating free carriers within. The semiconductor post is therefore changed from a capacitive to a conductive load, allowing for the transmission or reflection of mm-waves within the waveguide channel, respectively.

The result of increasing the conductivity of the semiconductor post inside a waveguide channel as illustrated in Fig. 1(a) is simulated in HFSS. A waveguide with broad and narrow wall dimensions of 7.112 mm and 200 μm , respectively, is chosen for operation within the Ka-band. The waveguide is loaded in the center with a semiconductor post of radius 200 μm and dielectric constant $\epsilon_r = 11.9$. The choice of reduced height waveguide is to allow the photo-excited plasma to extend the total height of the post H . The choice of permittivity matches that of silicon, a commonly available semiconductor, while the choice of post radius is due to the available optical fiber size for plasma excitation at the time of this work. More specific discussions on the choice of these values are presented below and in section III.

In Fig. 1(c), the ON-state scattering parameters with no optical excitation are shown, where the semiconductor is modeled as a dielectric element. Here the switch is in the transmission mode, with low insertion loss. Improving the ON-state return loss is discussed in section III.

In Fig. 1(d), the OFF-state of the switch is shown, whereby increasing the optical power incident on the top of the post

increases the amount of isolation realized by the switch. Here, the post is modeled in HFSS as a lossy dielectric with a specified conductivity, and a maximum isolation is reached at a conductivity between 350 - 400 S/m. Further increasing the conductivity improves the total system loss, i.e., more waves are reflected instead of dissipated in the post. This effect, and methods to improve the isolation, are discussed further in section V and section III, respectively.

From this simple proof of principle, clearly the primary goal is to maximize the amount of on/off ratio versus optical energy on the post. Therefore, a material with good semi-insulating properties to drive the ON-state, and optical excitation properties to drive the OFF-state, is desired. Two such materials which have been explored in the literature for optical switches are high resistivity intrinsic silicon and germanium [22]. Both offer long carrier lifetimes due to their indirect bandgaps, enabling higher conductivity at lower optical energies for the OFF-state. However, germanium generally has poorer semi-insulating properties than silicon for the ON-state insertion loss [23], as well as less availability for purchasing high quality substrates. Therefore, due to long carrier lifetimes, reasonable resistivities, greater availability of high insulating substrates at low cost, along with well developed bulk micromachining processes, high resistivity ($>10 \text{ k}\Omega\text{cm}$) intrinsic silicon was determined to be the most reasonable choice for the present work, and will be referred to going forward.

B. Photoconductivity Model

To quantify the relationship between the optical power incident on the top surface of the silicon post and the photogenerated conductivity and permittivity within the bulk, a theoretical analysis is now developed. This will allow for a quick and accurate calculation for the silicon plasma design parameters to be used in a 3D full-wave simulation tool such as HFSS. Validation of the analysis is presented in section V, where an excellent match between the theory developed here and the experimental results of the waveguide switch is shown.

When light is incident on the surface of silicon with photon energy $h\nu$ greater than the bandgap ($E_g = 1.12 \text{ eV}$), electron-hole pairs are generated within the bulk, and the silicon enters a non-equilibrium state. The carrier concentrations within the silicon are then expressed as

$$n = n_0 + n' \quad (1)$$

$$p = p_0 + p' \quad (2)$$

where n , p are the total, n_0 , p_0 the intrinsic, and n' , p' the photogenerated excess concentrations of electrons and holes, respectively. For high-carrier injection, the typical case for the present application, $n' \gg n_0$ and $p' \gg p_0$. Furthermore, the number of photogenerated electrons and holes are equal, such that $n' = p'$.

In order to simplify the analysis, the silicon is treated as a bulk volume in which a steady flux of photons ϕ_{opt} at optical wavelength λ_{opt} incident on the top of the post generates a uniform carrier concentration throughout. This is a reasonable assumption if the depth of the post H is larger than the absorption depth $1/\alpha$ [24], where the absorption coefficient α

can be calculated from $\alpha = 4\pi\kappa_s/\lambda_{opt}$, with κ_s the imaginary part of the complex refractive index ($n_r = n_s - j\kappa_s$) at λ_{opt} [24]. Given the optical source shown in Fig. 1(a) with a wavelength $\lambda_{opt} = 915$ nm and $\kappa_s = 1.894 \times 10^{-3}$ [25], the calculated absorption coefficient $\alpha = 250$ cm⁻¹. Thus, at a depth of $H = 200$ μ m, 99.4% of the photon flux is absorbed by the silicon. It is then reasonable to expect the carriers to diffuse throughout the enclosed volume of the post within a time scale based on the thermal velocity $v_{th} = \sqrt{3kT/m^*}$, where k is the Boltzmann constant, T the ambient temperature, and m^* the effective mass, creating a uniform carrier concentration throughout.

Considering the 1D case where the top of the silicon post shown in Fig. 1 is uniformly illuminated by light, with variation of the photon flux density only in the $\hat{y}$ direction, the steady-state generation (G_e) and recombination (R_e) rates of the electron-hole pairs can then expressed by the following relationships [24]

$$G_e = \frac{\eta\phi_{opt}(y)}{H} \quad (3)$$

$$R_e = \frac{n'}{\tau(n')} \quad (4)$$

$$G_e = R_e. \quad (5)$$

Here, $\tau(n')$ is the carrier lifetime as a function of carrier concentration, and η the quantum efficiency (number of electron-hole pairs generated per photon).

Considering an optimal efficiency ($\eta = 1$), the photon flux density can be expressed as [24]

$$\phi_{opt}(y) = P_{opt}(y)/h\nu \quad (6)$$

where the power intensity P_{opt} is determined from [24]

$$P_{opt}(y) = P_0(1 - R)e^{-\alpha y} \quad (7)$$

with $P_0 = P/A$ the incident light intensity on the surface of the silicon, P the incident optical power, $A = \pi d^2$ the surface area of the top of the post with diameter d , and $R = \{(1 - n_s)^2 + \kappa_s^2\}/\{(1 + n_s)^2 + \kappa_s^2\}$ the reflection coefficient at the silicon interface with normal incidence. Therefore, based on the earlier assumption of a uniform carrier concentration throughout the silicon post, the average power intensity absorbed into the post can be calculated as

$$\overline{P_{opt}} = \frac{1}{H} \int_0^H P_{opt}(y) dy = \frac{P_0}{\alpha H} (1 - R)(1 - e^{-\alpha H}) \quad (8)$$

and the uniform carrier concentration throughout the post can be determined from

$$n' = \frac{P_0/h\nu}{\alpha H^2} \tau(n')(1 - R)(1 - e^{-\alpha H}) \quad (9)$$

With respect to (9), the carrier concentration is proportional to the incident optical power intensity, the carrier lifetime, and one minus the reflection coefficient. To improve the number of carriers generated, the reflected power can be decreased by depositing anti-reflection coatings (ARC) on the surface of the silicon. Furthermore, the optical power intensity can be increased. However, it is well known that the carrier lifetime begins to rapidly decrease at higher carrier concentrations

($\sim 10^{16-17}$ cm⁻³ [23]) primarily due to Auger recombination [24], [26]. To model this effect, the following equation is used to represent the carrier lifetime as a function of carrier concentration [27]

$$\tau(n') = \frac{\tau_0}{1 + (n'/N_0^{ref})^{3/2}} \quad (10)$$

where τ_0 and N_0^{ref} are fitting coefficients. Thus, the most important parameter to consider when designing for the maximum on/off ratio of the post is the carrier lifetime, which is largely related to the quality, or maximum resistivity, of the intrinsic silicon material. Typical values for τ_0 and N_0^{ref} in the literature are 0.1 – 1000 μ s and $10^{15} - 10^{17}$ cm⁻³, respectively [26], [27].

With the carrier concentration now known, the DC photoconductivity of the silicon post can be determined from [24]

$$\sigma_{DC} = q(\mu_n + \mu_p)n' \quad (11)$$

where μ_n , μ_p are the electron and hole drift mobilities, respectively, and q is the unit charge of an electron. Thus, the contribution to the total DC photoconductivity from electrons and holes adds in parallel. Furthermore, the drift mobilities are themselves functions of carrier concentration, and can be calculated for a given n' using the following [28]

$$\mu_n = \frac{1318}{1 + (n'/1 \times 10^{17})^{0.85}} + 92 \quad (12)$$

$$\mu_p = \frac{420}{1 + (n'/1.6 \times 10^{17})^{0.7}} + 50 \quad (13)$$

As free carriers are generated in the silicon bulk, along with the change in conductivity, a change in the dielectric constant occurs. This effect can be modelled using the Drude response in terms of the intrinsic bulk complex conductivity of the silicon plasma given by [29], [30]

$$\sigma(\omega) = \frac{\sigma_{DC}}{1 - j\omega/\gamma_{n,p}} = \sigma'(\omega) - j\sigma''(\omega) \quad (14)$$

where $\gamma_{n,p} = (m_{n,p}^* \mu_{n,p}/q)^{-1}$ is the average collision rate, and $m_{n,p}^*$ the effective mass, of an electron or hole, respectively. Thus, the real and imaginary components of $\sigma(\omega)$ can be expressed as the following

$$\sigma'(\omega) = \frac{\sigma_{DC}}{1 + \omega^2/\gamma_{n,p}^2}, \quad \sigma''(\omega) = \frac{\sigma_{DC} * (\omega\gamma_{n,p}^{-1})}{1 + \omega^2/\gamma_{n,p}^2} \quad (15)$$

At operating frequencies below 100 GHz, $\gamma_{n,p} \gg \omega$, and the real component $\sigma'(\omega)$ is approximately equal to the DC photoconductivity σ_{DC} calculated in (11). Using the well known relationship between intrinsic bulk permittivity $\epsilon(\omega)$ and intrinsic complex conductivity $\sigma(\omega) = j\omega\epsilon(\omega)$, the effective dielectric constant $\epsilon_r(\omega)$ of the silicon plasma can be determined from the following [30]

$$\epsilon_r(\omega) = \epsilon_\infty - \sigma''(\omega)/\omega\epsilon_0 \quad (16)$$

where ϵ_∞ is the background dielectric constant for silicon (11.9, [24]), and ϵ_0 is the permittivity of free-space. Thus, to simulate the photo-excited silicon material in HFSS, the effective dielectric constant ϵ_r and DC photoconductivity σ_{DC} are entered into their respective material fields for relative permittivity and bulk conductivity [30].

Fig. 2. HFSS simulation results of the ON-state return loss and OFF-state isolation at 30 GHz versus silicon post radius for the waveguide switch model shown in Fig 1.

III. DESIGN

This section describes the design of a silicon plasma waveguide switch. Due to the high permittivity of the silicon post located within the waveguide channel shown in Fig. 1(a), the ON-state of the waveguide switch suffers large reflection losses caused by the large shunt capacitive loading of the post. Fig. 2 shows the effect on the ON-state return loss and OFF-state isolation versus the radius of the post for the waveguide switch in Fig. 1(a). By increasing the radius, more isolation is achieved at the expense of impedance matching, and vice versa. Increasing the number of posts in the transverse plane would have a similar effect. It is clear that a trade-off between ON-state return loss and OFF-state isolation must be made, thus maximizing the on/off ratio becomes difficult with such a switch configuration.

For a more optimal way to increase the on/off ratio for switches with high ON-state capacitance, a π -match switch topology can be chosen [31]. A high impedance section is inserted between two shunt switch elements to improve ON-state matching. The required characteristic impedance value Z_h of the high impedance section can be calculated from the following equation [31]

$$\tan(\beta l) = \frac{2\omega_0 C_u Z_h Z_0^2}{Z_h^2 - Z_0^2 + (\omega_0 C_u Z_h Z_0)^2} \quad (17)$$

where β is the propagation constant and l the propagation length of the high impedance waveguide section, Z_0 the characteristic impedance of the main waveguide section, and ω_0 the angular frequency at band center. To relate the waveguide height H_h and width W of the high impedance section to its characteristic impedance, the following power-current definition for an air-filled waveguides is used [32]

$$Z_h = \frac{465 H_h \lambda_g}{W \lambda} \quad (18)$$

where λ_g is the guided wavelength and λ the free-space wavelength at the band center frequency. Thus, the high impedance section can be formed by simply increasing the height of the waveguide section between the two shunt switches.

In Fig. 3, the final design layout including dimensions for microfabrication of the waveguide switch is shown. The

Fig. 3. π -design layout of the photogenerated silicon plasma waveguide switch showing (a) the top wafer underside with silicon posts and π -match network, and (b) top wafer flipped onto bottom wafer for bonding (units in μm).

Fig. 4. HFSS simulation results of the (a) ON-state and (b) OFF-state of the silicon plasma π -match waveguide switch shown in Fig. 3.

Fig. 5. (a) 3D layout of the CPW-to-waveguide feed network for characterization of the waveguide switch using high frequency probes (units in μm), and (b) HFSS simulation results of the transition.

prototype was chosen to operate within the Ka-band, with a total waveguide width of 7.112 mm (WR28). The design was limited to four silicon posts due to the availability of a 1×4 optical fiber splitter, with four individual fibers supplying the optical excitation. Therefore, to achieve greater than 20 dB OFF-state isolation, a 2-by-2 array of posts with 400 μm diameters was placed within the waveguide channel. A high impedance π -match section was designed in between the posts to improve ON-state impedance matching, while also decreasing the electrical length of the overall switch. The top wafer was then flipped and bonded to the bottom wafer, as

Fig. 6. Fabrication process flow for the waveguide switch.

shown in Fig. 3(b). Four optical fibers inserted into holes etched in the backside of the top wafer directly above the silicon posts provided optical excitation of the silicon plasma.

As discussed in section II, a longer carrier lifetime results in a silicon post with a higher conductivity. Thus, a high resistivity ($>10 \text{ k}\Omega\text{cm}$) intrinsic silicon wafer was chosen with a thickness of 675 μm to allow for the height of the high impedance section, and the backside etching of slots to align the fibers. The height of the waveguide channel was chosen to be 200 μm to allow for the silicon posts to have high enough conductivity for good isolation in the OFF-state, while also being large enough to limit conductor losses due to the reduced height waveguide in the ON-state.

In Fig. 4, the HFSS simulated results are plotted for the ON-state and OFF-state of the final prototype shown in Fig. 3. The ON-state return loss is above 20 dB from 27.6 GHz to 39.5 GHz, with a reflection zero at 33.1 GHz due to the π -match network. The OFF-state was simulated with a silicon post conductivity of 1000 S/m and dielectric constant $\epsilon_r = -2$, according to (16). The isolation is greater than 20 dB across the entire band up to 40 GHz.

In order to characterize the waveguide switch using high frequency RF probes, a coplanar waveguide (CPW)-to-waveguide feed network was designed, based on a current probe topology [33]. Fig. 5(a) shows the 3D layout of the CPW-to-waveguide transition. A CPW trace with 120 μm signal and 15 μm gap was designed for probing, which then enters an opening in the waveguide short-circuit wall. The CPW then tapers to a signal line width of 272 μm and 9 μm gap before it reaches a current probe, which extends from the bottom CPW trace to the top of the waveguide channel. The distance from the current probe to the waveguide back wall short-circuit is approximately $\lambda_g/4$ at the band center frequency. A small open-circuit stub on the other side of the current probe can be used to help tune the impedance match. The HFSS simulation results of the transition are plotted in Fig. 5(b), where good matching is achieved from 30 to 40 GHz. At 35 GHz, the simulated insertion loss of the transition is 0.67 dB.

IV. FABRICATION

The fabrication process of the waveguide switch is shown in Fig. 6. Silicon micromachining using deep reactive ion etching (DRIE) was chosen for its capability to achieve both small and large features with high precision [21]. The process starts with a high resistivity intrinsic silicon wafer 675 μm thick with a

1.2 μm thermal oxide grown on both topside and backside faces (1a). The oxide was patterned on both sides for the topside and backside DRIE masks (1b), where the topside etch was used to pattern the waveguide, silicon post, and waveguide feed network, and the backside etch was used to pattern cavities to insert and align the optical fibers directly above the silicon posts. The cavities for the fiber were then etched into the backside using DRIE (1c), and a PECVD nitride was deposited as an anti-reflection coating (1d). Next, to achieve two different topside etch depths for the main waveguide channel and high impedance slot of the π -match network, AZ 1529 photoresist was first patterned above the topside oxide (1e), and the high impedance π -match slot was etched (1f). The resist was stripped (1g), and the main waveguide channel was etched (1h). The topside oxide mask was stripped to improve the electrical connection of the post (1i). Deposition of a sputtered 100/1000 nm Ti/Cu layer metalizes the topside waveguide channel (1j), and the metal from the sidewalls of the silicon posts were removed by patterning AZ 1529 (1k) and wet chemical etching (1l). The individual samples were then diced (1m). For this prototype, a borosilicate glass wafer 1.1 mm thick was chosen for the bottom carrier wafer and CPW feed network. A 40/1000 nm Ti/Cu layer was patterned using a MicroChem LOR 5B and AZ 1512 bi-layer lift-off process, and the individual samples were diced (2a). Finally, the top and bottom wafers were bonded together using Cu-Cu thermocompression bonding (3a).

V. EXPERIMENTAL RESULTS

A. Experimental Setup

Fig. 7 shows the experimental setup for characterization of the π -match waveguide switch designed in section III. The device was measured using an Agilent E8361C PNA with an N5260A millimeter head controller, N5260-60003/60004 test head modules, and Cascade Microtech Summit 11000 probe station with Z-probes. The optical setup included a 915 nm, 7 watt Sheumann Laser Inc. laser diode [34] in a TO220 package pig-tailed with a 100 μm fiber and attached to a general purpose heatsink with thermal paste. The optical source at $\lambda_{\text{opt}} = 915 \text{ nm}$ ($h\nu_{\text{opt}} = 1.36 \text{ eV}$) was chosen to be within the range of high quantum efficiency for silicon [35]. A Wavelength Electronics TCS610 10 kOhm thermistor was inserted underneath the laser diode to monitor the operating temperature. The laser diode was driven by a Wavelength

Fig. 7. Experimental setup with (a) device characterization using a high frequency probe station, (b) optical fiber setup including beam splitter and connector losses, and (c) close up of the laser diode driver and device under test (DUT).

Electronics LD5CHA 5 A constant current laser diode driver [36] attached to a general purpose heatsink with thermal paste. The laser diode driver was powered by a Wavelength Electronics PWRPAK-5V +5 V switching power supply with less than 1% peak-to-peak input ripple and noise. In order to supply four separate fibers to the π -match switch, the 100 μm fiber was split into four 400 μm fibers using a non polarizing beam splitter with 25% power ratio from OZ Optics [37]. The estimated optical loss as given by the manufacturer for each component is shown in Fig. 7(b). The total loss at the output of each 400 μm fiber versus input optical energy from the laser diode, including the 25% power-ratio splitting, is estimated to be less than 10.5 dB. The choice of optical setup was mostly due to availability and experimental convenience. A more integrated setup could be employed in the future with less optical loss, using microLEDs or vertical-cavity surface-emitting lasers (VCSEL).

B. Measured Results

In Fig. 8, pictures of the fabricated waveguide switch prototype are presented. The top and bottom wafer pieces before bonding are shown in Fig. 8(a), highlighting the switch region, the CPW-to-waveguide transition region for characterization, and the back-to-back waveguide without silicon posts or π -

Fig. 8. Picture of the (a) top and bottom wafers highlighting the switch region, CPW-to-waveguide transition, and the back-to-back waveguide without silicon posts or π -match network, (b) the device after bonding (units in μm), and (c) the measurement of the device using two FormFactor |Z| Probes, with four optical fibers inserted into the four holes etched in the backside of the top wafer located above each silicon post.

Fig. 9. Measured and simulated ON-state scattering parameters for the waveguide switch, with inset (a) the back-to-back structure (with no silicon posts).

match network for switch loss extraction. Fig. 8(b) shows the bonded waveguide switch, highlighting the hole locations for the optical fibers, and final dimensions of the waveguide switch including transitions. In Fig. 8(c), a picture of the probe measurement is shown, with the four optical fibers inserted into the holes located directly above the silicon posts.

In Fig. 9, the measured ON-state scattering parameters of the π -match waveguide switch are compared with the simulation results from HFSS, including CPW-to-waveguide transitions. The measured switch has return loss greater than 20 dB from 29.2 – 41.6 GHz, and return loss greater than 10 dB from 27.4 – 47.2 GHz. At 35 GHz, the measured insertion loss is 2.86 dB, with a minimum and maximum insertion loss of 2.81 dB and 3.71 dB, respectively, within the 20 dB return loss bandwidth.

To extract the loss of the switch element by itself, the back-to-back waveguide structure without the silicon posts and π -match network shown in Fig. 8 was measured, with its scattering parameters shown in Fig. 9(a). The extracted ON-state insertion loss of the waveguide switch element is then

found by subtracting the insertion loss of the back-to-back structure from the insertion loss of the waveguide switch. With a measured back-to-back insertion loss of 2.34 dB at 35 GHz, the measured extracted insertion loss of the switch is 0.52 dB, while the net impact of the switch element across the entire band from 30 GHz to 40 GHz is below 0.88 dB.

The discrepancy between measured and simulated return loss is likely due to the fabrication tolerances of the silicon DRIE processes shown in Fig. 6. First, the fabricated sidewalls had a measured negative slope of 2.8° . Second, the etch depths for both the waveguide channel and high impedance slot had measured tolerances of approximately $\pm 5\%$ across the wafer. With target etch depths of 200 μm and 220 μm , respectively, this led to a variability of $\pm 10 \mu\text{m}$ and $\pm 11 \mu\text{m}$ for the final height of the two regions, respectively.

The discrepancy between the measured and simulated insertion loss is likely due to the overall thickness and skin depth of the sputtered copper across the wafer, especially considering the thickness of the sidewall coverage will generally be less than the horizontal surfaces. The conductivity of the sputtered copper was measured using a four-point probe, with a value of $\sigma = 2.3 \times 10^7 \text{ S/m}$. Thus, at 35 GHz, the skin depth is approximately 561 nm. Increasing the sputtered copper thickness from 1 μm to greater than $3\times$ the calculated skin depth would help decrease insertion loss.

Furthermore, the period of time between sputtering and bonding allows the growth of a copper oxide. The effect of this oxide was determined to be most significant at the current probe of the CPW-to-waveguide transition. To mitigate this effect, a quick 10 second dip in diluted hydrochloric acid solution right before the bonding step in Fig. 6 was carried out during fabrication to remove the oxide layer [38]. However, a certain amount of oxide will always be present due to a non-negligible amount of time the sample spends in atmosphere between the acid dip and bonding step, while the acid dip also slightly increases surface roughness. This effect can be mitigated for industrial applications with proper levels of process control, i.e., keeping the copper in an inert environment at all times.

In Fig. 10, the measured OFF-state (a) isolation ($|S_{21}|$) and (b) return loss ($|S_{11}|$) of the waveguide switch are shown with increasing optical power at the output of each fiber. At 35 GHz, an isolation of 20 dB and return loss of 9 dB is achieved at an optical power of 50.1 mW per fiber, while an isolation of 25 dB and return loss of 6 dB is achieved at an optical power of 166.7 mW per fiber. This is significant isolation for this frequency range, and clearly demonstrates the potential of this technology for mm-wave switch applications.

It is noted in Fig. 10 that with increasing optical power above 166.7 mW up to 332.1 mW, the isolation improves by only 0.51 dB. Thus, a saturation point is reached, where any further increase in optical power no longer returns a significant change in isolation. However, the post continues to become more conductive, reducing the total loss in the system, which will be discussed in the next section. To further improve OFF-state isolation, additional posts can be added, keeping in mind the need to compensate for an increase in ON-state capacitive loading with the π -match region.

Fig. 10. Measured OFF-state (a) isolation ($|S_{21}|$), and (b) return loss ($|S_{11}|$) of the waveguide switch with increasing optical power. The value shown is the power output of each individual fiber for the two-by-two post array as shown in Fig. 3.

C. Theoretical Validation

The theory derived in section II is now used to correlate the measured waveguide switch performance versus applied optical power to the simulated performance versus the conductivity of the silicon posts. As described in section II, the photo-excited silicon elements simulated in HFSS are treated as a material with real conductivity and permittivity, where the permittivity for a given conductivity is determined from (16) [30]. To isolate the effect of losses due to the silicon plasma from losses associated with the copper conductor, the ON-state loss is subtracted from the OFF-state loss at each applied optical power level (or each simulated conductivity), with the respective loss calculated using the equation [31]

$$Loss = 1 - |S_{11}|^2 - |S_{21}|^2. \quad (19)$$

In Fig. 11, the extracted losses of the measured and simulated waveguide switch are plotted, with inset (a) showing the correlation between the photogenerated conductivity versus applied optical power. By adjusting the fitting coefficients of the carrier lifetime in (10), a good match between simulation and measurement is achieved with values $\tau_0 = 6.2 \mu\text{s}$ and $N_0^{ref} = 1.1 \times 10^{16} \text{ cm}^{-3}$, which are within the respective ranges for silicon. As the optical power begins to increase, a peak in the extracted loss occurs at approximately 69 S/m. Here, the silicon post is in its most lossy state, behaving

Fig. 11. Measured and simulated extracted loss at 35 GHz, with inset (a) the correlation between photogenerated conductivity versus applied optical power.

closer to an absorptive switch. Further increasing the optical power decreases the loss, with more power reflected due to the increase in conductivity of the silicon plasma. Furthermore, it is interesting to note that the above technique can be used as a reasonably effective method to characterize the carrier lifetime of silicon at microwave and millimeter-wave frequencies.

D. Application as a Variable Attenuator

As is shown in Fig. 10, by adjusting the amount of optical power, a variable attenuator can be achieved with the proposed waveguide switch. Therefore, it is important to know how the transmission phase delay and group delay change versus the level of attenuation.

Fig. 12(a) plots the phase of S_{21} versus frequency for a few different optical power levels along with the measured unloaded back-to-back waveguide. With greater optical power, the amount of phase lag at 13.0 mW increases compared to the ON-state (laser OFF). However, at 50.1 mW and above, the amount of phase lag decreases compared to the ON-state. In addition, the phase lag of the switch is lower than the phase lag of the back-to-back waveguide above approximately 83.4 mW. There is also a slight increase in the slope from 30 GHz to 40 GHz at all power levels other than the ON-state, indicating a dispersion effect when the silicon post is in its excited state.

In Fig. 12(b), the measured and simulated S_{21} group delay versus frequency are shown for the ON-state (laser OFF), the OFF-state at the maximum applied power level, and the OFF-state at an intermediate power level showing the minimum achieved group delay, along with the unloaded back-to-back waveguide. The group delay τ_g is calculated using the equation [39]

$$\tau_g = d\phi/d\omega \quad (20)$$

where ϕ is the phase of S_{21} , and ω the angular frequency. The S_{21} phase data for each measured trace was pre-fit with a 5th order polynomial to reduce the systematic calibration error. The fitted data was then used to calculate the group delay.

A clear decrease in group delay is observed, indicating that with increased optical power, the group velocity of the waveguide switch becomes greater than the group velocity of the unloaded back-to-back waveguide. As the switch transitions

Fig. 12. (a) Measured S_{21} phase, and (b) measured and simulated S_{21} group delay versus frequency of the waveguide switch at different optical powers. The phase and group delay of the back-to-back waveguide (without silicon posts and π -match network) are also shown for comparison.

between the ON-state to the OFF-state, within the transition, an evanescent mode effect inside a waveguide channel is known to give faster group velocity than the unloaded case [40].

It is also worth mentioning the significant jump in the level of attenuation from the ON-state to the lowest power OFF-state in Fig. 10. This is likely due to the sensitivity of the laser diode driver used in experiment. Having more sensitive control of the drive current for the laser diode would allow lower optical power levels, and thus attentions, to be reached.

VI. DISCUSSION

Table I compares the performance of the presented photogenerated silicon plasma waveguide switch to the state-of-the-art in millimeter-wave waveguide switches, grouped by electrical (top) and mechanical (bottom) based technologies. While electromechanical switches achieve very good insertion loss and isolation, they suffer slow switching speeds in the millisecond range and are generally large in size [3]. The RF MEMS switches achieve the lowest insertion losses with good isolation, yet their fabrication is more complex and their switching speed is in the high 10s of microseconds [8]. Comparing the electronic switches, the photogenerated silicon plasma switch of this work achieves the lowest insertion loss, and is orders of magnitude smaller than the silicon plasma switch presented in [19].

TABLE I
PERFORMANCE COMPARISON OF MILLIMETER-WAVE WAVEGUIDE SWITCHES

Ref.	Switching Technology	Frequency Range (GHz)	Fractional Bandwidth	Peak Insertion Loss (dB)	Isolation (dB)	Volume Normalized to λ^{3a}
This Work	Photogenerated Silicon Plasma	29.2 – 41.6	35%	0.52	> 25	0.005
[19]	Photogenerated Silicon Plasma	170 – 260	42%	0.7	> 45	3.98
[14]	Photogenerated Silicon Plasma in SIW	23.3 – 26.5	13%	0.7	> 22	0.017
[4]	PIN Diode ^b	60 – 90	40%	2.5	20	131.8
[41]	PIN Diode in SIW	20 – 24	18%	1.3	> 10	0.11
[3]	Electromechanical ^c	26.5 – 40	41%	0.4	60	211.4
[42]	Mechanical in SIW	50 – 75	40%	4.5	> 45	0.096
[7]	RF MEMS	60 – 80	29%	< 0.2	> 20	0.002
[8]	RF MEMS	60 – 70	15%	0.4	> 30	0.22
[10]	Microfluidic	25 – 40	46%	< 0.5	> 22	1.47

^a In the respective material at lowest band frequency.

^b QuinStar Technology, Inc. QSD series.

^c QuinStar Technology, Inc. QWZ series.

VII. CONCLUSION

A photogenerated silicon plasma π -match waveguide switch using silicon bulk micromachining was presented for operation at millimeter-wave frequencies. A theoretical study of the photoconductivity model along with the design procedure for a π -match waveguide switch were discussed, with measured results agreeing well with simulation. The reported measured ON-state return loss was below 20 dB from 30 – 40 GHz, with extracted insertion loss as low as 0.52 dB at 35 GHz, and less than 0.88 dB across the entire band. The OFF-state isolation was greater than 25 dB at 35 GHz, and showed good variability versus optical excitation energy for application as a variable attenuator. A microfabrication process flow using deep reactive ion etching to form silicon posts within the waveguide channel was presented, allowing for both high accuracy and low cost manufacturing due to economies of scale. The presented results highlight the significant potential of silicon micromachined waveguide switches using optically excited plasma tuning elements for controlling millimeter-wave signals in high power and high speed switching applications.

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