A Very Low-phase-noise CMOS Ring VCO Intended for Sensor Interfaces

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Abstract—We describe in the paper a ring voltage-controlled oscillator (VCO) indicating an improved phase noise over a wide range of frequency offsets and an extended frequency/voltage tuning range. The phase noise is improved by leveraging a better linearity approach, while reducing the VCO gain and maintaining wide tuning range. The proposed VCO is a block of a time-domain comparator embedded in a monitoring and readout circuit of an industrial sensor interface. An analytical model is extracted resulting in closed-form expressions for both input-referred noise and phase noise of the VCO. Employing the analytical expressions, the contributed noise and phase noise limitations are fully addressed and all the effective factors are investigated. The prototype of the proposed VCO was implemented and fabricated in a $0.35\ \mu\text{m}$ CMOS process. The integrated VCO consumes $0.903\ \text{mW}$ from a $3.3\ \text{V}$ supply, when running at its maximum frequency of $9.37\ \text{MHz}$. The measured phase noise of the proposed VCO is $-147.57\ \text{dBc/Hz}$ at $1\ \text{MHz}$ offset from the $9.37\ \text{MHz}$ oscillation frequency, and the occupied silicon area of circuit is $0.005\ \text{mm}^2$.

Index Terms—Sensor interface, ring oscillators, Voltage controlled oscillator, phase noise, linear characteristics.

I. INTRODUCTION

THE evolution of sensor electronic interfaces become a vital step to attain numerous high-performance mixed-signal ICs in a wide range of applications. In the real world, these enhancements yield communication advances between various electronics systems conducting analog or digital signals from sensors, switches, antennas, etc [1]. In such a scenario, a sensor interface is required to pre-process the sensor signals prior to feeding them to the next system level. Therefore, the sensor interface's reliability, safety, efficiency, and compactness influence the performance of the whole system.

Over the past decades, growing appeals on compact and low-cost systems with very limited power budget rises the need for advanced integration methods, such as System-on-Chip (SoC) and System in Package (SiP) structures. Furthermore, the semiconductor industry is directed to smaller technologies so as to improve cost, energy consumption, speed, and achieve a high-level integration of the devices [2]. Therefore, the continued proliferation of small integrated systems provokes the necessity of innovative on-chip techniques and topologies for electronic interfaces.

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Fig. 1. Block diagram of the proposed sensor interface with monitoring stage.

Traditionally high-performance analog interface methods include conventional analog building blocks, such as operational amplifiers, and highly-matched capacitive DACs in a feedback loop. Although technology scaling is especially beneficial for digital circuits, it raises some difficulties in designing analog blocks as a result of lowering supply voltage, which reduces the intrinsic transistor properties (e.g. lower gain, mismatch) [3]. Moreover, these analog architectures do not follow the same power reduction and area scaling as digital circuitry, resulting in large power and chip area in scaled CMOS technologies. So, purely analog solutions suffer from poor portability to other technology nodes [4]. As a result, time-based interfaces have become more popular recently thanks to their highly-digital implementation which offers a small area, a high energy efficiency, and good scalability, exploiting the benefits of advanced technology nodes [5]–[7].

Sensor interface ICs connect right to a sensing element and provide the necessary signal conditioning intended to extract an accurate signal for monitoring and control systems. Process monitoring is an essential part of any sensor interface as the sensing nodes are exposed to extreme and unpredictable conditions [8]. Therefore, special considerations must be taken in designing the monitoring stage to meet the readout requirements for the sensor interface. Fig. 1 shows a novel structure which allows adaptive operation of readback circuitry in a load switch sensor interface. In this configuration, the monitoring circuit is employed to form the closed-loop frequency control system in order to read and process the load voltage/current. Thereafter, the processed feedback signal will be compared with a FPGA command signal through an internal control stage

for the purpose of fault detection.

In this type of architecture, the switch sensor information is inserted into a time domain comparator (TDC) and converted to frequency information through adopted Voltage-Controlled Oscillators (VCOs). Then, the frequency-domain outcome is compared to a consistent and distinctive reference frequency. This reference frequency could be provided from the FPGA. Therefore, the VCO is one of the most critical blocks in our proposed sensor interface structure. Also, it is considered as a key circuit in modern system designs such as VCO-based comparator (or TDC), phase locked loops, clock/data recovery, frequency de/modulation, and synchronizing circuits [9], [10].

The most common techniques to implement VCOs are using ring structures, LC resonant configuration, or relaxation circuits. LC-VCOs exhibit better phase noise performance owing to high Q resonator. However, besides the limited tuning range of these structures, adding high-performance bulky passive devices (such as inductors) to a CMOS process leads to chip complexity, area and cost inefficiency [11]. On the contrary, ring VCOs are popular alternative in scaled CMOS technologies since they offer wide tuning range, less die area, straightforward integrated design, multi-phase output capability, and good power performance which substantially decreases with scaling [12].

In consequence, a ring type VCO is a promising approach for voltage-to-time conversion, frequency translation, and generating required periodic signals for timing in digital circuits that are widely used in industrial platforms. However, ring VCOs suffer from poor phase noise behavior and the non-linear nature of voltage-to-time conversion provokes the linearity issue in a time-domain comparator [13], [14].

In attempt to obtain low phase noise, authors of [15] promote rail-to-rail voltage swings. However, their employed delay cells limit the design's noise performance by injecting a substantial amount of noise during the VCO's transition periods. Another study presented in [11] focused on injected channel thermal noise reduction in transistors during VCO's output transitions, however the VCO performance remains limited due to low frequency tuning range and large power consumption. An ultra-low-power ring VCO is achieved in [16] by employing a differential delay cell to generate negative conductance without requiring the cross-coupled latch. This design suffers from unattractive phase noise performance, low frequency tuning range, and large occupied area as a result of the passive components used in the delay cell implementation.

In this work, we present a compact, wide-swing, enhanced phase-noise, and low-power CMOS ring VCO which employed a linearization technique to improve the overall characteristics. This architecture exploits a fully integrated, time-based electronic interface circuit and is tested with industrial load switch sensors at micro scales in power management industrial applications. The rest of the paper is organized as follows: Section II describes the phase noise analysis of the ring-VCO. The design and the analysis of the proposed VCO architecture are revealed in Section III. Section IV presents the measurement results while Section V discusses the performance of the proposed VCO in comparison with prior-art. The conclusion is drawn in Section VI.

Fig. 2. Different regions of phase noise spectral density.

II. ANALYSIS OF THE RING OSCILLATOR DESIGN

There is an inherent trade-off between the diverse properties of ring oscillators; phase noise, tuning range, linearity, gain, voltage swing, power dissipation, and supply voltage. Phase noise of an oscillator is a short-term instability, or variations from perfect periodicity, which leads to some deviation on amplitude, phase or in severe cases the frequency range in frequency domain [10]. Phase noise induces various interferences and errors in integrated circuits' functionality, so it is a leading concern in the field of circuit design.

A wide variety of models has been developed to quantify these fluctuations and analyze the phase noise of the oscillator. The short-term instabilities in a signal are normally characterized in the matter of a single side-band noise spectral density (dBc /Hz) given by [14]

$$\mathcal{L}_{\text{total}}\{\Delta f\} = 10 \cdot \log \left[\frac{\mathcal{P}(f_c + \Delta f)}{\mathcal{P}_{\text{Signal}}} \right], \quad (1)$$

where $\mathcal{P}(f_c + \Delta f)$ is the one-side power at Δf offset frequency from the carrier with a measurement bandwidth of 1 Hz and $\mathcal{P}_{\text{Signal}}$ is the carrier power. The well-known equation (2) avowed that the total average power carried by signal or noise is equal to the area under its spectrum.

$$\mathcal{P}_{\text{Signal}} = \int \mathcal{S}_{\text{signal}}(\Delta f) d(\Delta f) \quad (2)$$

On the other hand, in order to emphasize on the noise power per unit bandwidth definition, the mean-square noise voltage density, $v_{\text{noise}}^2/\Delta f$ (or v_{noise}^2 at bandwidth = 1 Hz), and $\mathcal{S}_n(\Delta f)$ are used interchangeably. This normalization brings in the following equation for the normalized single-sideband noise spectral density:

$$\mathcal{L}_{\text{total}}\{\Delta f\} = 10 \cdot \log \left[\frac{v_{\text{noise}}^2}{v_{\text{signal}}^2} \right], \quad (3)$$

According to the type of devices used to implement the VCO, the contributing noise sources are thermal noise of parasitic resistance, thermal noise of transistors channel and transistors' flicker noise which is responsible of the phase noise in low frequency circumstances. In order to convert the flicker noise to phase noise of a VCO, we should consider the $1/f$ region behavior in the noise spectral density plot. As shown in the Fig. 2, the upconversion of the low-frequency

dominant noise, $1/f$ noise, is governed by the behavior in the $1/f^2$ and $1/f^3$ regions. By considering the transfer function approach, these behaviors can be realized in the commonly used Leeson's noise model [14]:

$$\mathcal{L}_{\text{total}}\{\Delta f\} = 10 \log \left[\frac{2 \cdot \mathcal{F} \cdot \mathcal{K} \cdot T}{P_{av}} \cdot \underbrace{\left[1 + \left(\frac{f_{osc}}{2 \cdot \Delta f \cdot Q} \right)^2 \right]}_{\alpha} \cdot \underbrace{\left(1 + \frac{\Delta f_{1/f^3}}{\Delta f} \right)}_{\beta} \right] \quad (4)$$

where

- $\mathcal{F}$ noise empirical factor
- $\mathcal{K}$ Boltzmann's constant (J/K)
- T Temperature (K)
- f_{osc} central frequency
- Q the loaded quality factor
- $\Delta f_{1/f^3}$ flicker noise corner frequency
- P_{av} average power dissipated at oscillator output

This equation experimentally portends the phase noise presence in the VCO, where terms α and β respectively correspond to $1/f^2$ and $1/f^3$ regions which can be attributed to the effect of transistor $1/f$ noise on the phase noise of the oscillator.

Typically, most reported phase noise models do not consider the nonlinearity in the tuning characteristics of VCOs which yields to a nonuniform performance of the phase noise over the tuning range. Any noise on the control line can provoke additional phase noise, and thereby such nonlinearity degrades the settling behavior of the system. As a result, the disturbance of the output phase and frequency as a consequence of noise on the control line is of great importance in the design of VCOs. This term can be added to the equation (4) to take this additional noise mechanism into account.

The output oscillation frequency of a VCO is a function of its control voltage, such as:

$$K_{VCO} = \frac{\partial \omega_{osc}}{\partial V_{cont}}, \quad (5)$$

$$\omega_{osc} = \omega_0 + K_{VCO} \cdot V_{cont} \quad (6)$$

where K_{VCO} is the tuning gain and ω_0 is free running frequency of the ring oscillator. Suppose v_n as a voltage noise at the tuning node of the oscillator, based on the equation (6), for a given noise amplitude, the noise in the output frequency is proportional to K_{VCO} . Therefore, it will affect the power spectral density (PSD) of noise and thereby the phase noise behavioral model. On the other hand, we know that the output spectrum of a time-invariant system with transfer function $H(s = 2\pi jf)$ in view of an applied signal with spectrum $\mathcal{S}_{sig}(\Delta f)$ is given by

$$\mathcal{S}_{out}(\Delta f) = \mathcal{S}_{sig}(\Delta f) \cdot |H(\Delta f)|^2 \quad (7)$$

Since phase is the integral of the frequency, the VCO acts as an ideal integrator for the control voltage when the output variable is phase. So, its transfer function can be simply expressed as $H_{vco}(s) = \frac{K_{VCO}}{s}$. Therefore, the one-sided

Fig. 3. Schematic of the proposed ring-based VCO.

spectral density of a signal's phase deviation caused by a given noise in the VCO can be written as

$$\mathcal{S}_{\phi}(\Delta f) = \mathcal{S}_n(\Delta f) \cdot \frac{K_{VCO}^2}{\Delta f^2}. \quad (8)$$

Taking this scenario into consideration, the time-invariant model of Leeson would be modified considering the general definition of the phase fluctuation spectrum in equation (9) as follows:

$$\mathcal{L}\{\Delta f\} = 10 \cdot \log \left[\frac{\mathcal{S}_{\phi}(\Delta f)}{2} \right], \quad (9)$$

$$\begin{aligned} \mathcal{L}\{\Delta f, K_{VCO}\} = & 10 \log \left[\frac{2 \cdot \mathcal{F} \cdot \mathcal{K} \cdot T}{P_{av}} \left[1 + \left(\frac{f_{osc}}{2 \cdot \Delta f \cdot Q} \right)^2 \right] \left(1 + \frac{\Delta f_{1/f^3}}{\Delta f} \right) \right. \\ & \left. + \underbrace{\left(\frac{v_n^2 \cdot K_{VCO}^2}{2 \cdot \Delta f^3} \right)}_{\chi} \right] \end{aligned} \quad (10)$$

Therefore, the equation (10) substantiates the major impact of the VCO gain on the phase fluctuation. The phase noise can be enhanced by the output voltage swing increment, fast transition, dropping the voltage/current noise sources during transitions, and K_{VCO} reduction. As highlighted before, in the conventional on-chip ring-VCO designs, nonlinearity across the tuning range leads to a variable gain and thereby inconstant phase noise. Wherefore, the less variation of VCO gain, the less effect of noise on V_{cont} . This paper focuses on an enhanced approach for linearity improvement and while attaining wide tuning range ring-VCO along with a minimized and constant K_{VCO} to ameliorate the phase noise.

III. PROPOSED VCO ARCHITECTURE

A. Topology of the Proposed VCO

Fig. 3 presents the architecture of the proposed VCO. It consists of five voltage-to-time converter (VTC) stages in addition to a buffer at the output of the VCO to sharpen the generated signal. In each VTC stage, the control voltage (V_{cont}) is

Fig. 4. Equivalent noise circuit of the proposed VTC stage.

applied to the voltage-controlled current source M_{P1} and the resulting current is mirrored to the inverter (constructed from M_{P4} and M_{N4}) through the current mirror M_{N1} , M_{N2} , and M_{P2} . The non-linearity imperfection stems from the relation of the inverter current, I_{out} , with $(V_{GS_P})^2$ (the gate-source voltage of the controlling PMOS = $V_{DD} - V_{cont}$) in VTC stage. In order to deal with this constraint, a linearization method is used in the VCO implementation to reduce the effect of this issue on the current of the clocked inverter.

To improve the VCO linearity, the employed current mirrors have been designed with a small mirroring factor to decrease the effect of gate-source voltage of the controlling PMOS (M_{P1}), and thereby V_{cont} to the clocked inverter's current. However, the improvement in linearity results in lowering the VCO gain. This has no impact on the functionality of the proposed VCO since the required tuning is only from 0.01 MHz to 10 MHz. Furthermore, in contrast to some conventional ring VCOs which are tuned by supply voltage variation, the proposed VTC block is maximising the output swing by coupling the input signal to the gate of the current source transistor, M_{P1} . This bias controlled voltage/current configuration is optimized in such a manner that the VTC cell's transistors remain in saturation region for the entire control voltage range. Hence, a wider tuning range is obtained.

For a single-ended VCO, the oscillation frequency is primarily realized by the number (N) and the propagation delay (t_p) of VTC stages:

$$f_{osc} = \frac{1}{\tau} \simeq \frac{1}{2 \cdot N \cdot t_p}. \quad (11)$$

The propagation delay time can be estimated by the average tail current resulting from the tuning current going through the output capacitance, as

$$f_{osc} = \frac{I_{out}}{2 \cdot N \cdot V_{sw} \cdot C_{tot}}, \quad (12)$$

where V_{sw} is the peak-to-peak voltage swing of V_{out} and C_{tot} is the total parasitic capacitance seen at the output of every VTC stage [17]. According to equation (5) the gain can be expressed as:

$$K_{VCO} = 2\pi \frac{\partial f_{osc}}{\partial V_{cont}}, \quad (13)$$

By considering equations (12) and (13), the VCO's gain is expressed as:

$$K_{VCO} = 2\pi \frac{\partial I_{out}}{2 \cdot N \cdot V_{sw} \cdot C_{tot} \cdot \partial V_{cont}} \quad (14)$$

Therefore, the current-source biasing, without the need of additional passive components or sophisticated controlling approaches, leads to a high steepness in transition slope, faster transition, output swing augmentation, and tuning range improvement. This enhances the phase noise of the presented VCO, based on equation (14). Additionally, flicker noise of transistors used to implement the VCO is the dominant close-in phase noise source. This impact was reduced by adopting PMOS transistors for input controlling source since holes are less likely to be trapped and leads to inherent lower flicker noise of PMOS than the NMOS transistors.

B. Noise analysis

To drive the proposed VCO's noise contribution, the generated noise by means of each VTC stage have to be first calculated. The noise in the MOSFETs at low frequency can be referred to the gate as a series noise voltage source with a PSD of $\overline{v_n^2}$ (or equivalently noise current source $\overline{I_n^2}$ across the drain) [10]. By considering the M_{P1} reflected current to the current-starved inverter stacks, the equivalent noise transfer model of the proposed VTC can be illustrated as shown in Fig. 4. It is worth mentioning that pull-up and pull-down currents incorporate the uncorrelated noise effect of M_{P1} and the current mirror which might not vary over a single transition, and alters gradually after many transitions.

Due to the pull-up and pull-down currents supplies, the frequency oscillation in the j th VTC stage of an N -stage ring VCO is [18]

$$f_{osc} = \frac{2}{V_{DD} \cdot C_{tot}} \left(\sum_{j=1}^N \frac{1}{I_{N_j}} + \frac{1}{I_{P_j}} \right)^{-1}, \quad (15)$$

Concerning the control-line noise realization in the phase noise of the VCO, the equivalent one-side spectral density in (8) can be written as [18]

Fig. 5. The proposed VCO phase noise based on analytical model.

$$\begin{aligned} S_{\phi}(\Delta f) &= S_n^i(\Delta f) \cdot \frac{K_I^2}{\Delta f^2} = \frac{\overline{I_n^2}}{\Delta f} \cdot \frac{(\partial f_{osc}/\partial I_{N_k})^2}{\Delta f^2} \\ &= \frac{1}{\Delta f^3} \left(\frac{f_{osc}}{2 \cdot N \cdot I_{out}} \right)^2 \overline{I_n^2} \end{aligned} \quad (16)$$

where K_I is the sensitivity of f_{osc} to the pull-up (or pull-down) current and $I_{N_j} \simeq I_{P_j} \simeq I_{out}$ is considered. Using equation (16), the last term in the modified phase noise equation (10), χ , can be calculated as

$$\chi = \frac{1}{2\Delta f^3} \left(\frac{f_{osc}}{2 \cdot N \cdot I_{out}} \right)^2 \times N \left(\overline{I_{n_{N_k}}^2} + \overline{I_{n_{P_k}}^2} \right) \quad (17)$$

By considering the MOSFET flicker noise and the channel thermal noise in the active region, the equivalent input noise PSD for both uncorrelated sources is given by

$$\overline{v_n^2} = \frac{K_f}{WLC_{ox}\Delta f} + \frac{4 \cdot \mathcal{K} \cdot T \cdot \gamma}{g_m} \quad (18)$$

and

$$\begin{aligned} \overline{I_n^2} &= g_m^2 \overline{v_n^2} = \\ &\left[\left(2\mu C_{ox} \left(\frac{W}{L} \right) I_{out} \right) \cdot \frac{K_f}{WLC_{ox}\Delta f} \right] + 4 \cdot \mathcal{K} \cdot T \cdot \gamma \cdot g_m \end{aligned} \quad (19)$$

where $K_f \approx 10^{-25} (V^2 F)$ is a process dependent constant and coefficient γ is typically equal to 2/3 for long-channel transistors. By substituting equation (19) in equation (17), the control-line noise contribution in the phase noise equation can be approximated as

$$\begin{aligned} \chi &= \frac{1}{8 \cdot N \cdot \overline{I_{out}^2}} \cdot \frac{f_{osc}^2}{(\Delta f)^3} \left[\frac{8}{3} \cdot \mathcal{K} \cdot T \cdot (g_{m_n} + g_{m_p}) \right. \\ &\quad \left. + \frac{2I_{out}}{\Delta f} \left(\frac{\mu_n K_{fN}}{L_N^2} + \frac{\mu_p K_{fP}}{L_P^2} \right) \right] \end{aligned} \quad (20)$$

In order to address the terms α and β , the quality factor, Q , and the flicker noise corner frequency, $\Delta f_{1/f^3}$, must be analyzed. Among the several definitions for the Q factor, the open-loop Q concept proposed by Razavi is well conformed with Leeson's formula [10]. This frequency-domain, transfer-function-based techniques states that the open-loop Q factor is a measure of the closed-loop mechanism persistency against

the oscillation frequency variations. This widely-used Q definition characterizes an oscillator's frequency stability and is represented by a frequency-to-line width ratio:

$$Q = \frac{f_{osc}}{\Delta f_{3dB}} \quad (21)$$

where Δf_{3dB} is the 3dB line-width of the spectrum of the oscillator's output.

On the other hand, for oscillator designs with a moderate Q factor, we can assumed approximately that $\Delta f_{1/f^3}$ portion of the curve shown in Fig. 2 meets the segment of the white noise region, and $\Delta f_{1/f^3} \approx \frac{f_{osc}}{2Q}$.

Consequently, in view of the typical noise figure value, $F \approx 5$ dB, the standard absolute temperature $T = 290$ K, and the Boltzmann's constant $\mathcal{K} = 1.38 \times 10^{-23}$ J/K, and the analytical phase noise model of the proposed VCO can be approximated as

$$\begin{aligned} \mathcal{L}\{\Delta f, K_{VCO}\} &\simeq \\ 10 \log \left[\frac{2.53 \times 10^{-20}}{P_{av}} \left(1 + \left(\frac{f_{osc}}{2 \cdot Q \cdot \Delta f} \right)^3 \right) + \chi \right] \end{aligned} \quad (22)$$

Fig. 5 shows the proposed VCO phase noise for different offset frequency obtained by the developed analytical model of equation (22) at the maximum oscillation frequency. In section IV where the measurement results of the proposed VCO is covered, we will explain and justify that the employed analytical methods have a good agreement with the real-time experimental phase noise behaviour.

C. Design Considerations

According to the equation (22), the phase noise of the VCO is inversely proportional to the output current and oscillation frequency while it is proportional to the carrier power. Therefore, there is a trade-off between the frequency range and the power budget and their impact on the phase noise. The power (or current) consumption and the frequency range of the generated signals at the output of the proposed VCO may vary according to the chosen parameters and the target application (here low noise integrated readout interface). With respects to these trade-offs, a nearly optimal design with low phase noise and low power consumption can be achieved.

The target point of this ring oscillator design is to generate up to 10 MHz pulse signals and feed its time (frequency)-domain information to the next block to define a bit decision at the end of a low-power, low-noise, high-resolution time-domain (VCO-based) comparator. To this end, the proposed five-stage ring-VCO were designed and fabricated using a 0.35 μm standard CMOS technology with a power supply value of 3.3 V. The circuits were designed with AMS-kit rules that required a minimum drawn channel length of 0.4 μm . The test chip also included other circuits such as an integrated internal controlling prototype, phase-frequency detector (PFD) circuit, and TDC networks, but these are not discussed in this brief.

Fig. 6. Chip micrograph of the proposed VCO.

Fig. 7. Measured oscillation frequency and power consumption of the proposed VCO versus its control voltage.

IV. MEASUREMENT RESULTS

The chip micrograph of the proposed linear ring VCO prototype, which is a part of a monitoring and readout circuit in industrial sensor interface, is shown in Fig. 6. The VCO occupies an area of 0.005 mm^2 with a form factor of $34 \mu\text{m} \times 161 \mu\text{m}$. The chip is wirebonded inside a pin grid array (PGA) package for measurements. The package is soldered to a custom printed-circuit board (PCB) for test. Decoupling capacitors with value of $0.1 \mu\text{F}$ and $10 \mu\text{F}$ are utilized to filter the power lines.

The measured oscillation frequency and its corresponding core power consumption of the integrated VCO as a function of its tuning voltage is depicted in Fig. 7. As shown in the figure, the presented VCO exhibits an improved linear performance. The VCO was designed to generate output frequency between 0.01 MHz and 10 MHz for a control voltage varying from 0 to 2.5 V. However, the measured output is from 0.01 up to 9.37 MHz resulting in a tuning range, TR_f , of 199.5%. This slight degradation in the maximum measured generated frequency is because of process variations and the generated capacitances from PCB traces and coaxial cable in the signal path.

Fig. 8 shows the measured VCO phase noise behavior, where it exhibits values of -87.69, -114.87, -145.80, and -147.57 dBc/Hz at 1 kHz, 10 kHz, 100 kHz, and 1 MHz offset

Fig. 8. Measured phase noise performance of the VCO.

Fig. 9. Measured spectrum of the VCO at a control voltage of 0 V

Fig. 10. Accuracy of measured phase noise compared to the analytical model.

from 9.37 MHz carrier, respectively. Furthermore, it shows the measured RMS jitter at 1 MHz bandwidth of integration equal to 17.64 ps (or 1.039 mrad). In addition, the measured spectrum of the presented VCO circuit when tuned to generate a maximum frequency of 9.37 MHz (with $V_{cont} = 0 \text{ V}$) is shown in Fig. 9. The prediction of analytical model given in equation (22) has been compared with the measured phase noise of the integrated VCO in Fig. 10. The carrier frequency in the equation (22) is optimized with respect to the measured

TABLE I
PERFORMANCE SUMMARY AND COMPARISON OF THE PROPOSED VCO WITH PRIOR-ART PUBLICATION.

Reference	Tech. (nm)	Supply (V)	Oscillation Freq. (MHz)	Avg. Pdis (mW)	Phase Noise ^a (dBc/Hz)	Frequency TR _f (%)	Voltage TR _V (%)	Area (mm ²)	FoM ₁ (dBc/Hz)	FoM ₂ (dBc/Hz)
This Work	350	3.3	0.01-9.37	0.32	-147.57	199.5	76	0.005	-168	-193.45
TCASII'13 [11]	65	1	480-1010	10	-110.8	71.2	80	0.0225	-157	-174
TCASII'01 [15]	500	1.5	290.5-470.9	2.25	-105	47.4	50	0.0127	-159.4	-172.91
TCASII'18 [16]	65	0.6	430-550	0.045	-94.84	25.2	99	0.21	-162.1	-170.13
TCASII'18 [20]	130	1.2	2-20	0.27	-88.59	163.6	75	0.01 ^b	-117	-141.27
TCASII'17 [21]	180	1.8	400-850	1.17	-97	72	58	0.0008	-156.3	-173.45
Int. J'11^c [22]	180	3.3	16-368.9	25.5	-100	183.4	80	N/A	-129	-154.26
JOLPE'17 [23]	350	2.5	100-450	0.4	N/A	127.2	40	0.02	N/A	N/A
JSSC'12 [24]	130	0.5	340-490	0.44	-91.5	36.2	99	0.0736	-151.6	-162.77
TMTAT'13 [25]	180	1.8	700-1200	9.5	-102	52.6	72	0.046	-151.52	-165.95
TVLSI'19 [26]	180	1.2	13.4	0.158	-124.07	N.A	N.A	0.117	-154.4	N.A

^a At 1 MHz offset frequency, ^b Estimated from die micrograph, ^c Simulation results

value of maximum oscillation frequency of 9.37 MHz. The result shows that the average phase noise variation is less than $\pm 2\%$ as the frequency offset changes from 1 kHz to 1 MHz. This small difference stems from some correlated noise sources on different nodes of the oscillator. For instance, substrate and supply noise, arising from current switching in other parts of the chip are considered negligible in the analytical model.

Table I summarizes the measured performance of the proposed VCO compared with state-of-art VCOs. In favor of a fair comparison with other relevant works at different oscillation frequencies and power dissipation, the following well-known Figure-of-Merit (FoM) is utilized [11],

$$\text{FoM}_1 = \mathcal{L}\{\Delta f\} - 20 \log \left(\frac{f_{osc}}{\Delta f} \right) + 10 \log \left(\frac{P_{diss}}{1mW} \right) \quad (23)$$

where $\mathcal{L}\{\Delta f\}$ is the phase noise at the offset frequency of Δf , f_{osc} is the oscillation frequency and P_{diss} is the VCO's consumed power. In addition, another FoM (FoM_2) with respect to the total frequency tuning range (TR_f) is defined as [19]

$$\text{FoM}_2 = \mathcal{L}\{\Delta f\} - 20 \log \left(\frac{f_{osc} \cdot TR_f}{10 \cdot \Delta f} \right) + 10 \log \left(\frac{P_{diss}}{1mW} \right), \quad (24)$$

$$TR_f = \frac{f_{max} - f_{min}}{f_{central}} (\%) \quad (25)$$

V. DISCUSSION

Table I presents various ring-VCO designs that were implemented in different CMOS processes, from 65- to 500-nm technologies. It can be seen that the phase noise of [15] is better than other designs with almost same oscillation

frequency range, such as [16], and [22]–[24]. This emanates from the larger phase noise for the short-channel oscillator compared to the long-channel one at the same center frequency and power dissipation due to the larger γ of the short-channel transistor [14]. However, this effect does not limit the phase noise of the 4-stages VCO in [11] compared to the designs with same frequency range in [21] and [25], at the cost of larger power consumption and occupied area even in a 65-nm technology.

As explained in Section III-C, the proposed VCO is designed for a sensor interface application where a low-frequency range was adopted. However, by adjusting the transistors feature size in the proposed design, higher oscillation frequency could be achieved. Generally, the maximum oscillator frequency as a function of the CMOS technology development has an ascending behaviour while the phase noise performance is descending. Therefore, it is evident that the proposed design at the higher frequencies may experience some degradation on its phase noise performance.

From FoM_1 prospective, the performance of all VCOs in terms of power consumption, and phase noise with respect to carrier frequency and considered frequency offset, can be examined. Also, TR_f behavior has been taken into account by FoM_2 . The presented structure in [20] and [26] is implemented to operate at low-frequency close to that of the proposed VCO. At almost same carrier frequency, the proposed design shows better phase noise performance while consuming more power. It is worth mentioning that the value of supply leads to a significant difference in terms of power consumption since the dynamic power is proportional with the square of the voltage supply. Although the channel lengths of [20] and [24] are the same, [24] has superior FoM_1 because of using a low-noise delay cell. However, the employed delay element suffers from a narrow tuning range which leads to a VCO with only 36.2% TR_f under a tuning voltage of 0.5 V. On the other hand, its power dissipation and occupied area is more than the ones of [20] due to resistor-varactor structure. The structure in [15] has decent results in terms of FoM_1 and FoM_2 , but the narrow tuning frequency range makes it hardly

suitable for wide-band applications in the advanced CMOS technologies because the continues reduction of supply voltage forms a narrower frequency tuning range.

The proposed VCO achieves low power and small integration area compared with the designs introduced in the Table I. The average power consumption is 0.32 mW and the power dissipation at maximum oscillation frequency of 9.37 MHz is 0.903 mW. In spite of the high supply voltage and the long-channel technology whose power consumption is inferior, the proposed VCO shows almost full-range frequency tuning range with a tuning voltage up to 2.5 V and a F_oM_2 of -193.45 dBc/Hz, which at least 20 dB better than other designs listed in Table I. In addition, it shows linear voltage tuning range (TR_V), as defined hereinafter, while significantly outperforms conventional techniques on phase noise and F_oM_1 .

$$TR_V = \frac{V_{cont_{max}} - V_{cont_{min}}}{V_{DD}} (\%) \quad (26)$$

Therefore, the proposed VCO can be used as a low-noise ring VCO for low supply voltage and scaled-down technology.

Moreover, since the proposed design is a part of a time-domain comparator, its performance in terms of resolution is of great importance. The close-in and broadband phase noise affects the frequency resolution and overall system SNR [27]. If we suppose that other critical factor in TDC resolution such PFD's dead-zone behaves ideally, the magnitude of the jitter (or phase noise) contribution in a single full cycle of VCO's output signal can approximate the overall system resolution. From the measured jitter result of 17.64 ps the overall TDC resolution which exploited the proposed VCO can be estimated equal to 75.63 dB. This substantiates the capability of proposed VCO in realization of high-resolution TDC.

VI. CONCLUSION

We demonstrated in this paper the design and analysis of a low-noise, wide-tuning range ring-VCO were operating as part of a constituent block of an integrated readout sensor interface. The prototype was implemented in AMS-kit 0.35 μm CMOS technology under a 3.3 V supply voltage. The measured oscillation frequency range is from 0.01 to 9.37 MHz which brings about a 199.5% frequency tuning range over 2.5 V control voltage. At maximum frequency, the measured phase noise is -147.57 dBc/Hz at a 1-MHz offset frequency while the FoM of the proposed VCO is -168 dBc/Hz. The average power consumption of the proposed design is 0.32 mW while occupying a silicon area of $34 \mu\text{m} \times 161 \mu\text{m}$. Given the close match between the measured jitter and the prediction of the analytical model, we can assert that the main contributor of the VCO's phase noise comes from the uncorrelated flicker noise of the MOS transistors. The experimental results of the tuning range and figure of merits evidenced that the proposed VCO's performance can be preserved in the case of process scaling. Therefore, the proposed configuration allowed the realization of a compatible VCO structure with a wide range of analog/digital circuits requiring VCO such as time to digital converters, and functions. As well as various sensor interfaces for numerous applications.

ACKNOWLEDGMENT

The authors would like to thank the National Sciences and Engineering Research Council of Canada and MITACS for the financial support and CMC Microsystems for providing the design tools. Authors would like to thank Dr. Ahmad Hassan for his input to this manuscript.

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