A single D.C. link Multi-level 42-sided polygonal Voltage Space Vector Generation with lower order harmonic suppression using Switched-Capacitive filter

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Abstract—In this work, a multi-level 42-sided polygonal space vector structure (SVS) for suppression of lower order harmonics for Open-End Induction Motor(OEIM) drive applications is proposed. The proposed power circuit topology consists of two inverters feeding an Open-End Induction Motor from either side. The main inverter fed with a single DC link providing active power for motor operation is switched at low switching frequency. The secondary inverter fed with a capacitive supply is switched at high frequency to suppress lower order harmonics upto 39th order, up to the base speed of operation allowing maximum utilization of the DC link. The advantages of lower order harmonic suppression in motor phase voltage, for polygonal space vector structures are combined with multi-level inverter topology. This results in lower switching losses in low frequency switching main inverter and low voltage secondary inverter. Use of a single DC link facilitates four-quadrant operation of the inverter. The proposed scheme is validated for steady state and dynamic performance by experimental results.

Index Terms—Flying Capacitor, harmonic suppression, Induction Motor drives, polygonal Space Vector Structure, multilevel inverters, pulse width modulation(PWM).

I. INTRODUCTION

HIGH performance variable speed Induction Motor Drives present a unique design challenge. Optimizing various performance metrics like the inverter switching losses, lower order harmonics in phase voltage, dv/dt in the motor phase voltage, Electro-Magnetic Interference(EMI), switching stress in semiconductor switches, switch voltage ratings, etc. becomes essential. A conventional 2-level voltage source inverter operating at high switching frequency mitigates lower order harmonics in phase voltage but increases switching losses [1].

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Moreover, 2-level inverters lead to hexagonal space vector structures. At higher modulation index, the hexagonal space vector structure operates in over-modulation region generating lower order harmonics, despite having a high-switching frequency. Multi-level inverter topologies [1]–[4] offer attractive features like improved THD(Total Harmonic Distortion), and reduced dv/dt stress in the motor phase voltage. However, since conventional Multi-level inverter topologies also lead to hexagonal space vector structures, the problem of lower order harmonics in over-modulation region persists [2].

Different approaches have been proposed in literature to address the problem of lower order harmonics in motor phase voltage. The use of passive L-C filter proposed in [5], [6] results in bulky components, since the cut-off frequency of the filter needs to be lower than the harmonic frequencies. This results in a bulky system with increased cost. Another approach to tackle the problem, is by implementing sophisticated PWM (pulse-width modulation) schemes to selectively eliminate harmonics at a particular frequency. Selective-Harmonic Elimination (SHE) [7], [8] achieves the suppression of lower order harmonics by introducing notches in the motor phase voltage to suppress harmonics of a particular order. The drawback here is that, the computation of optimal notch width involves solutions of non-linear equations that must be computed offline and stored in the controller. Despite the complex offline computations, SHE algorithms cannot achieve suppression of lower order harmonics at full base speed. A split phase Induction motor for suppression of lower order harmonics has been proposed in [9] for suppression of lower order harmonics in torque ripple. In this method the harmonic flux components are canceled by the asymmetric motor phases, resulting in smooth torque profile. This method requires the use of specially designed asymmetric 6-phase Induction Motors. Due to the aforementioned limitations, suppression of lower order harmonics for variable speed induction motor drives continues to be a topic of active research.

The concept of higher sided polygonal Space Vector Structures (SVS) has been proposed in literature for suppression of lower order harmonics [10]–[15], that extend the linear modulation range close to the base speed of operation. For example, the Dodecagonal SVS proposed in [14] leads to suppression of $6 * k \pm 1$ order harmonics for odd values of

k . In general a p -sided polygonal space vector structure will have the presence of $k * p \pm 1$ order harmonics for positive integer values of k .

The authors have proposed a scheme for suppression of lower order harmonics using 42-sided polygonal Space Vector Structure (SVS) for induction motor drive applications in [10]. The work in [10] addresses most of the design challenges in the over-modulation region of operation. However, it creates a single layer of 42-sided SVS. In the present work, a multilevel structure with 21 concentric layers of 42-sided polygonal SVS is proposed for variable speed IM drive applications. Here also, Open End Induction Motor is used. The primary inverter topology is a 3-level Flying capacitor inverter, due to ease of capacitor voltage balancing using pole voltage redundancies as explained in [16], [17]. The secondary inverter is a dense 6-level topology, first proposed in [10]. The primary inverter operating with active DC link supply of V_{dc} is switched at low frequency to mitigate issues like EMI, dv/dt stress on switching devices. The secondary inverter operating at lower voltages is switched at higher frequencies to filter out the harmonics generated by the primary inverter.

II. POWER CIRCUIT TOPOLOGY

Fig. 1. Proposed Power Circuit Topology for generating the 21-concentric 42-sided Space Vector Structure.

The proposed power circuit topology is shown in Fig.1. The open-end Induction Motor (OEIM) is connected to inverters on either side. The primary inverter, fed with an active DC link supply of V_{dc} , provides all of the active power for motoring operation. The secondary inverter is fed with a Capacitive supply balanced at a nominal voltage of $0.39V_{dc}$ [10]. The secondary inverter absorbs the reactive power generated by the primary inverter resulting in suppression of lower order harmonics in motor phase voltage.

The active DC link fed primary inverter is operated at low switching frequency to minimize switching stress on switches with high voltage ratings. As a result the primary inverter generates lower order harmonics in the pole voltage. The Capacitor fed secondary inverter operating at lower voltages, is switched at high frequency to suppress the lower order harmonics generated by primary inverter. The space vectors generated by the superposition of primary and secondary space vectors, form a 42-sided polygonal space vector structure,

which is devoid of all lower order harmonics up to 39^{th} order harmonics, as explained in [10].

The primary 3-level inverter has a Flying-Capacitor in each phase, cascaded with DC link supply of V_{dc} . The primary FC inverter results in a 3-level hexagonal Space Vector Structure (SVS). The primary inverter SVS can be visualized as a combination of two independent 2-level hexagonal SVS of radius $V_{dc}/2$ operating in 6-step mode of operation. That is, the primary inverter space vectors can be generated by switching two active space vectors from 2-level SVS, and adding them as vectors, as illustrated in Fig.2. The addition of vectors is also illustrated in the figure.

Fig. 2. Primary inverter SVS visualized as a combination of two independent 2-level SVS of radius $V_{dc}/2$.

The zero vector can be generated by switching two 2-level vectors that are 180° out of phase ($\vec{V}_1$ and $\vec{V}_4$). If the 2-level vectors $\vec{V}_1$ and $\vec{V}_3$ with a phase difference of 120° are switched, their vector sum results in vector $\vec{OC}$, with an amplitude of $V_{dc}/2$.

$$V_{dc}/2 \angle 0^\circ + V_{dc}/2 \angle 120^\circ = V_{dc}/2 \angle 60^\circ$$

Similarly, vectors with phase differences of 60° ($\vec{V}_1$ and $\vec{V}_2$ in Fig.2) and 0° ($\vec{V}_1$ and $\vec{V}_1$) result in 3-level space vectors of amplitude $0.866V_{dc}$ ($\vec{OB}$) and V_{dc} ($\vec{OA}$), respectively.

$$V_{dc}/2 \angle 0^\circ + V_{dc}/2 \angle 60^\circ = 0.866V_{dc} \angle 30^\circ$$

$$V_{dc}/2 \angle 0^\circ + V_{dc}/2 \angle 120^\circ = V_{dc} \angle 0^\circ$$

Thus, any space vector of the primary inverter can be visualized as a combination of the two independent 2-level SVS of radius $V_{dc}/2$, operating in 6-step mode of operation. The individual 2-level SVS operating in 6-step mode of operation, will generate 5^{th} and 7^{th} order lower order harmonics in the primary pole voltage. The phase difference with which the two independent 2-level SVS are operated is used to control the fundamental component of motor phase voltage. The harmonics of the 2-level SVS are suppressed using secondary inverter space vectors, as explained in [10], to generate two independent 42-sided space vector structures.

The secondary inverter SVS is shown in Fig.3. The secondary inverter has a 2-level stage fed by a common capacitor supply, balanced at a nominal voltage of $0.39V_{dc}$, cascaded with a CHB stage balanced at $0.13V_{dc}$. Note that the CHB stage is balanced at one-third the voltage of the preceding 2-level stage. The 2-level stage generates a 2-level hexagonal SVS of radius $0.39V_{dc}$, whereas the CHB stage generates a 3-level SVS of radius $0.26V_{dc}$. The space vector structure of

Fig. 3. Secondary inverter SVS generated by combination of 2-level stage SVS of radius $0.39V_{dc}$ and CHB stage SVS of radius $0.26V_{dc}$.

the CHB stage can be superimposed on the capacitor-fed two level stage, to generate the combined 6-level secondary SVS. The asymmetric voltage levels of the two stages, lead to a dense SVS of radius $0.65V_{dc}$ for secondary inverter.

Fig. 4. Design of secondary Space Vector Structure for generating reference vectors at base speed of operation, with primary inverter operating in 6-step mode of operation.

At the base speed of operation, the primary inverter is operated in 6-step mode of operation and the reference vector lies on a 42-sided polygonal SVS. The 42-sided polygonal reference vector is generated by superposition of primary and secondary vectors. This requires that the radius of secondary SVS must be sufficiently large, so that the primary and secondary vectors can be superimposed to generate the reference space vector location (refer Fig.4). The largest secondary vector will be switched, for the reference vector of $V_{ref} = V_{dc} \angle 30^\circ$, as shown in Fig.4. To generate the reference vector, the primary vector $V_{pri} = V_{dc} \angle 0^\circ$ is switched. The secondary vector is generated by switch-averaging three secondary space vector locations, forming the triangle enclosing the tip of the secondary vector. The amplitude of the largest secondary space vector can be determined by the vector subtraction of reference space vector and primary vector.

$$\begin{aligned} |\vec{V}_{sec}|_{max} &= |\vec{V}_{ref} - \vec{V}_{pri}| \\ &= |V_{dc} \angle 30^\circ - V_{dc} \angle 0^\circ| \\ &= 0.52V_{dc} \end{aligned} \quad (1)$$

The radius of the secondary SVS is determined by the nominal voltages of the CHB stage capacitors and the common supply capacitor feeding the secondary inverter. If the CHB stage capacitors are balanced at a nominal voltage of $x * V_{dc}$, then the supply capacitor must be balance at $3x * V_{dc}$. The CHB stage and the 2-level stage, then have SVS of $2x * V_{dc}$ and $3x * V_{dc}$, respectively, leading to a combined secondary SVS then has a radius of $5x * V_{dc}$. The orientation of the secondary vector is not known. Since the secondary SVS is hexagonal, the worst case of 30° orientation with α -axis, is assumed for secondary vector. The largest secondary space vector with 30° orientation, that can be generated by the secondary SVS of radius $5x * V_{dc}$ will be $\cos(30^\circ)5x * V_{dc} = 4.33x * V_{dc}$. For the secondary SVS to generate a vector of $0.52V_{dc}$, it must satisfy the relation,

$$\begin{aligned} 4.33x * V_{dc} &\geq 0.52V_{dc} \\ \Rightarrow x &\geq 0.12 \end{aligned}$$

Based on the above design relations, secondary CHB stage and 2-level capacitor nominal voltages are selected to be $0.13V_{dc}$ and $0.39V_{dc}$, resulting in a secondary SVS of radius $0.65V_{dc}$.

III. GENERATION OF TWO INDEPENDENT 42-SIDED SPACE VECTOR STRUCTURES

This section explains the philosophy by which the two independent 42-sided Space Vector Structures are generated. The primary inverter is visualized as a combination of two independent 2-level SVS of radius $V_{dc}/2$, operating in 6-step mode of operation. To generate the 42-sided space vector, a secondary vector is superimposed on the primary vector. The secondary inverter SVS of radius $0.65V_{dc}$, is visualized as combination of two independent secondary vectors of half the radius. That is, for the two independent primary SVS of radius $V_{dc}/2$, there are corresponding two independent secondary SVS of radius $0.65V_{dc}/2$, each. Similar to Fig.4, the superposition of primary and secondary vectors is used to generate 42-sided polygonal Space Vector Structure. Since the secondary inverter is fed with a capacitive supply, it cannot deliver active power during motor operation. Thus, the 42-sided polygonal SVS operating in 42-stepped mode of operation, must generate the same fundamental phase voltage, as that generated by the primary hexagonal SVS of radius $V_{dc}/2$ operating in 6-step mode of operation. From Fourier analysis of 42-stepped and 6-stepped phase voltage waveforms, the corresponding fundamental components ($V_{fund,42-stepped}$ and $V_{fund,6-stepped}$) can be determined as,

$$\begin{aligned} V_{fund,6-stepped} &= 0.637V_{dc}/2 \\ V_{fund,42-stepped} &= 0.666V_{42} \end{aligned} \quad (2)$$

Where, V_{42} is the radius of the 42-sided polygonal SVS. The fundamental components in both cases, must be same,

since the secondary inverter cannot generate a fundamental component in phase voltage. Thus,

$$\begin{aligned} V_{fund,42-stepped} &= V_{fund,6-stepped} \\ \Rightarrow 0.666V_{42} &= 0.637V_{dc}/2 \\ \Rightarrow V_{42} &= 0.478V_{dc} \end{aligned} \quad (3)$$

Fig. 5. Generation of two independent 42-sided SVS using two independent 2-level SVS from primary inverter of radius $V_{dc}/2$, superimposed with secondary vectors.

The two independent 42-sided SVS are generated by superposition of the primary and secondary space vectors. The secondary space vectors are given by,

$$\vec{V}_{sec} = \vec{V}_{ref} - \vec{V}_{pri}$$

If the secondary space vectors are maintained at this value, assuming ideal conditions, secondary inverter provides only reactive power, and the capacitor voltages will be maintained at their nominal values. The primary SVS of radius $V_{dc}/2$ operating in 6-step mode of operation generates lower order harmonics in the pole voltage. These harmonics are suppressed by the secondary inverter by generating the 42-sided polygonal SVS. The resultant two independent 42-sided SVS are devoid of any lower order harmonics. The two independent 42-sided polygonal Space Vector Structures are combined to generate the 21-concentric, 42-sided SVS in the next section.

IV. GENERATION OF 21 CONCENTRIC LAYERS

The two independent 42-sided SVS of radius $0.478V_{dc}$ can be combined by vector addition. Each of the two independent SVS consists of identical set of 42 space vectors. Since the two independent SVS consist of identical set of vectors, so the two vectors switched from these SVS can either be *collinear* or *non-collinear*. Say the vectors switched from two independent SVS are $\vec{O}_{p1}\vec{X}$ and $\vec{O}_{p2}\vec{Y}$, where X and Y are integers between 1 and 42 (refer Fig.6). Then, if $\vec{O}_{p1}\vec{X} = \vec{O}_{p2}\vec{Y}$, it is said that collinear vectors are switched from the two independent SVS, otherwise the two vectors are said to be non-collinear. There are $^{42}C_2 = 42 * 41/2$ different ways in which a pair of *non-collinear* vectors can be selected from the two independent SVS. Of these, $^{42}C_2$ pairs of vectors, there are 21 pairs of vectors for which the sum results in zero vector, as the selected vectors are opposite in phase. Similarly, there $^{42}C_1 = 42$ pairs of *collinear* vectors. Thus,

by combining the two independent 42-sided SVS, a total of $^{42}C_2 - 21 + ^{42}C_1$ vectors can be generated. On simplifying, the number of vectors can be expressed as $21 * 42$. The set of vectors can be grouped into 21 concentric layers of 42-sided polygonal space vectors as shown in Fig.6.

Fig. 6. Generation of the 21 concentric 42-sided polygonal SVS using a combination of two independent 42-sided SVS

If *collinear* vectors are selected from the two independent 42-sided SVS, the vectors add in-phase, and the vector sum results in a 42-sided polygonal layer of radius $0.478V_{dc} + 0.478V_{dc} = 0.956V_{dc}$. In general, two *non-collinear* vectors with a phase difference of $\phi = k * 360^\circ/42$, can be selected from the two independent SVS. The vector addition of these vectors results in 42-sided polygonal layer of radius $0.478V_{dc}\cos(\phi/2) + 0.478V_{dc}\cos(\phi/2) = 0.956V_{dc}\cos(\phi/2)$. Substituting ϕ , the radii of 21-concentric layers is of the form,

$$R_k = 0.956V_{dc}\cos(k * 4.3^\circ) \quad (4)$$

Where, R_k is the radius of k^{th} concentric 42-sided layer and k is an integer between 0 to 20.

Fig. 7. Generation of sampled reference space vector using 21 Concentric 42-sided Space Vector Structure.

The resulting 21-concentric 42-sided dense Space Vector Structure is illustrated in Fig.7. A section of the SVS is cut out and enlarged to show the PWM scheme. The 21-concentric SVS is composed of polygons with 0° (for even values of k) and $360^\circ/42/2 = 4.3^\circ$ (for odd values of k) orientation with respect to α -axis. As a result, the SVS can be segregated into symmetric isosceles triangular regions. The sampled rotating reference vector lies inside a triangular region, that is marked in the figure. To identify the triangular region inside which the reference vector lies, the magnitude and phase of the reference

vector are used, which are derived from the speed control loop for Induction Motor control. The magnitude and phase of the reference vector for the example considered in Fig.7, are $0.68V_{dc}$ and 7.3° , respectively.

The first step is to identify the two adjacent concentric layers, between which the reference vector lies. The adjacent layers can be identified by comparing the magnitude of reference vector with the radii of the concentric layers. In this example, the magnitude of reference vector $0.68V_{dc}$, lies between concentric layers 10 and 11, whose radii, R_{10} and R_{11} , evaluated using Equation.4, are given by,

$$R_{10} = 0.956V_{dc}\cos(10 * 4.3^\circ) = 0.7V_{dc}$$

$$R_{11} = 0.956V_{dc}\cos(11 * 4.3^\circ) = 0.65V_{dc}$$

Since, the magnitude of reference vector $0.68V_{dc}$, satisfies the relation $R_{11} = 0.65V_{dc} \leq 0.68V_{dc} \leq R_{10} = 0.7V_{dc}$, the two adjacent concentric layers are layers 10 and 11.

The second step is to identify the specific vectors in layers 10 and 11 (vector $\vec{V}_0$, $\vec{V}_1$, $\vec{V}_2$ and $\vec{V}_3$ in Fig.7), that are adjacent to reference vector, using the phase of the reference vector. The phase of reference vector is $\theta_{ref} = 7.3^\circ$, as shown in Fig.7. The layer 10 forms a 42-sided polygon aligned at 0° with α -axis, so that the polygonal vectors of layer 10 have a phase of $\theta_{10} = \lambda_{10} * 360^\circ/42$ (where, λ_{10} is integer between 0 to 42). Whereas, layer 11 forms a 42-sided polygon aligned at 4.3° with α -axis, so that the polygonal vectors of layer 11 have a phase of $\theta_{11} = 4.3^\circ + \lambda_{11} * 360^\circ/42$ (where, λ_{11} is integer between 0 to 42). The values of λ_{10} , that result in adjacent vectors are given by,

$$\lambda_{10} = \text{ceil}(\theta_{ref} * 42/360^\circ) = 1$$

$$\lambda_{10} = \text{floor}(\theta_{ref} * 42/360^\circ) = 0$$

Where the *ceil* function returns the smallest integer value that is bigger than or equal to a number (i.e, rounds "up" to the nearest integer); whereas the *floor* function returns the largest integer that is smaller than or equal to a number (i.e, rounds "down" to the nearest integer). Thus, the phase of layer 10 adjacent vectors is given by $1 * 360^\circ/42 = 8.6^\circ$ and $0 * 360^\circ/42 = 0^\circ$. The layer 10 vectors are marked as $\vec{V}_2$ and $\vec{V}_3$, respectively, in Fig.7. Similarly, the values of λ_{11} , that result in adjacent vectors are given by,

$$\lambda_{11} = \text{ceil}((\theta_{ref} - 4.3^\circ) * 42/360^\circ) = 1$$

$$\lambda_{11} = \text{floor}((\theta_{ref} - 4.3^\circ) * 42/360^\circ) = 0$$

Thus, the phase of layer 11 adjacent vectors is given by $4.3^\circ + 1 * 360^\circ/42 = 12.86^\circ$ and $4.3^\circ + 0 * 360^\circ/42 = 4.3^\circ$. The layer 11 vectors are marked as $\vec{V}_0$ and $\vec{V}_1$, respectively, in Fig.7.

The third step is to identify the triangular region in which the reference vector lies. The search so far has narrowed down the reference vector to the quadrilateral formed by vectors $\vec{V}_0$, $\vec{V}_1$, $\vec{V}_3$ and $\vec{V}_2$. The quadrilateral can be further split into 2 triangular regions marked as Region.I and Region.II in Fig.7. An assumption is made in this step, that the reference vector lies in one of the regions (either Region.I or Region.II), and

the timing of polygonal vectors to satisfy volt-sec balance is calculated, for that region. If the assumption of region is incorrect, the timing calculations for timings T_a , T_b and T_c , give negative values for one or more of the timings(T_a , T_b or T_c), indicating that the assumption was incorrect. For instance, it can be assumed that the reference vector lies in Region.II. The reference vector is generated by switch averaging of vectors $\vec{V}_3$, $\vec{V}_1$ and $\vec{V}_2$ for timing T_3 , T_1 and T_2 . The timings are calculated to satisfy the volt-sec relations given by,

$$T_{sw} * \vec{V}_{ref} = T_1 * \vec{V}_1 + T_2 * \vec{V}_2 + T_3 * \vec{V}_3$$

The timings that satisfy the volt-sec relations are $T_1 = 0.395T_{sw}$, $T_2 = 0.644T_{sw}$ and $T_3 = -0.039 * T_{sw}$. Thus, the initial assumption about the reference being in Region.II is incorrect. The timing for Region.I can be calculated to satisfy the volt-sec relation,

$$T_{sw} * \vec{V}_{ref} = T_0 * \vec{V}_0 + T_1 * \vec{V}_1 + T_2 * \vec{V}_2$$

The reference vector can now be generated by switched-averaging the vectors $\vec{V}_0$, $\vec{V}_1$, $\vec{V}_2$, that lie at the vertices of the triangular Region.I. The corresponding timings to satisfy the volt-sec relations, are $T_0 = 0.0393T_{sw}$, $T_1 = 0.35T_{sw}$ and $T_2 = 0.611T_{sw}$. Once the polygonal space vector locations and their corresponding timings are determined, the reference vector can be generated by PWM switching of polygonal space vector locations. The space vector locations for the 21 Concentric, 42-sided polygonal space vector structure are stored in the TMS320F28335 DSP platform.

The rotating sampled reference space vector is obtained from the speed loop for Induction motor control. The reference vector amplitude varies depending on the reference speed. The proposed scheme generates reference vector for the speed reference, by adjusting the phase difference with which the two independent 42-sided polygonal SVS are operated, to generate the reference vector of desired amplitude. The experimental results for the the motor operation are shown in later section.

V. CAPACITOR BALANCING SCHEME

In the discussion thus far, it has been assumed that the capacitor voltages are balanced close to their nominal voltages during inverter operation. In practice however, the capacitors may discharge or over-charge due to the currents flowing in or out of capacitor during inverter operation or due to circuit non-idealities. Thus, it is important to sense capacitor voltages and implement algorithms that would correct for any deviations in the capacitor voltages from their nominal values. In the power circuit topology illustrated in Fig.1, the capacitor of FC stage in primary inverter, the capacitors of CHB stage in secondary inverter and the common capacitive supply of secondary inverter require the use of capacitor balancing schemes.

The primary inverter FC stage capacitors are balanced at a nominal voltage of $V_{dc}/2$, with the help of pole voltage redundancies as described in [16], [17]. The FC stage capacitors are bypassed when the primary pole voltage is switched to 0 or V_{dc} . To generate a pole voltage of $V_{dc}/2$, there are two possible

switch states. One of the switching states leads to charging and the other leads to discharging of the capacitor voltage depending on the direction of phase current. By sensing the capacitor voltage, the deviation from the nominal voltage is determined, and a suitable switching stage is selected to reduce the deviation in capacitor voltage.

The secondary inverter topology presented in Fig.1 is first proposed in [10], where the balancing scheme for CHB stage is explained in detail. The CHB stage capacitor voltages are balanced at their nominal voltages within one switching cycle by using space vector redundancies. The balancing scheme for secondary inverter is explained here with an example.

Fig. 8. Space Vector Redundancies for capacitor Voltage Balancing Scheme of CHB stage.

Fig.8 illustrates the balancing scheme for CHB stage capacitor voltages for the case when $\vec{V}_{sec}$ is switched from secondary inverter. The CHB stage voltages for each of the redundancies are different and hence the charging/discharging of CHB stage capacitors is different, so the CHB stage voltages for redundancies are assigned switching stage codes to track the capacitor charging/discharging states. The CHB stage can contribute a voltage of $0.13V_{dc}$, 0 or $-0.13V_{dc}$ to the pole voltage. The voltages are assigned switching state codes of 1, 0, -1, respectively. Similarly, the two level stage pole voltage of $0.39V_{dc}$ or 0 are assigned switching state codes of 1 and 0, respectively.

The space vector redundancies for $\vec{V}_{sec}$ are illustrated in the figure. The secondary vector $\vec{V}_{sec}$ can be realized using any of the three redundancies shown in Fig.8. As illustrated in figure, the first redundancy of $\vec{V}_{sec}$ is generated by superposition of the 2-level stage vector of $0.39V_{dc}\angle 0^\circ$ and the CHB stage vector of $-0.13V_{dc}\angle 0^\circ$. The vectors correspond to the switching state codes of [3,0,0] and [-1,0,0] for the secondary 2-level and CHB stage respectively. Similarly, the other two stages can be assigned the switching state codes of [0,1,1] and [1,-1,-1] in the CHB stage, and switching state codes of [3,0,0] and [0,0,0] in the 2-level stage. The switching state codes of the three redundancies are collected for all vector redundancies are tabulated in Table.I below.

Note that the A-phase CHB stage codes for redundancy (a) and redundancy (c) are opposite (-1 and 1). Thus, to balance the CHB stage capacitor in A-phase, redundancy a and redundancy (c) must be employed for equal timings. Following a similar argument for B and C-phase CHB capacitors, it can be deduced that if the three redundancies are employed for equal timings, then the capacitor voltages for all phases in CHB stage remain undisturbed during the inverter operation.

TABLE I
SWITCHING STATE CODES FOR THE REDUNDANCIES OF SECONDARY INVERTER SPACE VECTOR.

Redundancy	CHB stage space vector	secondary 2-level space vector
(a)	[-1,0,0]	[3,0,0]
(b)	[0,1,1]	[3,0,0]
(c)	[1,-1,-1]	[0,0,0]

Further details of the secondary inverter capacitor balancing schemes can be found in [10].

The 2-level common capacitor feeding the secondary inverter is balanced at it's nominal voltage by exploiting the power relations between the primary inverter and the motor load. By modifying the PWM scheme for secondary inverter alone, the power delivered to the motor load can be decreased (or increased), without disturbing the power drawn from the primary inverter. As a result the excess power (primary power - motor load power) is delivered to the secondary inverter common capacitor to increase (or decrease) the capacitor voltage. This relationship can be exploited to maintain the secondary inverter supply capacitor voltage at it's nominal value. Consider the condition that the voltage of secondary inverter supply capacitor is discharged slightly, and is below it's nominal value. To charge the secondary capacitor, power must be supplied to the secondary inverter. Since the PWM of primary inverter is not disturbed, the power drawn from primary inverter, P_{pri} is not disturbed. To reduce the power delivered to the motor load, the motor phase voltage is reduced, by reducing the amplitude of the reference space vector. To reduce the reference vector, primary inverter PWM is not disturbed, and only the secondary inverter space vectors are modified.

As a result, the resultant space vector and the phase voltage applied to the motor load reduce momentarily, and hence the power delivered to motor load, P_{load} is less than P_{pri} . Since the secondary inverter PWM pattern will change due to this correction, the excess power will be fed to the secondary inverter to charge the supply capacitor. Thus, a corrective strategy is proposed to sense the secondary inverter supply capacitor and balance it close to it's nominal voltage during inverter operation. More details for the capacitor balancing scheme of secondary inverter supply capacitor can be found in [10].

VI. EXPERIMENTAL RESULTS

The proposed scheme is implemented and experimentally verified using a laboratory prototype. A 4-pole, 2kW, 415V, 50Hz, 3-phase Open End Induction Motor is used in experiments. The control algorithm is implemented on Texas Instruments' TMS320F28335 DSP platform. The Xilinx Spartan-XC3S200 FPGA platform is used in conjunction with the DSP to propagate the PWM signals inverter gate drivers. SKM75GB12T4 half-bridge modules are used to realize inverter switches.

Fig.10 illustrates a functional block diagram of the proposed scheme. The proposed control scheme is implemented in the

Fig. 9. Experimental steady-state results. (a)-(d) waveforms for A-phase: (1) Motor phase voltage, (2) Primary pole voltage, (3) Secondary pole voltage, (4) Motor phase current; (e) waveforms for A-phase: (1) FC stage capacitor voltage, (2) secondary supply capacitor voltage, (3) CHB stage capacitor voltage, (4) Motor phase current; (f) FFT results for: (1) Primary inverter pole voltage, (2) Secondary inverter pole voltage, (3) Phase voltage.

Fig. 10. Functional Block Diagram of the hardware implementation.

DSP platform. A speed encoder is employed to provide the mechanical speed feedback for the closed loop Field Oriented Control (FOC) scheme. The capacitor voltages and phase currents are sensed and fed to the ADC channels of the DSP for the capacitor voltage balancing schemes described in the work.

The results for the Open-End Induction Motor operation in steady state are presented in Fig.9. Fig.9(a)-(d) present the steady state waveforms of motor phase voltage, primary pole voltage, secondary pole voltage, and motor phase current for 5Hz, 30Hz, 40Hz and 50Hz frequency of operation. It can be observed from the primary pole voltage waveform, that the phase voltage generated by the primary inverter, increases with increasing frequency of operation. The fundamental motor phase voltage generated by the primary inverter alone can also be observed to increase proportionally. The secondary inverter operates to suppress the lower order harmonics in motor phase voltage for smooth operation. The phase current can be observed to be a sinusoidal waveform, since the lower

order harmonics are completely suppressed in the motor phase voltage. Fig.9(e), shows the capacitor voltages of FC stage, CHB stage in A-phase, and the secondary supply capacitor voltage during steady state operation at 50Hz. The capacitor voltages are tightly controlled close to their nominal voltages. Fig.9(f) presents the FFT of the primary pole voltage, secondary pole voltage and the motor phase voltage. The lower order harmonics in the primary and secondary inverters, are identical in amplitude, and cancel out in the motor phase voltage, resulting in smooth motor operation.

The experimental results for dynamic performance of the proposed drive scheme are presented in Fig.11. In Fig.11(a), the motor speed, $d-q$ currents and motor phase current are presented. The frequency of operation is changed from -30Hz to 30Hz. In steady state, torque producing part of the current, $I_{s,q}$, is close to zero for no load operation. As the reference speed for the drive is changed from -30Hz to 30Hz, $I_{s,q}$ increases from zero and saturates to its maximum limit. As the mechanical speed approaches 30Hz, $I_{s,q}$ is reduced to zero again. Fig.11(b) presents the motor phase voltage along with $d-q$ and motor phase currents. The motor phase voltage is reduced in amplitude initially, to change the motor speed from -30Hz to 0Hz. Thereafter, the motor phase voltage amplitude is increased again to energize the motor to 30Hz of operation. Fig.11(c), shows the capacitor voltages of FC stage, CHB stage in A-phase, and the secondary supply capacitor voltage during speed reversal from -30Hz to 30Hz. It can be observed that the capacitor voltages are tightly controlled close to their nominal voltages through out the dynamic operation of the motor.

VII. CONCLUSION

In this work, a multi-level 42-sided polygonal Space Vector Structure for Open-End Induction Motor drive applications is proposed. A 42-sided polygonal SVS leads to suppression of all lower order harmonics, up to 39th order harmonic,

Fig. 11. Experimental results for speed reversal from -30Hz to 30Hz under Field Oriented Control: (a) Traces: (1) Motor speed, (2) d -axis component of phase current, (3) q -axis component of phase current, (4) Motor phase current; (b) Traces: (1) Phase voltage, (2) d -axis component of phase current, (3) q -axis component of phase current, (4) Motor phase current; (c) Traces: (1) FC stage capacitor voltage, (2) secondary supply capacitor voltage, (3) CHB stage capacitor voltage, (4) Motor phase current.

in the motor phase voltage. The advantages of lower order harmonic suppression are extended to full base speed of operation, where power delivering primary inverter, operates in six-step mode of operation. The lower order harmonics generated by the primary inverter operation, are suppressed by employing a secondary inverter with capacitive supply. At the full base speed, the switching losses of the primary inverter, are significantly reduced. The low voltage secondary inverter, is switched at high frequencies for suppression of lower order harmonics. The proposed scheme, takes advantage of the low switching in primary inverter, and lower voltages in secondary inverter to reduce the switching losses during inverter operation, improving overall efficiency. The advantages are retained for lower modulation index, by visualizing the SVS of the proposed scheme as two independent 42-sided SVS operating in the extreme case of over-modulation. To generate a lower amplitude, the two independent SVS are operated with corresponding phase shift. The proposed scheme is verified for steady state and dynamic operation by conducting speed reversal under Field Oriented Control. The lower losses in primary inverter are evident from the waveforms of the primary inverter pole voltage, thus verifying the efficiency of the proposed scheme.

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