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Accurate High Frequency Modelling of the Input Admittance of PWM Grid-Connected VSCs

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Abstract—This paper addresses high frequency admittance modelling of current-controlled voltage source converters (VSCs). Recent studies have shown that harmonic instability may also occur at frequencies above the Nyquist frequency. To form an accurate multiple-frequency model in this frequency range, sidebands that originate from modulation and sampling must be examined. In this paper, an accurate small-signal model is developed taking into account an adequate digital pulse-width modulator (DPWM) representation, which allows to predict dependence of the frequency response on the steady-state DC (SS-DC) operating point. It is shown that, when center-pulse sampling is implemented, PWM sidebands do not create additional loops leaving only sampling sidebands to be considered. Using the same approach as for SS-DC operation, a model which accurately represents admittance measurements during sinusoidal AC (S-AC) operation is developed. Its basis is a novel DPWM model suitable for S-AC regime, which allows to predict dependence of the VSC's input admittance on the grid voltage magnitude. Experimental and simulated admittance measurements, performed on a single-phase two-level VSC during various SS-DC and S-AC regimes, show an excellent match with the proposed models up to twice the sampling frequency.

Index Terms—Admittance measurements, multiple-frequency model, passivity, sideband harmonics, voltage-source converters (VSCs)

I. INTRODUCTION

CONSIDERABLE growth in the number of grid-connected voltage source converters (VSC) in contemporary power systems has brought in harmonic instability issues [1]–[3]. Depending on the root cause of the harmonic instability, affected frequency range might be below and above fundamental frequency [1]. At higher frequencies, which are the focus of this article, destabilization of poorly damped grid resonances is a consequence of current control loop dynamics in presence of delays, such as those caused by sampling, computation and modulation [1], [4], [5]. Contributing to the phenomenon are also the sampling and pulse-width modulation (PWM) sidebands [1], [4], [6]–[8].

Originating from the impedance based stability approach [9], [10], passivity oriented controller design for VSCs has recently drawn significant attention [8], [11]–[13]. Even though an upper frequency limit for passivity compliance is not clearly defined even by traction standards [14], it is usually considered to be the Nyquist frequency (NF) [11]. However, recent studies have shown that harmonic instability may also be caused by resonances above the NF [4], [6]–[8].

These observations have motivated extensive research in the field of high frequency admittance modelling. Several approaches have been proposed, with the differences between

them being the small-signal modeling of the digital pulse-width modulator (DPWM), its generation of sidebands, and the modelling of aliasing due to the sampling process [4], [6], [7], [15]. In [4] a multiple-frequency model is developed which takes all sampling sidebands into account, but none of those originating from PWM. Certain discrepancies are observed between simulated admittance frequency response (FR) and the proposed model, due to incomplete DPWM representation. In [4], as well as in most of the works on this topic, DPWM is modelled as a zero-order-hold (ZOH). However, it is well-known that this is not a precise small-signal model [5]. In [16], [17], a small-signal model of DPWM is derived using the describing function approach. The resulting model is dependent on the steady-state operating point (SSOP), unlike the ZOH. Using [4] as a basis, in [6] authors develop a multivariable model that results in the matrix representation of the VSC admittance. Admittance measurements (AM) are provided, but some mismatch with the proposed model is observed. Contrary to [4] and [6] where only sampling sidebands are considered, the model presented in [15] and [18] considers only the lowest-order PWM sideband. In [18] it is reported that, around NF, this sideband causes the admittance to depend on the grid voltage magnitude, which models from [4] and [6] fail to predict. However, neither [15] nor [18] provide a clear comparison between the proposed model and AM. Authors in [7] sought to include sideband influence from both sampling and PWM, but again assumed the ZOH model of DPWM and limited the analysis to the lowest-order sidebands. As an alternative to the previously described continuous time domain modelling, intersample modelling is proposed in [19], again considering the DPWM dynamics equal to ZOH.

To fill in the gaps of previous research, this paper aims to provide a systematic approach for high frequency admittance modeling of digitally controlled VSCs. An impact of operating point (OP) on AMs is revealed, which has not been previously examined nor properly analyzed. It is shown that FR obtained during sinusoidal AC (S-AC) operation lies somewhere in-between FRs obtained during steady-state DC (SS-DC) regimes within the same OP range. An accurate high frequency model during SS-DC operation is thus considered to be a prerequisite for admittance modeling of grid-tied VSCs during S-AC regime. A simple, SSOP dependent, small-signal model for current-controlled VSC's is derived. Its key features are the accurate small-signal DPWM model from [16], the sampling sideband modelling from [4] and an observation that center-pulse sampling [5] removes the need for considering the PWM sidebands. Experimental AMs, performed on single-phase,

two-level, VSC with an inductive filter show an excellent agreement with the proposed small-signal model up to the sampling frequency (SF). Previously reported models [4], [11] and the model derived in this paper are also compared against simulated AMs all the way up to twice the SF, to show the superiority of the proposed approach. The last contribution of this paper is a simple, but accurate, model which predicts AM during S-AC operation, as prescribed e.g. in the traction standard [14]. It is developed using the proposed small-signal model as a basis. Key advantage of the proposed model is its ability to predict AM even above the SF, as well as the dependency on the magnitude of the AC voltage at the point of common coupling (PCC). The model is verified using experimental AMs up to the SF, and simulated AMs up to twice the SF. Comparison with previously used models is shown to highlight the obtained advantages.

This paper is organized as follows. Influence of OP on AMs is revealed in Section II. An accurate small-signal model for current-controlled VSC is derived in Section III and compared to the existing models. The model which predicts AM during S-AC operation is presented in Section IV and benchmarked against state-of-the-art models. Experimental AMs, performed during different SS-DC and S-AC regimes of the VSC, are provided in Section V. Conclusions and summary of the manuscript are given in Section VI.

II. INFLUENCE OF OPERATING POINT ON ADMITTANCE MEASUREMENTS

A. System description

Throughout this paper a digitally-controlled, pulse-width modulated, single-phase, two-level, grid-following VSC with an inductive filter is considered. Nevertheless, the presented approach is directly applicable to the analysis of three-phase grid-connected VSCs in stationary reference frame, as well as to any output filter.

A block diagram of the system considered is shown in Fig. 1 a). The system is current-controlled, with the control period T_s being half the switching period T_{pwm} , i.e. double-update rate is used [5]. Transition from continuous to digital domain is performed by an analog-to-digital converter (ADC). The current sampling instant is synchronized with the carrier w so that center-pulse (synchronous) sampling [5] is obtained, as illustrated in Fig. 2. This removes the switching ripple from the current i and results in its average value. The sampled current i_s is subtracted from the reference i_r , resulting in the error signal e that is used as an input to the current controller G_c . Due to finite algorithm execution time, the controller output update is delayed by one sampling period [5]. Voltage reference generated by the current controller is scaled to the range $[0, 1]$ to obtain the digital modulating signal m_s . The DPWM serves as an interface between digital and continuous domains. Its inherent ZOH function transforms m_s to m and compares it with the carrier w . The DPWM output, i.e. switching waveform x , is used to control the power transistors within the VSC. The output voltage of the VSC, v_o , is applied to the output filter G_l :

$$G_l(s) = \frac{i(s)}{v_o(s)} = \frac{1}{sL}, \quad (1)$$

where L is the filter inductance and s is the complex variable of the Laplace transform.

B. Admittance Passivity Criterion

The impedance-based approach has proven to be adequate for small-signal stability assessment of systems containing numerous power electronic devices [10]. For current-controlled systems, this method assumes representing the converter by its Norton equivalent circuit, which consists of a current source i_N paralleled with an admittance Y , as shown in Fig. 1 b) [9]. The elements of the Norton equivalent circuit can be found from a small-signal representation of the system, such as in Fig. 1 c), where G_d and G_{dpwm} model the computational delay and the digital modulation, respectively. The current source and admittance are defined by $i_N(s) = i(s)/i_r(s)|_{v_{pcc}(s)=0}$ and $Y(s) = -i(s)/v_{pcc}(s)|_{i_r(s)=0}$.

Under the assumption that current-controlled VSC is stable when connected to an ideal grid, stability of the system is determined by applying Nyquist stability criterion to the product of the VSC admittance and the grid impedance, i.e. to the minor-loop gain [9].

Relying on the impedance stability approach, admittance passivity criterion implies that, if the grid impedance Z_g is passive, a sufficient condition for system stability is that converter's admittance Y is also passive [12]. Note that a linear single-input single-output (SISO) system is considered to be passive if the real part of its FR is non-negative for all frequencies, i.e. if its phase is within the range $[-\frac{\pi}{2}, \frac{\pi}{2}]$ [11].

C. Admittance Measurements for Passivity Compliance

Admittance passivity criterion has inspired passivity related grid-connection requirements to be imposed in recent traction standards [14]. The EN 50388-2 standard [14], which is imposed in railway systems of several European countries, requires the VSC admittance to be measured while being connected to an AC source, i.e. while generating fundamental frequency voltages at its output. Waveforms of interest are to be acquired for a time interval equal to 8 or more multiples of the fundamental periods. This approach may bring to misleading conclusions, due to non-linear nature of certain elements in the current control loop. The main non-linearity comes from DPWM itself, because its small-signal input-output relation depends on the duty cycle, i.e. on SSOP [16]. The result of this is that in SS-DC regime, FR of the system depends on the SSOP for which AM is performed. As a consequence, when the system is operating in AC regime, where the fundamental frequency is considerably smaller than the switching frequency, influence of all OPs spanned during each fundamental period is present. In the following subsection, the impact of the OP on AMs is showcased providing simulation results. The necessity for the clear definition of the OP for which the VSC admittance should be measured is emphasized.

D. Comparison between AM during SS-DC and S-AC regime

For the following validations, simulations were performed in MATLAB Simulink environment, with a full-bridge VSC,

Fig. 1: Digitally controlled, pulse-width modulated, single-phase, two-level grid-following VSC: a) system block diagram; b) Norton equivalent circuit used for impedance-based stability analysis; c) single-frequency small-signal representation of the current control loop.

Fig. 2: Synchronization between current sampling instant and switching carrier w to obtain average value of the current i . Sampling is performed at peaks and valleys of w , ideally corresponding to the center of the applied voltage pulse.

operated using the bipolar modulation and described in Table I. AMs during different SS-DC regimes, i.e. for different duty cycles D , as well as during different S-AC regimes are performed. Each S-AC regime is defined by the peak-peak value of the duty cycle's fundamental frequency variation u_{pp} . AMs are performed by applying sinusoidal voltage perturbation at PCC and measuring the current response. For AMs during SS-DC operation, a DC source is connected in series with the perturbing source and its magnitude V_g is set depending on the desired OP, i.e. as $V_g = (2D - 1)E$. For AMs during S-AC operation a sinusoidal AC source with $f_1 = 50$ Hz is connected in series with the perturbing source, and its magnitude V_g is set depending on the desired u_{pp} , as $V_g = u_{pp}E$.

Perturbation generation, as well as post-processing of i and v_{pcc} to obtain the admittance FR is performed using FR Estimation block in Simulink. Sinestream experiment mode is used with the perturbation frequencies from the range [6, 80] kHz, whereas perturbation around multiples of switching frequency is avoided. Note that perturbation frequencies are chosen to be multiples of 25 Hz but not of 50 Hz, to minimize the impact of non-linear effects related to fundamental fre-

quency operation [6]. A fixed voltage perturbation magnitude of 50 V is used, to obtain high-enough magnitude of the perturbation current flowing through VSC. Fixed settling and estimation periods equal to 20 ms and 40 ms, respectively, are used. The estimation time was set lower than 8 times the fundamental period, due to data length and simulation time. Note that this does not compromise the measurement precision, as the window length is equal to an integer multiple of each perturbation frequency. A sufficient DC bias current reference is also imposed to avoid zero crossings which are reported to cause non-linear effects related to dead-times [20]. Note that DC component of the inductor current has no influence on AMs in the frequency range of interest.

As an application example, proportional resonant (PR) controller is used in this paper [21]. Its s domain transfer function is:

$$G_c(s) = \frac{v_r(s)}{e(s)} = k_p + k_r \frac{s}{s^2 + \omega_1^2}, \quad (2)$$

where k_p and k_r are proportional and resonant gains, respectively, and ω_1 is the fundamental angular frequency. The proportional gain is set as $k_p = \omega_c L$, where ω_c is the desired angular crossover frequency of the current loop [5]. The resonant gain k_r is designed so that its influence on crossover frequency is negligible [5], e.g. $k_r = \frac{1}{10}k_p$. The desired crossover frequency f_c is set depending on required stability margin. In typical double-update applications, due to delays, the crossover frequency is usually limited to 10% of the SF [11].

In order to illustrate that during S-AC operation all OPs, throughout which the system goes have an impact on AM, results for a S-AC and many SS-DC regimes, covering the same range of D , are shown in Fig. 3. Note that in this, as well as in all other figures presented in this paper, dots represent AM points. AM during S-AC operation is obtained for $u_{pp} = 0.8$, which corresponds to the nominal PCC voltage from Table I. AMs for SS-DC regimes are performed for duty cycles calculated as the arithmetic sequence starting from $0.5 - u_{pp}/2 = 0.1$ and ending at $0.5 + u_{pp}/2 = 0.9$. According

TABLE I: VSC and control loop parameters

VSC	label	value	unit
Nominal power	P_n	3	kW
Nominal DC link voltage	E	400	V
Nominal PCC voltage	V_g^{rms}	230	V
Filter inductance	L	2.5	mH
Fundamental frequency	f_1	50	Hz
Switching frequency	f_{pwm}	20	kHz
Dead-time	$\frac{t_{dt}}{T_{pwm}}$	1	%
Control loop	label	value	unit
Sampling frequency	f_s	40	kHz
Crossover frequency	f_c	4	kHz

Fig. 3: Comparison between AM during S-AC regime with $u_{pp} = 0.8$ (red plot) and multiple AMs during SS-DC regimes for the same duty cycle variation range (gradient from blue to yellow). The gray vertical line marks the NF.

to the presented results, AM during S-AC operation is a sort of average of AMs during SS-DC regimes for the same duty cycle variation range. Therefore, to analytically predict AM during S-AC operation, an accurate small-signal model for SS-DC regimes is considered to be a prerequisite. Development of such model is addressed in the following section.

III. SMALL-SIGNAL MODELLING OF VSCs

In this section, an accurate small-signal model of the system from Fig. 1 a) is derived. Modelling is performed in s domain [5], as effects above NF are the main focus of the paper.

A. DPWM model

Compared to the analog implementation, uniformly-sampled PWM introduces delay [5]. The phase lag due to modulation is shown to be equal to that of a pure time delay of $T_s/2$ [5]. Therefore, DPWM is often modelled as a pure delay [12]. For the purposes of predicting the system behavior at frequencies considerably below the NF, this model is sufficient [12]. However, to analyze behaviour near and above NF, a more accurate small-signal model is required, which accounts for magnitude attenuation at higher frequencies [4]. Motivated by the fact that sample and hold function is an inherent part

of DPWM process, the ZOH model is often considered to be an adequate DPWM model for higher frequencies [4], [6]. Nevertheless, as shown in [16], neither pure delay nor ZOH are accurate small-signal models of DPWM. In this paper, the small-signal model of the asymmetrical uniformly-sampled PWM, obtained using the describing function approach [5], [16], is used:

$$G_{dpwm}(s) = \frac{d(s)}{m(s)} = \frac{1}{2} \left(e^{-sDT_s} + e^{-s(1-D)T_s} \right), \quad (3)$$

where d is the continuous-time duty-cycle of $x(t)$, used in averaged modeling [5]. Expression (3) can be represented in the frequency domain as:

$$G_{dpwm}(j\omega) = \cos \left(\omega T_s \left(D - \frac{1}{2} \right) \right) e^{-j\omega \frac{T_s}{2}}, \quad (4)$$

where ω is the angular frequency and j is the imaginary unit. Contrary to ZOH and delay models, the small-signal DPWM model in (3) shows dependency on the SSOP, i.e. on the steady-state value of the duty cycle D .

B. Single-frequency admittance model

At first, a single-frequency small-signal model of the system from Fig. 1 is derived, which neglects the influence of sideband harmonics. A small-signal continuous time domain representation of the current control loop is given in Fig. 1 c). One step computation delay is modelled by:

$$G_d(s) = e^{-sT_s}. \quad (5)$$

Using the small-signal DPWM model from (3) and load representation given in (1), the loop gain of the system from Fig. 1 c) is defined by:

$$T(s) = \frac{i(s)}{e(s)} = G_c(s)G_d(s)G_{dpwm}(s)G_l(s). \quad (6)$$

Single-frequency model of the input admittance of the VSC is then given by:

$$Y(s) = -\frac{i(s)}{v_{pcc}(s)} = \frac{G_l(s)}{1 + T(s)}. \quad (7)$$

C. Sidebands in digitally controlled PWM systems

Besides the desired frequency component f_p , PWM creates sideband harmonics. They are created symmetrically around switching frequency multiples, i.e. at frequencies $m f_{pwm} \pm n f_p$, where m and n are integers [22]. These sidebands are reported to create additional loops which have considerable impact on system performance, especially near the switching frequency [23], [24].

In digitally controlled systems, additional sidebands, created by the sampling process, are also manifested [16]. If the signal to be sampled is a sine wave at frequency f , in addition to this frequency component, the sampled signal will contain an infinite number of aliases, appearing as sidebands to the SF multiples, i.e. at $k f_s \pm f$ [4]. These sampling-related sidebands are also reported to create additional loops in the control system, which have a non-negligible impact on the system performance above NF [4].

In the general case of a DPWM-controlled system, both switching and sampling sidebands are present and mutually coupled. This makes a precise high-frequency modelling, considering both effects, very challenging [16]. Modelling is especially complex in case of the double-update rate since, due to the switching and sampling frequencies being different, PWM and sampling sidebands are not created around the same frequency. To the best of authors' knowledge, no such model for double-update digital application has been reported in the literature. Rather than developing such a complex model, in this paper we show analytically, and verify in simulations and experiments, that in the current-controlled systems with center-pulse sampling, sidebands originating from PWM do not create additional loops.

D. Multiple-frequency admittance model

In this paper, to derive a multiple-frequency small-signal model of the system from Fig. 1, the approach from [4] is used to include the influence of sampling sidebands only. According to the derivation provided in the Appendix, if the sampling instants are properly synchronized with the carrier, these sidebands are the only ones which create additional loops in the closed loop operation of the digitally-controlled VSC. Thus, as it will be validated through simulations and experiments, the multiple-frequency model derived below accurately predicts the small-signal properties of the system from Fig. 1 a) even above the NF. Considering the aliases generated by the sampling process, sampled current i_s is given by [4], [25]:

$$i_s(t) = i(t) \sum_{k=-\infty}^{\infty} (1 + 2 \cos(jk\omega_s t))^1, \quad (8)$$

where $\omega_s = 2\pi T_s$. Applying Laplace transform to (8) gives:

$$I_s(s) = \sum_{k=-\infty}^{\infty} I(s - jk\omega_s) \quad (9)$$

Using (9) as a basis and following the procedure from [4], the multiple-frequency input admittance of the converter is derived as:

$$Y_m(s) = \frac{G_l(s)}{1 + \frac{T(s)}{1+T_s(s)-T(s)}}, \quad (10)$$

where $T_s(s)$ is

$$T_s(s) = \sum_{k=-\infty}^{\infty} T(s - jk\omega_s). \quad (11)$$

E. Model performance and comparison with existing models

To illustrate the performance of the proposed multiple-frequency small-signal model, in Fig. 4, AMs simulated during different SS-DC regimes are compared to the FR obtained

¹If signal $i(t)$ contains spectral component above NF, magnitude of the corresponding component in i_s depends on the relation between sampling instant and initial phase of the considered component. This is not analyzed in [4] and not included in this model of the sampling process. The impact of this sampling instant dependency is shown to be negligible, by repeating simulations and experiments with various initial phases of the perturbation component.

Fig. 4: Comparison between simulated AMs and the proposed small-signal model given by (10). The gray vertical line marks the NF.

analytically using (10). The infinite sum from (10) is replaced by a finite sum of 1000 elements, since the contribution of higher order elements is shown to be negligible. Simulations were performed in the same way and with the same parameters described in Section II. According to the presented results, the proposed methodology accurately models VSC's input admittance even in the very high frequency range, and is able to predict dependence of the small-signal properties on the SSOP.

In order to illustrate the benefits of the proposed model, it is compared to different models reported in the literature. The models differ from each other in the way PWM and sampling process are modelled, as listed in Table II. Models 1-3 are single-frequency models which represent PWM as a delay, ZOH and (3), respectively. Model 4 is the multiple-frequency model from [4], whereas Model 5 is the small-signal multiple-frequency model, proposed in this paper and given by (10).

TABLE II: Different small-signal models used for benchmarking.

Model	DPWM: $G_{dpwm}(j\omega)$		Sampling: $I_s(j\omega)$
	gain	phase	
1	1		
2	$\frac{2}{\omega T_s} \sin\left(\frac{\omega T_s}{2}\right)$		$I(j\omega)$
3	$\cos\left(\omega T_s \left(D - \frac{1}{2}\right)\right)$	$e^{-j\omega \frac{T_s}{2}}$	
4	$\frac{2}{\omega T_s} \sin\left(\frac{\omega T_s}{2}\right)$		$\sum_{k=-\infty}^{\infty} I(j(\omega - k\omega_s))$
5	$\cos\left(\omega T_s \left(D - \frac{1}{2}\right)\right)$		

Fig. 5 illustrates the comparison between the analytical models from Table II and simulation results obtained at $D = 0.5$. Firstly, it can be seen that different modeling approaches differ more in the admittance phase than in its magnitude. Secondly, for $D = 0.5$ Model 1 and 3 are identical. Next, for the VSC and control loop parameters considered in this paper, Model 2 and 4 show very similar results. Another important observation is that Model 3 shows an excellent match with simulation results up to a certain frequency, in this case $0.8f_s$. Finally, only Model 5 is able to accurately predict admittance

Fig. 5: Comparison between different models and simulated AMs at $D = 0.5$. Results for Model 1 completely overlap with those of Model 3.

Fig. 6: Comparison between different models and simulated AMs at $D = 0.85$. The gray vertical line marks the NF.

FR in the very high frequency range (around and above SF). Note that, up to very high frequencies, single-frequency Model 3 negligibly deviates from multiple-frequency Model 5. Fig. 6 illustrates comparison between the analytical models from Table II and simulation results obtained at $D = 0.85$. Since Models 1, 2 and 4 are unable to predict dependence of the small-signal properties on the OP, they give the same results regardless of the duty cycle. As in the previous case of $D = 0.5$, Model 3 shows an excellent match with simulation results up to $0.8f_s$, but only Model 5 accurately predicts admittance FR in the full frequency range.

Note that all of the previously presented simulation results were obtained (as specified in Table I), with 1% dead-time, which did not compromise the proposed modelling validation. Dead-time is one of the causes for non-ideal center-pulse sampling. In addition, due to non-zero filter resistance, presence of analog low-pass filters, etc. [26], [27] ideal center-pulse sampling is difficult to achieve in practice. Thus, a question arises if the reasoning for PWM sideband elimination provided in Appendix is justified in practical applications. To address this issue, multiple simulations for obtaining admittance FR were performed with intentionally increased non-idealities. Two different sets of simulations were performed, each implementing either increased values of dead-time or of filter

resistance R . Simulation parameters other than these were the same as previously explained. Deviations between simulation results and the proposed model (10) are expressed relative to the values predicted by the model. Table III shows only the maximum values of deviations and frequencies at which they are obtained. According to the presented results, even with unrealistically high levels of non-idealities, mismatch between the proposed model and simulation results is very low. Thus, PWM sideband influence proves to be negligible even in practical applications where center-pulse sampling is not ideal.

TABLE III: Deviations between simulation results with non-ideal center-pulse sampling and the proposed small-signal model (10).

max error [%] @ freq. [kHz]	t_{dt}/T_{pwm}		$L/(RT_{pwm})$	
	0.03	0.1	10	2
magnitude	0.9 @ 6	1.9 @ 11	0.6 @ 6	2.3 @ 33
angle	0.5 @ 22	2.2 @ 51	0.5 @ 41	2.3 @ 29

IV. MODEL FOR PREDICTING AM DURING S-AC REGIME

As illustrated in the previous section, the small-signal DPWM model depends on the SSOP. For grid-tied AC operation, OP is changing slowly with respect to the control period. Indeed, during S-AC regime, the OP is exhibiting a sinusoidal change at the fundamental frequency. In practical grid-connected applications, purely S-AC operation may not be present due to significant grid distortion; however, the following approach, derived for S-AC operation, may be extended for any waveform of the grid voltage.

According to the results presented in Section II, FR obtained during S-AC operation is a weighted average of AMs obtained during SS-DC regimes in the same OP range. Therefore, a question arises about which representation of the DPWM model would be accurate for predicting the admittance FR during S-AC operation. As per EN 50388-2 standard, AM should be performed with an estimation data window length which is a multiple of the fundamental period. In order to address this, we present the approach to obtain an adequate DPWM representation compliant with EN 50388-2. The small-signal model from (3) is averaged on the fundamental period:

$$G_{dpwm}^{s-ac}(j\omega) = \frac{1}{u_{pp}} \int_{u_1}^{u_2} \cos\left(\omega T_s \left(u - \frac{1}{2}\right)\right) e^{-j\omega \frac{T_s}{2}} du, \quad (12)$$

where u is the duty cycle which is assumed to change in a sinusoidal manner with respect to $\theta = 2\pi f_1 t$:

$$u = \frac{u_{pp}}{2} \sin \theta + \frac{1}{2}. \quad (13)$$

Since $\theta \in [-\pi, \pi]$, limits of the integral in (12), are $u_1 = \frac{1}{2} - u_{pp}$ and $u_2 = \frac{1}{2} + u_{pp}$. Substitution of (13) in (12) results in:

$$G_{dpwm}^{s-ac}(j\omega) = \frac{1}{\pi} \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \cos\left(\omega T_s \frac{u_{pp}}{2} \sin \theta\right) e^{-j\omega \frac{T_s}{2}} d\theta, \quad (14)$$

which, when solved, yields:

$$G_{dpwm}^{s-ac}(j\omega) = J_0\left(\omega T_s \frac{u_{pp}}{2}\right) e^{-j\omega \frac{T_s}{2}}, \quad (15)$$

where J_0 is the zero order Bessel function of the first kind. As it will be verified in simulations and experiments, the derived model is a suitable representation of the DPWM which operates in an AC regime, with the modulating signal exhibiting sinusoidal change at the fundamental frequency, which is considerably lower than the SF. Therefore, the single- and multiple-frequency models to predict AM during S-AC operation are similar to the ones from (7) and (10), respectively, the only difference being that the DPWM model from (3) is replaced with (14). Therefore, the modified single-frequency model suitable for S-AC operation is given by:

$$Y^{s-ac}(s) = \frac{G_l(s)}{1 + T^{s-ac}(s)}, \quad (16)$$

where $T^{s-ac}(s) = G_c(s)G_d(s)G_{dpwm}^{s-ac}(s)G_l(s)$. The resulting multiple-freq. model is finally obtained as:

$$Y_m^{s-ac}(s) = \frac{G_l(s)}{1 + \frac{T^{s-ac}(s)}{1 + T^{s-ac}(s) - T^{s-ac}(s)}}, \quad (17)$$

where $T_s^{s-ac}(s) = \sum_{k=-\infty}^{\infty} T^{s-ac}(s - jk\omega_s)$. It should be emphasized, that the model from (17) is not anymore a small-signal model and thus is not adequate for system stability assessment. To address stability of the VSC during S-AC operation, the tools developed for stability assessment of linear time periodic systems must be used [28]. Yet, as it will be shown, the proposed model accurately predicts AM, compliant with the EN 50388-2 standard, and therefore can be considered a valuable tool when designing control loops to satisfy the prescribed passivity criteria.

A. Model performance and comparison with existing models

To illustrate performance of the proposed S-AC multiple-frequency model (17), admittance FR obtained from simulations is compared to the proposed analytical model (17) in Fig. 7. Results are given for different S-AC regimes, defined by peak-peak duty cycle variation u_{pp} . Simulations were performed in the same way and with the same parameters described in Section II. According to the presented results, the proposed methodology accurately models VSC's input admittance even in the very high frequency range and is able to predict dependence of the system properties on the fundamental frequency peak-peak duty cycle variation.

In order to illustrate the benefits of the proposed model, it is compared to different models reported in the literature. The same models from Table II are used to denote Model 1, 2 and 4, whereas models denoted as Model 3^{s-ac} and 5^{s-ac} are the models defined by (16) and (17). Note that in [4], [11], Model 1, 2 and 4 are used for admittance modelling during S-AC operation and therefore are considered for benchmarking in this paper. Fig. 8 illustrates the comparison between the analytical models and simulation results obtained at $u_{pp} = 0.8$. Note that peak-peak duty cycle variation of 0.8 corresponds to the nominal PCC voltage (see Table I). As can be seen, Model

Fig. 7: Comparison between simulated AMs and the proposed model for predicting AM during S-AC operation given by (17). The gray vertical line marks NF.

Fig. 8: Comparison between different models and simulated AMs during S-AC operation with $u_{pp} = 0.8$. The gray vertical line marks the NF.

Fig. 9: Comparison between different models and simulated AMs during S-AC operation with $u_{pp} = 0.4$. The gray vertical line marks the NF.

1 fails to predict system performance at high frequencies. All other models give almost the same FR results and predict well the system dynamics. Still, the proposed model gives the best match with simulation results. Note that, since for $u_{pp} = 1$ the proposed DPWM model (14) reduces to ZOH model, Model 2 and 4, which use ZOH model to represent DPWM, are expected to give valid AM predictions only

Fig. 10: Experimental setup: 1) Input power supply, 2) VSC and control board, 3) Perturbation circuit, 4) Programmable AC source.

for high u_{pp} values. Due to u_{pp} being defined as the ratio between grid voltage magnitude and DC link voltage, lower values of u_{pp} might be present in some applications. In Fig. 9 the analytical models are compared to simulation results obtained with $u_{pp} = 0.4$. Model 1, 2 and 4 now result in a significant error, whereas Model 3^{s-ac} gives valid predictions until approximately $0.8f_s$. Again, only Model 5^{s-ac} is able to accurately predict AM during S-AC operation in the entire considered frequency range.

V. EXPERIMENTAL VERIFICATION

With the goal of validating the proposed analytical models, experimental AMs during different SS-DC and S-AC regimes are provided in this section. Experimental verification is performed using an industrial full-bridge single-phase VSC operated via bipolar modulation. Regenerative power system Keysight RP7962A is used as VSC's input DC voltage. Hardware parameters of the system used are provided in Table I. The experimental setup is shown in Fig. 10.

The control system is implemented on an NI sbRIO-9606, which is based on a Xilinx Zynq 7020 all programmable system on chip (AP-SoC). The inductor current is sensed by a custom interfacing board, based on a shunt resistor. The board uses conditioning circuits, a 12 bit ADC module AD9226 by Analog Devices, and digital isolators. The DPWM clock runs at 160 MHz. For the purposes of digital implementation of (2), used in the following experiments, PR current controller is discretized using impulse invariant method [21].

AMs are performed in the same way as described in Section II. For injecting the perturbation, the same approach as in [13] is followed. The sinusoidal perturbation source is implemented using power operational amplifier MP118 from APEX. For AMs during S-AC operation, Chroma 6460 programmable AC power supply is used to provide fundamental frequency component.

Perturbation is injected at 22 different frequencies, one at the time, starting from 6 kHz and up to 41 kHz, thereby avoiding multiples of switching frequency. In order to ensure precise measurements in presence of switching ripple and noise, magnitude of the injected sinusoidal perturbation is calculated for each perturbation frequency to obtain at least 100 mA magnitude of the perturbation current flowing through the VSC. Perturbations above 41 kHz resulted in the required

Fig. 11: Comparison between experimental AMs during different SS-DC regimes and the proposed small-signal model given in (10). The gray vertical line marks NF.

perturbation voltage being above hardware limitations of the prototype. Therefore, experimental AMs are given up to 41 kHz, which is just above the SF. The inductor current i and the PCC voltage v_{pcc} are measured via Tektronix 5 series oscilloscope with the data length of 40ms. Postprocessing, which assumes FFT of i and v_{pcc} , is performed in MATLAB to obtain spectral components of i and v_{pcc} at perturbation frequency. These components are then used to calculate the admittance at the perturbation frequency. Note that AMs were performed with the reduced DC link voltage $E = 250$ V to achieve higher resolution for data acquisition. According to (10) and (17), this has no effect on AM, as it will be validated by the subsequent results.

AMs during different SS-DC regimes are shown in Fig. 11, where they are compared to the proposed small-signal model (10). An excellent match between experiments and analytical predictions is achieved up to the SF for all measured SS-DC regimes. This attests to the accuracy and robustness of the proposed high frequency small-signal modelling approach.

AMs during different S-AC regimes are shown in Fig. 12, where they are compared to the proposed model for S-AC operation (17). Experimental measurements match very well with the analytical results up to the SF for all measured S-AC regimes. This verifies that the proposed modelling approach accurately predict AM during S-AC operation. The proposed model matches with the experimental AMs better than any of the reported models [4], [6], [7], [15].

VI. CONCLUSIONS

In this paper, high frequency modelling of the VSC input admittance is addressed. At first, the impact of the OP on AM is revealed. It is shown that AM obtained while the VSC is operating in S-AC regime is some kind of averaged result of AMs obtained during different SS-DC regimes from the same range. Next, a small-signal model which accurately represents system properties above NF is presented. Due to the accurate small-signal DPWM representation used, the proposed model is capable of predicting dependence of the FR on SSOP. It is shown that, when center-pulse sampling is employed, PWM sidebands do not create additional loops, which allows

Fig. 12: Comparison between experimental AMs during different S-AC regimes and the proposed model given in (17). The gray vertical line marks NF.

only sampling sidebands to be considered. Finally, in order to accurately predict AM during S-AC operation, a novel DPWM model suitable for S-AC operation is derived. Following the same methodology as for SS-DC operation, a model which is capable of predicting dependence of the FR on the grid voltage magnitude is derived. To validate the proposed methodologies, experimental verification is performed on a single-phase two-level VSC. An excellent match between experiments and the proposed analytical models is achieved up to SF during different SS-DC and S-AC regimes. Additionally, in order to illustrate the better accuracy of the proposed techniques, a comparison with the state-of-the-art models is provided.

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APPENDIX

In order to analytically show that center-pulse sampling eliminates additional loops created by PWM sidebands, the system shown in Fig. 1 a) is considered, without closing the feedback loop. It consists of DPWM, inductor and sampler. An input to this system $m_s(t)$ is assumed to be:

$$m_s(t) = D + M \cos(\omega_p t + \phi_p), \quad (18)$$

where D is the steady-state duty cycle and M is the magnitude of the sinusoidal perturbation at angular frequency ω_p with initial phase ϕ_p . Expressions for the voltage sidebands u_{sb} generated by asymmetrical uniformly-sampled PWM process are [22]:

$$u_{sb}^{m,n} = \frac{4E}{\pi} \frac{J_n(q2M\pi)}{q} \sin\left(r\frac{\pi}{2}\right) e^{jn\phi_p}, \quad (19)$$

where m and n are the orders of switching and sideband harmonics respectively, as in [22], $q = m + n\frac{\omega_p}{\omega_{pwm}}$ is the sideband order, J_n is Bessel function of the first kind with an order n and $r = m + n + q(2D - 1)$. Expressions for

Fig. 13: Spectrum of the inductor current: illustration of the components which, after sampling are mapped to the first sampled sideband.

currents i_{sb} resulting from these voltages are derived simply via dividing (19) by inductor impedance at sideband frequency $q\omega_{pwm}$:

$$i_{sb}^{m,n} = \frac{4E}{\pi L} \frac{J_n(q2M\pi)}{\omega_{pwm} q^2} \sin\left(r\frac{\pi}{2}\right) e^{j(n\phi_p - \frac{\pi}{2})}. \quad (20)$$

Finally, to derive an expression for the spectral content of the sampled current $i_{s,sb}$, the model of the sampling process needs to be applied [25]. Due to the double-update rate implementation, the NF coincides with the switching frequency. Therefore, to derive an expression for the sideband components after sampling, only sidebands around odd multiples of the switching frequency have to be taken into account². To keep the presentation concise, only expression for the first sampled sideband $i_{s,sb}^1$, which is at $\omega_{pwm} - \omega_p$, is derived. The reasoning shown below holds also for the higher order sidebands: $\omega_{pwm} - 2\omega_p, \omega_{pwm} - 3\omega_p, \dots$. The components of the inductor current which after sampling are mapped to $\omega_{pwm} - \omega_p$ are the first sideband components around odd multiples of the switching frequency, i.e. $|n| = 1$ for $m = 1, 3, 5, \dots$. This is illustrated in Fig. 13, where the spectrum of the inductor current is shown, resulting from $m_s(t)$ with the following parameters $D = 0.75, M = 0.0625, \omega_p = 2\pi 5$ rad/s.

Following the previously explained procedure, the expression for the first sampled sideband component is derived:

$$i_{s,sb}^1 = \sum_{m=1,3,5,\dots}^{\infty} \left| i_{sb}^{m,-1} \right| e^{j\phi_{i_{sb}^{m,-1}}} + \left| i_{sb}^{m,1} \right| e^{-j\phi_{i_{sb}^{m,1}}}. \quad (21)$$

As seen, this expression depends on an infinite number of sideband harmonics. Complex mathematical procedures are required to prove that the magnitude of this expression equals zero for any valid set of input parameters D, M, ω_p, ϕ_p . To avoid the added complexity, a numerical search is performed with the parameters being constrained by the following inequalities $0 < D < 1, D + M < 1, D - M > 0, 0 < \omega_p < \omega_{pwm}, 0 < \phi_p < 2\pi$. For these constraints, obtained

²Sidebands around even multiples of the switching frequency are after sampling reflected back to the original component ω_p . This does not produce any additional loop; however it does produce a certain impact on the perturbation component magnitude. These sidebands are always above the NF; hence resulting sampled current components depend on the relation between their phase and the sampling instant. A great number of consistent simulated and experimental AMs showed that the impact of this effect on closed loop operation is negligible.

Fig. 14: Comparison between spectra of the current before and after sampling in closed loop operation with 5 kHz perturbation frequency.

maximum of the first sampled sideband magnitude, relative to the magnitude of the perturbation current, is equal to 0.07%. Therefore, it can be safely assumed that:

$$|i_{s, sb}^1(D, M, \omega_p, \phi_p)| \approx 0. \quad (22)$$

The analysis provided above has shown that center-pulse sampling eliminates PWM sidebands created around odd multiples of the switching frequency. Thus, additional PWM sideband loops are not present in the closed loop operation. As an illustration of this phenomenon, the current spectrum before and after sampling, obtained from the closed loop simulation of the system in Fig. 1 is shown in Fig. 14. The perturbation frequency was set to 5 kHz. As seen from this figure, PWM sideband at 15 kHz is present in the inductor current, but not in the sampled signal.

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