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An Adaptive Gain Tuner Based Fore-ground Calibration Algorithm of a Pipeline ADC

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Abstract—This brief proposes a low power mixed-signal foreground calibration algorithm of a pipeline ADC, using a digitally controlled re-configurable switched capacitor multiplying DAC (MDAC) gain controller. The proposed calibration technique forces the front-end stage MDAC gain towards its ideal value to achieve the ideal ADC output linearity. In this paper, a feedback mechanism has been employed to nullify the effect of change in MDAC gain from its ideal value by sensing a digital back-end unit response. The proposed technique has been verified in 0.18 μm CMOS process using the cadence virtuoso tool by simulating an 11-bit pipeline ADC which contains a 1.5-bit non-ideal pipeline stage followed by a 10-bit linear back-end ADC (BE-ADC). Simulation results demonstrate the recovery of the lost linearity of a 11 bit pipeline ADC post calibration.

Index Terms—Pipelined-ADC, Foreground Calibration, MDAC Gain, Adaptive Gain Tuning, Mixed-Signal.

I. INTRODUCTION

PIPELINED ADCs [1]-[3] are very useful for wireless communication applications because of high speed, high resolution, and low power consumption at the same time. As the process technology nodes are shrinking every year, reduction of power consumption becomes one of the critical design concerns [4]. To reduce the power budget of a high resolution Pipeline ADCs, reducing the intrinsic gains of building blocks such as amplifiers are essential, resulting in non-linearity at the ADC output [5]. In order to counter the effect of non-linearity at the ADC outputs, calibration has become a popular choice [4], [6]-[15] to meet the growing specification demand. In this paper a low power mixed signal foreground calibration technique has been proposed based on a digitally assisted dynamic switched capacitor gain tuner. Unlike radix extraction based foreground calibration technique ([8], [12]-[15]), the proposed method forces the MDAC gain value of a pipeline stage to its ideal value by deliberately skewing the ideal passive component ratio and proper choice of amplifier open loop gain [11]. The advantage of using the proposed calibration algorithm over the radix extraction based calibration algorithm is two fold. **Firstly**, in case of the radix extraction based calibration algorithm, the ADC output bit streams are not calibrated; instead, it calibrates an ADC output code which is of the form $D_{out} = ra_1 D_1 + D_{BE}$, by accurately extracting the value of ra_1 . The proposed calibration algorithm, on the other hand, calibrates the ADC output bit-stream itself. In doing so, the proposed method calibrates the relevant stage gain to its ideal value, rather than extracting its actual value. **Secondly**, typical radix extraction based algorithms often requires complex back end post processing to generate

the correct radices ([6], [8] and, [12]-[15]), e.g., an iteration and update algorithm. In the proposed method, a fairly simple feedback mechanism does the job of calibrating the ADC output, without the need of an iteration and update method. Further, this method calibrates a pipeline stage within a very few clock cycles, in the order of 10. Summary of few existing works are given in Table I.

TABLE I: LITERATURE SURVEY

Ref.	Gain Error Calibration	Capacitor Mismatch Calibration	Radix Extraction based	Update and Iteration Based
[6]	YES	YES	YES	YES
[12]	YES	YES	YES	NO
[15]	YES	YES	YES	NO
[Pro.]	YES	YES	NO	NO

Fig. 1: Block Diagram of a Pipeline ADC

In this paper, an 11 bit pipeline ADC, as shown in Fig. 1, has been considered for illustration. In this ADC, 1st stage is under calibration. Rest of the stages, forming a 10 bit linear back-end ADC (BE-ADC), helps in the calibration process. As shown in [8], [9], [10] and [12]-[14], BE-ADC outputs are used as data for the post processing in order to carry out objectives such as extraction of radices of the target stages. It may be noted here that using an N bit BE-ADC for post processing is a fairly standard practice for algorithms using radix extraction. The proposed method, although does not use radix extraction, uses the linearity of the BE-ADC to accurately calibrate a pipeline stage. The paper is organized as follows: Section II explains the proposed calibration mechanism. Section III discusses the circuit implementation of the calibration block. The Simulation results are given in section IV followed by conclusions in Section V.

II. PROPOSED CALIBRATION TECHNIQUE

Fig. 2 shows the block diagram of the first stage of an 11-bit pipeline ADC, along with a BE-ADC of 10-bit linearity. The concept of the algorithm is explained considering a generalized block diagram of a switched capacitor pipeline stage. In latter sections, detailed analysis on two different types of pipeline stage topologies, viz. capacitor flip-over and capacitor nonflip-over types will be discussed in detail. As gain of pipeline stage for both these topologies depend upon the ratio of the two constituent capacitors, they have been indicated as C_S and C_F in Fig. 2. The basic idea behind the calibration algorithm is to use a DC signal at the ADC input, which has a defined digital output. Corresponding BE-ADC output of that signal is D_{BE} .

Due to the non-ideal nature of the first pipeline stage D_{BE} is different from $D_{BE,ideal}$. These two digital outputs are then compared by a 10-bit digital comparator, which activates a control logic, associated with the stage capacitors C_S and C_F . In [11], in order to achieve a pipeline stage gain of exactly 2, amplifier gain was varied. In this paper, instead of controlling the amplifier gain, magnitude of the capacitor ratio, C_S/C_F is controlled using a unit capacitor bank. However, in order to achieve that, a calculation of the desired amplifier gain is necessary. In the following sections, the two topologies of a switched-capacitor based MDAC circuit is discussed.

Fig. 2: Block Diagram Representation of Calibration Technique

A. Capacitor Flip Over Topology:

A capacitor flip around pipeline stage shown in Fig. 3. The residue ($V_{residue}$) signal expression can be written as [5],

$$V_{residue} = \left(\frac{C_S + C_F}{C_F + \frac{1}{A}(C_S + C_F + C_P)} \right) V_{in} - \left(\frac{C_S}{C_F + \frac{1}{A}(C_S + C_F + C_P)} \right) D_i \frac{V_R}{2} \quad (1)$$

where D_i s are the digital output of the i_{th} pipeline stage. A is the amplifier gain, C_P is the parasitic capacitance. $C_S = (1 + \gamma)C_F$, where γ is the mismatch factor. Ideally the residue voltage expression for 1.5 bit stage can be written as, $V_{residue} = 2V_{in} - V_{DAC}$, where V_{DAC} is $D_i V_R/2$. Equating coefficient of V_{in} to 2 and solving for A ,

$$A = 2 \left(\frac{C_F(2 + \gamma) + C_P}{\gamma C_F} \right) \quad (2)$$

Substituting "A" into the co-efficient of V_{DAC} and solving,

$$V_{residue} = 2V_{in} - \frac{1 + \gamma}{1 + (\gamma/2)} \times V_{DAC} = 2V_{in} - K \times V_{DAC} \quad (3)$$

Fig. 3: First Stage MDAC Showing Flip Around Topology

Under ideal condition, $\gamma = 0$ leads to $K_{ideal} = 1$. However for $\gamma \neq 0$, the non-ideal sub-DAC output distorts the residue characteristics. By replacing K in eqn. 3 with $K = K_{ideal} + K_{D-Error}$. In case of a flip-around MDAC topology, it is known that

$$V_{DAC} = \begin{cases} 0 & 0 \leq V_{in} \leq 3V_R/8 \\ V_R/2 & 3V_R/8 < V_{in} \leq 5V_R/8 \\ V_R & 5V_R/8 < V_{in} \leq V_R \end{cases}$$

For a input dynamic range of V_R , it is required to find out the linear and non-linear parts of the term $K_{D-Error} \times V_{DAC}$ [16]. To achieve that $K_{D-Error} \times V_{DAC}$ is segregated to,

$$K_{D-Error} V_{DAC} = \alpha_1 V_{in} + \beta_{1,V_{in}} \quad (4)$$

Plot of $K_{D-Error} V_{DAC}$ is shown in Fig. 4(a), where $\alpha_1 V_{in}$ represents the linear term and $\beta_{1,V_{in}}$ represents the non-linear function. To find α_1 , the mean absolute value of $\beta_{1,V_{in}}$ is calculated from eqn. (4) for $V_R = 1V$,

$$\int_0^{V_R} |(\beta_{1,V_{in}})| dV_{in} = \int_0^{V_R} |-(K_{D-Error})V_{DAC}| dV_{in} + \int_0^{V_R} |-\alpha_1 V_{in}| dV_{in} = 0.5K_{D-Error} + 0.5\alpha_1 \quad (5)$$

Fig. 4: Flip Over MDAC Sub-DAC Error Characteristics

The constant α_1 in eqn. (5) is determined such that the mean absolute value of $\beta_{1,V_{in}}$ is minimized [16]. From Eqn. (5), α_1 is calculated as $\alpha_1 = -K_{D-Error}$ and $\beta_{1,V_{in}=V_R} (= \beta_{1,V_{in,max}})$ can be calculated from eqn. (4) as,

$$\beta_{1,V_{in,max}} = (K_{D-Error} V_R) - (-K_{D-Error}) V_R = 2K_{D-Error} V_R \quad (6)$$

Considering a linear BE-ADC, INL of the 11 bit ADC will be equal to $|\beta_{1,V_{in,max}}|/LSB$. For $V_R = 1V$, with an allowable ADC INL value of $1LSB$, the maximum of $K_{D-Error}$ value is found out from eqn. (6) as,

$$1 = \frac{2(K_{D-Error} V_R)}{1LSB} \Rightarrow K_{D-Error,max} = 0.0003 \quad (7)$$

Eqn. (7) gives the maximum allowable value of K as 1.0003. Using Eqn. (1) and (2) Table II is formed, which gives the choice of A and C_S/C_F .

TABLE II: Identification of the optimum (C_S/C_F) and A value

$\frac{C_S}{C_F}$	C_P	A (V/V)	V_{in} Co-eff.	$ K_{D-Error} $	ADC SNDR
1.0002	10 fF	490	1.9918	1.0001	60.51 dB
1.0006	10 fF	490	1.9925	1.0003	61.35 dB
1.0006	10 fF	550	1.9935	1.0003	62.07 dB

B. Capacitor Non-Flip Over Topology:

A practical capacitor non-flip around pipeline stage shown in Fig. 5. Using the component parameters, the residue expression can be written as

$$V_{residue} = \frac{C_S}{C_F + \frac{1}{A}(C_S + C_F + C_P)} \times \left(V_{in} - D_i \frac{V_R}{4} \right) \quad (8)$$

Considering V_{in} as the input of a 1.5 bit non-flip around stage of MDAC gain G , the output signal can be written as,

$$V_{residue} = G(V_{in} - V_{DAC})$$

$$= (K_{G-ideal} + K_{G-Error})(V_{in} - V_{DAC}) \quad (9)$$

For non-ideal cases, G deviates from ideal value of '2' due to non-zero $K_{G-Error}$ value and distorts the ADC output. From [16], the term $K_{G-Error} \times V_{DAC}$ in the eqn. (9) determines the non-linearity error of the stage. For a non-flip around stage with dynamic range V_R , V_{DAC} is defined as,

$$V_{DAC} = \begin{cases} 0 & 0 \leq V_{in} \leq 3V_R/8 \\ V_R/4 & 3V_R/8 < V_{in} \leq 5V_R/8 \\ V_R/2 & 5V_R/8 < V_{in} \leq V_R \end{cases}$$

Fig. 5: First Stage MDAC Showing Non-Flip Around Topology

Hence, to evaluate the effect of $K_{G-Error}$ on the ADC output linearity, ADC INL will be estimated in terms of $K_{G-Error}$. As shown in eqn. (4), $K_{G-error} \times V_{DAC}$ can be seperated to,

$$K_{G-Error}V_{DAC} = \alpha_2 V_{in} + \beta_2 V_{in} \quad (10)$$

To determine α_2 , the mean absolute value of $\beta_2 V_{in}$ is calculated from eqn. (10) With $V_R = 1V$,

$$\int_0^{V_R} |(\beta_2 V_{in})| dV_{in} = 0.25K_{G-Error} + 0.5\alpha_2 \quad (11)$$

From Eqn. (11), α_2 is calculated as $\alpha_2 = -0.5K_{G-Error}$ [16]. $\beta_2 V_{in} = V_R (= \beta_2 V_{in,max})$ can be calculated from eqn. (10) as,

$$\beta_2 V_{in,max} = 1.5K_{G-Error}V_R \quad (12)$$

The ADC INL in terms of $K_{G-Error}$ is estimated as $(1.5 \times K_{Gain-Error}V_R)/LSB$. Considering ADC INL of $1LSB$, maximum $K_{G-Error}$ value is found out as,

$$1 = \frac{1.5(K_{G-Error}V_R)}{1LSB}$$

$$\Rightarrow K_{G-Error,max} = 0.0004 \quad (13)$$

If, $G = K_{G-ideal} = 2$ is set, from eqn.(13), theoretically INL of the 11 bit ADC becomes $0 LSB$. Taking $C_P = 10fF$, estimated values of C_S/C_F and amplifier gain of a front-end non-flip-around MDAC are tabulated in Table III.

TABLE III: Identification of the optimum (C_S/C_F) and A value

$\frac{C_S}{C_F}$	A (V/V)	V_{in} Co-eff.	$ K_{G-Error} $	ADC SNDR (dB)
2.26	24.95	1.9996	0.0004	67.54
2.26	25	2.0000	0.0000	67.99
2.26	25.04	2.0004	0.0004	67.81

Comparing Table II and Table III, it is evident that in order to achieve 11 bit linearity of the ADC, non-flip-around topology provides a more attractive proposition, which requires a very low value of amplifier gain. This advantage provides the designer a flexibility in power-speed trade-off. These tables further show that in order to achieve an INL $< 1LSB$, non-flipover MDAC topology achieves better SNDR value than flip-over topologies at a much lesser amplifier gain value.

C. Adaptive MDAC Gain Logic Controller Mechanism

Fig. 6 shows the MDAC gain tuner logic controller. In general for an N bit pipeline ADC, a $(N - i)$ bit BE-ADC response is utilized to calibrate the i_{th} stage [8]. In this diagram, a 1.5 bit front end pipeline stage of a 11 bit pipeline ADC has been calibrated using a 10-bit BE-ADC. In order to provide a low power solution of ADC non-linearity error calibration, a non-flip-around topology of the MDAC has been chosen. For such type of MDAC, from Table III, it is observed that when $C_S/C_F = 2.26$, pipeline stage amplifier gain must be at $A = 25$ V/V to obtain an MDAC gain of 2 V/V.

Fig. 6: MDAC Gain Controller Block Diagram

In practical circuits, it is difficult to maintain an open-loop amplifier gain which remains consistent with Process, Voltage and Temperature (PVT) variations. Hence, the proposed feedback mechanism ensures an MDAC gain of 2 V/V, by adaptively tuning the MDAC voltage gain of the pipeline stage by changing the desired capacitor ratio. To start the calibration, control signal (CAL) goes high and a input voltage of $V_R/4$ is applied at the input of the pipeline ADC. Sub-ADC (S-ADC) output of the front-end pipeline stage is fed with a forced input of 00 (Fig. 6(a)). For this condition, the residue output of the front end pipeline stage can be written from eqn. (8) as,

$$V_{residue} = \left(\frac{C_S}{C_F + \frac{1}{A}(C_S + C_F + C_P)} \right) \times \frac{V_R}{4} \quad (14)$$

This residue signal, when fed to the BE-ADC, under non-ideal condition deviates from the ideal $D_{BE-ADC,ideal}$, $(512)_{DE}$. A 10-bit digital comparator is employed to detect this error by giving three possible decisions (G, E, L) as outputs. Based on these signals, the digital logic block tunes the MDAC gain. As explained in Fig. 2, an additional $[n \times n]$ sized unit capacitor array ($C_{uS,1} \dots C_{uS,n}$) and ($C_{uF,1} \dots C_{uF,n}$) are used to gradually adjust the MDAC gain towards its ideal value of 2 to linearize the ADC output.

Fig. 6 (b) shows control logic to change the C_S/C_F ratio. Two 11 bit johnson-ring counter is utilized to supply the control signals for two switch array ($S_1 + \dots S_{11}+$) and ($S_1 - \dots S_{11}-$) as per the status of G and L signal. For example, considering an initial amplifier open loop gain $= 20$ V/V, the digital comparator gives "L" as logic high as $D_{BE-ADC} < (512)_{DE}$. $Count_2 = (\phi_1.L)$ signal triggers the ring counter to start counting. Consequently, $V_{residue}$ gradually increases to $(512)_{DE}$ by adding 10 equally sized unit capacitors ($C_{uS,1}$

to $C_{uS,10}$ to C_S in 10 clock cycles. At 11th clock cycle, $V_{residue}$ becomes $(512)_{DE} + 1 \text{ LSB}$ and this in turn makes "G" logic high and "L" logic low. This transition of $V_{residue}$ is detected by the control logic as shown in Fig. 6(c). To detect the transition of $V_{residue}$ signal using $Clock_1$ and $Clock_2$, two successive samples of G and L signals are fetched through D-FFs, generating $IN1$ and $IN2$. Hence, a logic high pulse will be produced in Ctl signal whenever there is opposite logic of G and L signal in two consecutive samples. The status of switch control signals $[(S_1 + \dots S_{11})$ and $(S_1 - \dots S_{11})]$ at $V_{residue} = ((512)_{DE} - 1 \text{ LSB})$ get stored in two 11 bit register at the positive edge of Ctl signal, which is finally used to linearize the ADC output for signal input conversion. The corresponding timing diagram depicting the calibration mechanism is shown in Fig. 8.

III. IMPLEMENTATION OF THE CIRCUIT

Determination of the Capacitor Size:

Fig. 7: Noise model of the front-end stage MDAC

Fig. 7 shows the noise model of the non flip around front end MDAC stage, which will be used to estimate the component values of C_S and C_F . In the two phases the total input referred noise can be calculated as [5],

$$V_{tot,in}^2 = \left(\frac{C_S K T}{2 C_F^2} \right) + \frac{2 K T (1 + n_t)}{3 C_S + \beta_2 C_S} \left(\frac{C_S + C_F}{C_F} \right) \quad (15)$$

Taking, $C_S = 2.26 C_F$ (Table III), β_2 can be calculated as 0.30. For single stage low power opamp, $n_t = 2$ [5]. From eqn (15), for $C_S = 2.26 C_F$ and $\beta_2 = 0.3$, $V_{tot,in}^2 = \frac{3.36 K T}{C_F}$. To minimize these noise at the ADC output, $V_{tot,in}^2 < (0.5 \times \text{Quantization noise})$ is considered. Hence for a 11 bit ADC having input dynamic range of $V_R = 1V$, the minimum value of C_F and C_S are calculated as, $C_{F,min} = 1.37 \text{ pF}$ and $C_{S,min} = 3.1 \text{ pF}$ respectively.

For a 11 bit ADC with calibration input of $V_R/4 \text{ V}$, for $+1 \text{ LSB}$ deviation of $V_{residue}$, from eqn. (14) the first stage MDAC gain becomes $\approx (.501V/.250V) = 2.004V/V$. Similarly for -1 LSB deviation of $V_{residue}$, the MDAC gain value is found out as $\approx (.499V/.250V) = 1.996V/V$. Simulation has been done using eqn. (8) to estimate the C_S , C_F value for $\pm 1 \text{ LSB}$ change in $V_{residue}$ as shown in Table IV.

TABLE IV: Estimation of $C_{\mu S}$ and $C_{\mu F}$ values

C_P	C_S	C_F	A	MDAC Gain
10 fF	3.1000 pF	1.3708 pF	25.5 V/V	$\approx 2.004 \text{ V/V}$
10 fF	3.1000 pF	1.3748 pF	25.5 V/V	2 V/V
10 fF	3.1000 pF	1.3708 pF	24.5 V/V	$\approx 1.996 \text{ V/V}$
10 fF	3.1065 pF	1.3708 pF	24.5 V/V	2 V/V

Hence from Table IV, the required unit capacitor value to be added in parallel with the existing C_F to compensate the $0.5V/V$ change in amplifier open loop gain is found out as $4fF$ (C_{uF}). Similarly from Table IV, the unit capacitor required to be added in parallel with the existing C_S is

determined as $6.5fF$ (C_{uS}). In the implementation of the pipeline stage, $C_{\mu S}$ and $C_{\mu F}$ capacitor bank require 11 number of unit capacitors in each bank respectively. The switches of the capacitor bank have been implemented using typical transmission gate topology with NMOS (W/L)= 2/0.18, and PMOS (W/L)= 2/0.18 respectively. Hence the additional hardware, comprising of $C_{\mu S,total} = 3.1715 \text{ pF}$, $C_{\mu F,total} = 1.414 \text{ pF}$ and the switching network consumes a very nominal extra die area.

IV. SIMULATIONS RESULTS

Fig. 8: Non Flip Around Topology Timing Diagram (a) for $A = 20 \text{ V/V}$ (b) for $A = 30 \text{ V/V}$

Fig. 8(a,b) shows the transient plots of $V_{residue}$, $Clock_1$, $Clock_2$, L , G and ctl signal for initial amplifier gain (A_{ini}) of 20 V/V and 30 V/V . For $\pm 20\%$ variation of amplifier gain, in worst case 14 ADC clock cycles are required for the calibration scheme to converge to the ideal MDAC gain (Fig. 8). Hence, negligible halt time of normal ADC conversion is required. Simulation results of a 11 bit pipeline ADC in an 180 nm CMOS process are presented. The first 1.5 bit stage is treated with non ideal conditions (low amplifier gain, capacitor mis-match) and rest of the stages are modelled with ideal conditions and resolve 10 bits of data. For an input signal dynamic range of $1V_{P-P}$ and clock frequency of 100 MHz, Fig. 9 shows the pre and post calibration SNDR plots of the 11 bit pipeline ADC output sampled at nyquist rate. Considering non-flip around MDAC topology, for an initial amplifier open loop gain (A_{ini}) of 20 V/V and 30 V/V , the SNDR value gets improved to 65.13 dB (10.52 ENOB) from 46.21 dB (7.38 ENOB) (Fig. 9 (a)) and 65.16 dB (10.53 ENOB) from 44.23 dB (7.05 ENOB) (Fig. 9 (b)) post calibration respectively.

Fig. 9: Before and after calibration SNDR plots of the ADC (a) for $A = 20 \text{ V/V}$ (b) for $A = 30 \text{ V/V}$

Fig. 10 shows the before and after calibration differential non-linearity (DNL) and integral non-linearity (INL) plots of the 11-bit ADC under calibration. It is found that, with an

initial amplifier O/L gain value of 30 V/V, after calibration the INL of the ADC gets improved to $-1LSB \leq INL \leq +1LSB$ from $-24.2LSB \leq INL \leq 0LSB$. Fig. 11 shows the plot of SNDR variation with respect to variation in C_S/C_F ratio ($\pm 2.5\%$) and amplifier gain ($\pm 20\%$) before calibration (Fig. 11(a)) and after calibration (Fig. 11(b)). Plot shows that for all cases the post calibration SNDR of the 11 bit ADC in calibration achieves a minimum value of 64.11 dB.

Fig. 10: Pre and post calibration DNL Plots (a) and INL Plots (b) of the ADC for $A = 30V/V$

Fig. 11: SNDR variation w.r.t to C_S/C_F ratio and amp. gain (a) before calibration (b) after calibration

A. Variation of Calibration I/P Due to Noise and Temp. Drift:
Table V shows the ADC SNDR under the influence of varying calibration signal input. However, the allowable range of the deviation of calibration signal can be increased further by adding additional unit capacitors in the unit capacitor array.

TABLE V: Cal. I/P Variation vs Post Cal. ADC SNDR & INL

Cal. Sig. Var.	ADC SNDR	ADC INL_{Max}	$C_{us,tot}$	$C_{uf,tot}$
$\approx \pm 1\% V$	65.43 dB	$\pm 1 LSB$	3.19 pF	1.42 pF
$\approx \pm 2\% V$	65.39 dB	$\pm 1 LSB$	3.20 pF	1.43 pF
$\approx \pm 3\% V$	65.38 dB	$\pm 1 LSB$	3.21 pF	1.44 pF
$\approx \pm 5\% V$	65.36 dB	$\pm 1 LSB$	3.24 pF	1.46 pF

B. Variation of Unit Capacitor Ratio in Non-Ideal Conditions:

The resiliency of the proposed algorithm in practical scenario is further checked against the random variation in C_{us}/C_{uf} from its ideal value of "1.625" (refer section III). Fig. 12 shows the plot of ADC SNDR with respect to gaussian distributed randomly varying C_{us}/C_{uf} ratio. Plot shows the efficacy of the calibration algorithm for $\pm 68\%$ variation of C_{us}/C_{uf} ratio.

Fig. 12: SNDR variation w.r.t to C_{us}/C_{uf} ratio

C. Variation of the ADC Clock Period (Random Clock Jitter)

Timing jitter analysis of the ADC has been done with input clock jitter of 2%, 5%, 10% variation at nyquist sampling rate (Table VI). Table VI shows that in all cases after calibration SNDR value denotes ENOB > 10 Bit.

TABLE VI: ADC Input Clock Jitter % vs ADC SNDR

Clock Jitter (%)	ADC SNDR
2.5%	62.25 dB
5%	62.23 dB
10%	62.14 dB

V. CONCLUSION

In this paper, a low power foreground calibration technique of a pipeline ADC has been developed. The proposed algorithm employs a feedback mechanism to dynamically adjust the MDAC gain towards the ideal value to calibrate the ADC output. An 11-bit pipeline ADC has been simulated in $0.18 \mu m$ CMOS process technology. The post calibration simulation results of the 11 bit ADC proves that the proposed technique is capable of providing requisite SNDR considering variation in the values of amplifier gain (A) and capacitor ratio (C_S/C_F).

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