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An Advanced 1-bit Arithmetic Logic Unit (ALU) with Hybrid Memristor-CMOS Architecture

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Abstract—Memristor is dubbed as the fourth fundamental electrical component which works primarily as a non-volatile memory element. Memristors can also be used to construct logic gates, and Memristor Ratioed Logic (MRL) is one of these structures. The higher area efficiency and CMOS architecture compatibility of MRL gates have lead researchers to pay attention to its use in digital logic architecture. In this work, binary MRL is integrated with Complementary Metal-Oxide Semiconductor(CMOS) logic elements to develop building blocks of an Arithmetic Logic Unit (ALU). The proposed 1-bit ALU is simulated using LTSpice, which allows the versatility of changing the parameters as per the model used. This work designs and analyses an optimized cascadable 1-bit ALU with voltage level based binary logic state via simulation. The proposed circuit shows improvement in transistor count and delay over benchmark circuits.

Index Terms—ALU, Binary Logic, Memristor, MRL, Simulation.

I. INTRODUCTION

Memristor is an electrical element that retains its previous state through its resistivity. Theoretically, memristor is a non-linear two terminal device that relates magnetic flux to the electric flux. It functions as a resistor whose resistance depends on the charge previously flown through the device. Despite being introduced by L. Chua in 1971 [1], memristor did not get much attention until the recent years, when HP implemented the memristor [2]. Researchers focused on its possibilities for its small size, low power consumption and high switching capabilities [3]. Use of memristor is analysed in the field of non-volatile memory [4], logic circuits [5] and artificial neural network [6], [7].

Arithmetic Logic Unit(ALU) is one of the basic building blocks of processors. Complex computer processors require a lot of time and area due to the limitations of ALU. Memristor has smaller area and delay, which makes it a good candidate for modeling ALUs [8]. Memristors can be used to form different types of logic gates for digital systems. Memristance based or voltage based logic gates are most prevalent [5]. MRL gates operate on voltage based logic variable, which uses positive logic scheme [9]. Thus it is not suitable to implement ALUs on its own. Hybrid memristor-CMOS structure can implement complete ALU structure, which has been the focus of several recent works [10], [11]. However, the output signal degrades substantially when multiple Memristor Ratioed Logic (MRL) [9] gates are cascaded [12]. MRL gates suffer from

sneak path current flow when the input voltages are different, which results in higher static power consumption [9]. This work improves upon the existing proposed ALU models by integrating memristor-CMOS logic circuits with sophisticated approach.

The proposed 1-bit ALU model is fully cascadable, having nine functionalities. It is implemented by integrating Memristor Ratioed Logic(MRL) gates and 180nm CMOS elements [13]. The behavioral analysis is done using LTSpice. Using optimized building blocks, the model leads to an efficient ALU architecture. This work has focused on the following areas:

- Design and simulation of basic building blocks of ALU using memristor-CMOS hybrid model.
- Comparison between this model and current state-of-art ALU models based on memristor-transistor hybrid approach.
- Reducing signal degradation in each stage and thus in the overall ALU circuit.
- Reducing transistor count by replacing them with memristors having less area.

This paper is organized in 6 sections in total. Section I discusses the premise of this work. Section II describes the memristor model used. Section III introduces proposed building blocks of ALU. Section IV focuses on the 1-bit ALU architecture. Section V presents the findings of this work. Finally, conclusion is given based on future prospects of this work in Section VI.

II. GENERIC VOLTAGE-CONTROLLED MEMRISTOR MODEL

Memristive devices are introduced first using symmetry arguments. Its I-V characteristic is a hysteresis loop. The pinched I-V characteristics is what makes memristor retain its previous state depending on previously applied voltage.

Figure 1: I-V characteristics of fundamental circuit elements [14]

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Memristor defines the relationship between magnetic flux and electric flux through the following equation:

$$d\phi = M.dq \quad (1)$$

Memristor functions like a resistive memory element, but unlike a resistor, it has polarity. The symbol of memristor is shown in Fig. 2. A thick black line indicates the polarity of the device. Memristor is a two terminal device. The resistance of the memristor decreases when current flows into the device and the resistance increases when the current flows out of the device.

Memristor modeling has been an active research topic and provides quite a few models to map memristor behaviour. Threshold adaptive models that emulate memristor switching based on current [15] or voltage [16] applied to it are used predominately in memristive logic circuits. Digital logic can be implemented through IMPLY, MAGIC and MRL [5] memristive circuits. This work uses Memristor Ratioed Logic (MRL) [9] implemented with generic voltage-controlled memristor model.

Figure 2: Symbol of Memristor [9]

The generic voltage controlled memristor model [5] switches between two stable memristance states depending on applied voltage. The following mathematical model denotes this behaviour.

$$\begin{aligned} \frac{dx}{dt} &= \begin{cases} \frac{1}{e^{x-a}} & v > 0.2 \\ 0 & -0.2 \leq v \leq 0.2 \\ \frac{-1}{e^{-x-a}} & v < -0.2 \end{cases} \\ R(x) &= \begin{cases} R_{ON} & x \geq 0 \\ R_{OFF} & x < 0 \end{cases} \\ i(t) &= \frac{1}{R(x)}v(t) \end{aligned} \quad (2)$$

For this mathematical model,

x = state variable of the system

a = memristor parameter

v = voltage across memristor

i = current through memristor

$R(x)$ = memristance

R_{ON} = memristance state with low resistance

R_{OFF} = memristance state with high resistance

The memristor model simulated with necessary parameters in LTSpice gives a pinched graph, much like a hysteresis loop. The threshold voltage here is $\pm 0.2V$. Within this range of input voltage, the memristor shows minimal resistance, and this state is considered ON state of the memristor. Outside this range the memristor shows very high resistance, and this state is considered OFF for the memristor.

Figure 3: I-V characteristics of generic voltage controlled memristor model [14]

In Fig. 3, the I-V characteristic of a meristor with $R_{ON} = 100k\Omega$ and $R_{OFF} = 10M\Omega$ is simulated with a sinusoidal input, $v = p \sin 2\pi ft$ having amplitude $p = 0.25V$, frequency $f = 1Hz$, memristor parameter $a = 10$ and initial state of memristive system $x = -2$. For design and practical implementation purposes, memristors have tuneable threshold voltage, on-resistance and off-resistance.

III. PROPOSED BUILDING BLOCKS

A basic 1-bit Arithmetic Logic Unit (ALU) takes two inputs and gives one output depending on the selection bits or OP-code. The ALU may perform different logical and conditional operations along with arithmetic operations. The proposed ALU uses several building blocks to implement these features. Logic blocks and multiplexers make up the structure of the ALU.

Figure 4: AND Gate using MRL

Figure 5: OR Gate using MRL

The AND and OR logic gates are formed with Memristor Ratioed Logic (MRL). It uses voltage threshold based logic, rather than memristance based threshold. The gates take two binary inputs, considering high voltage as logic '1' and low voltage as logic '0'. The output is also a logic state conforming to the voltage. For the proposed model, 1.8V denotes logic '1' and 0V denotes logic '0'.

Constructing bigger logic circuits using only AND and OR gates is counter-intuitive, as they only produce positive

Figure 6: Schematic of proposed memristor-CMOS hybrid block

logic. Using memristor to implement inverter is a fundamental area of research [17]. Inversion is necessary in complex logic operations. For this, memristor-CMOS hybrid structures have been proposed in previous works [13]. The hybrid structure uses 180nm CMOS for logic inversion. Memristor-CMOS hybrid gates hold advantage over pure CMOS gates in higher area efficiency. Hence, these hybrid gates can be exploited in conventional computing architectures.

Memristor functions as a resistor in each of its state. Significant signal degradation is observed when a large circuit is constructed purely using memristor. Which is why, MRL gates produce highly degraded output when cascaded directly [9]. The hybrid memristor-CMOS logic block proposed by Mehri Teimoori et al. [13] is also affected by this problem. This block is modified to reduce the signal loss and used as a building block of ALU in this work. Two inverters are inserted into the block to avoid direct connection of memristor gates. As a result, the output remains stable when multiple blocks are cascaded. This modified block is termed as 'nand-nor-xor'

Figure 7: Output of MRL gates within proposed 'NAND-NOR-XOR' block

Figure 8: Logical operations of the proposed 'NAND-NOR-XOR' block

block and Fig. 6 shows its structure.

The proposed block takes in two binary inputs and gives three different logical outputs- NAND, NOR and XOR. The two input signals are first processed simultaneously through memristive AND and OR gates. The output of MRL AND gate is marked by node 'C', and the output of MRL OR gate is marked by node 'D' inside the block. The output graphs are shown in Fig. 7.

The signals at node 'C' and 'D' are then processed through two CMOS inverters, which give the NAND and NOR outputs, marked with nodes 'E' and 'F' respectively. The next stage of the block uses a CMOS circuit. The NAND signal at node 'E' is connected to the source of a PMOS. The NOR signal at node 'F' is the common input at the gate of both the NMOS

Figure 9: Modified 2-to-1 multiplexer block(MUX)

Figure 10: Outputs at different nodes of the proposed 2-to-1 MUX

and PMOS. The XOR signal is taken from the common drain connection node. The NAND, NOR and XOR outputs are shown in Fig. 8.

It is evident from the graphs that both the input and the output voltage levels are 1.8V, which is equal to the supply voltage of the CMOS inverter. In the proposed block, output signals are only taken from associated CMOS circuits. The proposed ALU model uses outputs from CMOS circuits only to ensure stability and consistency throughout the circuit.

The arithmetic logic unit has many functionalities, but gives only one output depending on the selection bits. This requires the use of a multiplexer. This work proposes a modified

Figure 11: 4-to-1 multiplexer cascading 2-to-1 multiplexers

2-to-1 multiplexer(MUX) to reduce signal degradation and then cascade it to construct a 4-to-1 multiplexer.

The proposed 2-to-1 multiplexer circuit is shown in Fig. 9. This multiplexer is developed by combining the outputs of two MRL AND gates with an MRL OR gate, followed by a CMOS inverter to produce the final output. The outputs of MRL AND gates at node 'E' and 'F', MRL OR gate at node 'G' and the final output of the block are shown in Fig. 10. In the proposed ALU unit, the output of the inverter is used for signal propagation. Hence, the output of the proposed block is the inversion of the selected input signal.

The output of a single modified two-to-one multiplexer unit is inverted, but it can be used as a block unit to construct larger multiplexer units. The use of an inverter at the output effectively avoids signal loss inside the circuit and substitutes function of a buffer with less logic elements. Fig. 11 shows how a 4-to-1 multiplexer is constructed cascading modified 2-to-1 units. It is evident from the schematic that the output of 4-to-1 multiplexer is no longer inverted.

For the MRL gates used to construct this hybrid architecture, a constant current flows through the gates between the two inputs, which causes a higher static power consumption for the opposite input signals. The static power is given by [9] for MRL gates used as,

$$P_{static} = \frac{V_{high}^2}{R_{ON} + R_{OFF}} \quad (3)$$

In this work, memristor parameters $R_{ON} = 100k\Omega$ and $R_{OFF} = 10M\Omega$ are used for $V_{High} = 1.8V$. It results to $P_{static} = 0.32\mu W$; which is much lower static power consumption in comparison with the previous works [9], [11], [18].

The proposed building blocks have inverters with 1.8V power supply, which is suitable for 180nm CMOS transistors to keep the signal output stable throughout the ALU circuit. This is particularly useful as connecting the components in a much larger circuit still gives an output signal without significant deterioration. These blocks are then connected to construct the 1-bit Arithmetic Logic Unit (ALU) architecture.

IV. ARCHITECTURE OF ALU

The 1-bit ALU proposed in this work utilizes advantages of the memristor-CMOS hybrid circuits to implement logical, arithmetic and conditional operations. The full set of operations and op-codes are listed in Table I. The operations of the ALU can be divided into three types for ease of discussion- arithmetic operations; conditional operations; logical operations.

These operations are implemented using the proposed ALU circuit in Fig. 12. It takes two binary inputs, labeled A and B. Provision of one carry in (C_{in}) bit and one conditional bit termed 'Less' are also included. Cascading 1-bit ALUs to construct larger ALUs require these two bits for expanding arithmetic and conditional operations. The ALU gives a 1-bit binary output and a binary flag bit C_{out} .

The architecture of proposed ALU integrates four 'nand-nor-xor' blocks, one MRL AND gate, two CMOS

Figure 12: Schematic of proposed memristor-CMOS hybrid 1-bit ALU

Table I: Table for Operations and OP-Code of proposed ALU

SL No.	OP Code	Operation	Output
1	0000	NAND	$\overline{AB}$
2	0001	NOR	$\overline{A + B}$
3	0010	SUM	$A \oplus B \oplus C_{in}$
4	0011 or 1111	XOR	$A \oplus B$
5	0110	SUB	$A \oplus \overline{B} \oplus 1$
6	0111 or 1011	XNOR	$\overline{A \oplus B}$
7	1x10	SLT	SLT
8	1100	OR	$A + B$
9	1101	AND	AB

inverters, one 2-to-1 multiplexer and one 4-to-1 multiplexer. The ‘nand-nor-xor’ blocks placed immediately after the inputs perform controlled inversion. The next block is used for logical operations of NAND, NOR and XOR. The last block combined with a MRL AND gate and inverter forms a full adder. The 2-to-1 multiplexer controls the conditional operation and lastly, the 4-to-1 multiplexer displays the output selected using OP-code.

The arithmetic operations are Addition (SUM) and Subtraction (SUB). The 1-bit ALU implements a full adder, taking two inputs and C_{in} to perform addition. C_{in} and C_{out} bits enables expanding the ALU to higher bit sizes. Subtraction operation uses 2’s complement method. The C_{in} bit is set as ‘1’ for SUB operation.

The conditional operation SLT is used to notify when minuend (input A) is less than the subtrahend (input B) during subtraction. It gives ‘1’ as output if Input A is less than Input B while giving ‘0’ for vice versa. The simulated output for arithmetic and conditional operations of 1-bit ALU are shown in Fig. 13. The ALU also performs six logical operations- NAND, AND, NOR, OR, XOR and XNOR. Output wave-forms for these operations are presented in Fig. 14.

The 1-bit ALUs can be cascaded to construct larger ALUs. The Op-codes remain same for all the blocks. The structure of a 4-bit ALU is shown in Fig. 15. Here, C_{in} for the first block is shorted with OP2 to correspond with addition or subtraction directive. In the consecutive stages, C_{out} of previous stage becomes C_{in} for that stage.

The conditional operation is set depending upon the most significant bit (MSB) of the ALU. The “Set” bit in the Most Significant Bit (MSB) ALU and the “Less” bits are for the conditional operation SLT. During SLT operation of a multiple bit cascaded ALU, it performs subtraction from Input A to B and then feeds the sign bit of the result into the ALU’s least significant “Less” bit while all other “Less” bits are defaulted to zero. The “Set” bit in the MSB unit is taken from the node labeled “in0” in the 2-to-1 multiplexer and fed to the “Less” bit of LSB unit. Rest of the “Less” bit are “0” by default.

The signal degradation for the proposed 1-bit ALU block for the worst case scenario produces $\sim 17.2 \mu V$ drop for bit ‘1’ and $\sim 83.74 mV$ higher output for bit ‘0’. For a supply voltage of 1.8V, the degradation for bit ‘1’ is about $(0.0000172 \div 1.8) \times 100 = 0.00095\%$ and for bit ‘0’ is about $(0.08374 \div 1.8) \times 100 = 4.65\%$. Due to this is low signal degradation, the architecture is highly scalable.

V. RESULTS AND DISCUSSION

Proposed memristor-CMOS integrated structure ALU optimizes chip area and minimizes signal degradation. The size of the memristor model used in this work is $\sim 3nm$ with area approximately $9nm^2$. For the 180nm CMOS components, the length of an NMOS is $\sim 180nm$ and width is $\sim 400nm$. The width of a PMOS for the same CMOS is $\sim 800nm$ having the same length as the NMOS. The MRL gates are combined with the 180nm CMOS inverters, which makes the chip area of each proposed block much smaller than it would be using only CMOS technology. Hence, the proposed 1-bit ALU has much smaller area than conventional ALUs.

Figure 13: Arithmetic operations of the proposed block

Keeping the size of memristor and CMOS in mind, it is easy to compare the total area covered by each gate and block by comparing the number of memristors and transistors used. A comparative study is given in Table II. The number of transistor counts for different gates for only CMOS architecture are referenced from the work of Kumar et al. [11]

The comparison in Table II shows that the proposed structure uses much less number of transistors and instead used memristor MRL logic gates. This translates into smaller chip area. The output signal is consistent without much degradation. Use of inverters by part instead of whole buffers in one place, the number of CMOS used goes down. In previous works, directly cascading multiple MRL gates shows severe signal

Figure 14: Logical operations of the proposed ALU

loss ($\sim 15\%$) [9]. This work reduces this loss to make output signal degradation nominal ($\sim 4.65\%$).

In the proposed ALU, the worst case of propagation delay occurs for 'SUM' operation with $C_{in} = 1$. The propagation delay is compared with the delay of the CMOS-only architecture in Table III. It shows 92.83% improvement over standard 180nm CMOS ALU in the proposed hybrid structure.

Figure 15: Architecture of a 4-bit ALU cascading 1-bit ALUs

Table II: Component count comparison between different structures

Unit	Proposed Hybrid Architecture		CMOS [11]
	Memristor	Transistor	Transistor
AND	2	0	6
OR	2	0	6
XOR	4	6	12
Inverter	0	2	2
2-to-1 Mux	6	4	12
4-to-1 Mux	18	12	36
1-bit ALU	42	44	120

Table III: Delay comparison for worst case between different structures

Unit	Proposed Hybrid Architecture	CMOS-only Architecture	Improvement (%)
Propagation Delay(ns)	487.38	6794.69	92.83%

VI. CONCLUSION

The ALU architecture in this work focuses on functionality, modularity, transistor count minimization, signal loss reduction and delay improvement. Using voltage threshold based MRL gates along with 180nm CMOS transistor, this work is simulated in LTSpice to verify the proposed models and the ALU. The reduction in transistor count shows that our

proposed ALU is much smaller in area than purely CMOS architecture ALU. It also improves on previous ALU models of CMOS-MRL hybrid architecture with more operational functions [11]. The signal degrades by only $\sim 4.65\%$ due to the modified architecture. In future, there is scope to work on the total power consumption and switching characteristics of the proposed model. This work hopes to pave the path of using hybrid memristive circuits to design more complex computational models.

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