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An Enhanced Ultra-High Gain Quasi Z-source Inverter

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Abstract—This paper proposes an enhanced ultra-high gain quasi Z-source inverter (EUHG-qZSI). The proposed topology combines single switched inductor unit with single switched capacitor unit to achieve the ultra-high voltage gain. This single-stage inverter provides very high gain profile with limiting value of shoot-through duty ratio of 0.186. The numerator factor of its gain is also high. Thus, the suggested inverter achieves higher voltage gain than the existing ultra-high/high gain/two-switched topologies. It also retains desirable qualities such as common ground with input DC supply and continuous source-side current. The derivations of steady-state voltage gain, parameter values, current and voltage stresses of its components, input current ripple and losses in different components are given to analyze the operation and characteristics of proposed inverter. In this respect, various performance issues are compared with that of existing topologies to indicate its decent performances. Both simulation and experimental verifications of the suggested inverter are performed. The observations of both studies match well with the theoretical analysis.

Index Terms— Enhanced ultra-high gain quasi Z-source inverter (EUHG-qZSI), shoot-through period, voltage gain, current and voltage stresses, loss calculation.

I. INTRODUCTION

THE z-source/ quasi z-source inverter (ZSI/qZSI) [1, 2] is recently focused in the research and development field of power electronics converter. This topology is mainly used in the context of solar or fuel energy conversion system or electric vehicle applications. Various merits of the single-stage inverter can be mentioned as, capability of both buck and boost operation during DC-AC voltage conversion, reliable in terms of immunity from false firing by electro-magnetic interference or permissible shoot-through state and distortion-free effect due to dead-time less switching signals. The qZSI is the advanced option over ZSI for lesser voltage stresses on different components, continuous source current and sharing of ground with input DC supply. Various topological developments are still going on with the main objective as more enhancement of voltage gain profile. The increased voltage gain with less shoot-

through period results in high modulation index of the inverter. This causes reduced harmonic contents in output AC-side voltage/current i.e. reduction of filtering requirements.

The qZSI topologies can be categorized and discussed as,

i) *Coupled inductor type* - This topology [3-5] changes voltage gain by adjusting turn ratio. But this converter is prone to spike in DC link voltage due to leakage inductance effect [6].

ii) *Extended/enhanced boost type* - The diode-assisted (DA) and capacitor-assisted (CA) topologies are used to improve the gain. The two topologies are regarded as extended boost configuration [7]. But the gain value is not satisfactory. Thus, enhanced boost qZSI (EB-qZSI) [8] is proposed to further improve the voltage gain. The passive components used in extended/enhanced boost type are more.

iii) *Switched inductor type* - Switched inductor topology [9-12] is used in front-end instead of single inductor to improve the gain. Here, supply-side current is subjected to substantial amount of ripple.

iv) *Active switched capacitor type* - This configuration [10] reduces inductor in the boosting network in expense of higher capacitor voltage stress.

v) *quasi switched type* - The quasi-switched boost inverter (qSBI) [13] is also proposed to reduce number of passive components and also, it consists of single active power switch. But, more gain is desired. Therefore, switched-inductor qSBI (SL-qSBI) [14] is proposed in expense of significant ripple in input current.

vi) *High gain/boost type* - Two high gain qSBI (HG-qSBI) are proposed in [15]. These do not share ground of its supply. An enhanced boost active-switched qZSI (EB-ASqZSI) [16] having common ground is proposed, whose voltage gain equals to HG-qSBI. In the progress of time, one high boost converter [17] is suggested to further improve the gain. It has moderate input current ripple. There is possibility of further improvement in boosting level.

vii) *Ultra-high gain* - The very recent trend is the development of ultra-high gain qZSI. The multi-cell ultra-high gain topologies are proposed in [18]. But it uses more active switches in the impedance network, which can cause more

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switching losses. In [19], an ultra-high gain topology of qZSI family is proposed by taking combination of single switched inductor unit and active switched capacitor circuit for further improving the voltage gain also, it consists of lesser number of active switches in comparison to before mentioned multi-cell topology. Still, gain improvement is possible.

In this paper, an enhanced ultra-high gain qZSI topology (EUHG-qZSI) is proposed by combining a switched inductor cell and an active switched capacitor cell, which is shown in Fig. 1. Here, the shoot-through duty ratio is limited within 0.186 and the numerator factor of its gain is 2 times of (1+shoot-through duty ratio). The proposed topology uses same numbers of passive elements (both inductor and capacitor) and active switches to that of the above said ultra-high gain qZSI [19]. Two diodes are only more in proposed inverter, but enhanced ultra-high gain profile is achieved.

Fig. 1: Proposed enhanced ultra-high gain quasi Z-source inverter.

Section II proposes operational modes of proposed EUHG-qZSI, derivation of its boosting factor, design of its parameters and small signal dynamic modeling. Voltage and current stresses of its different components, calculation of various losses and comparisons of various performances are presented in section III. The working of the proposed inverter through both simulation and experimental works are illustrated in section IV. Section V gives conclusions.

II. PROPOSED ENHANCED ULTRA-HIGH GAIN QZSI

The operation and its design, voltage boost expression of enhanced ultra-high gain quasi Z-source inverter (EUHG-qZSI) are discussed here.

A. Modes

Both shoot-through (ST) and non shoot-through (NST) states of its operation are presented along with dynamic equations.

1) ST mode

In ST mode, the circuit representation of proposed inverter is presented in Fig. 2(a). Here, the ON/OFF conditions of various switching devices are: S_1 - S_7 : ON; D_1 , D_2 and D_4 : OFF (reverse-biased); D_3 : ON (forward-biased). The conditions of passive components are: L_1 , L_2 and C_3 : Charging; C_1 , C_2 and C_4 : Discharging. The dynamic equations in ST mode are given in (1).

2) NST mode

In NST mode, the effective circuit diagram is shown in Fig. 2(b). Here, the states of various active and passive components are: S_1 - S_7 : ON; D_1 , D_2 and D_4 : OFF (reverse-biased); D_3 : ON (forward-biased), L_1 , L_2 and C_3 : Charging; C_1 , C_2 and C_4 :

Discharging. The equations of this mode are provided in (2).

Fig. 2: Circuits during both modes of operation.

$$\left\{ \begin{array}{l} L_1 \frac{di_{L1}}{dt} = V_{in} + V_{C2} + V_{C3} \\ L_2 \frac{di_{L2}}{dt} = L_3 \frac{di_{L3}}{dt} = V_{C1} + V_{C3} \\ C_1 \frac{dv_{C1}}{dt} = -I_{L2} - I_{L3}; C_2 \frac{dv_{C2}}{dt} = -I_{L1} \\ C_3 \frac{dv_{C3}}{dt} + C_4 \frac{dv_{C4}}{dt} = -I_{L1} - I_{L2} - I_{L3} \\ \hat{V}_{dc} = 0; V_{C3} = V_{C4} \\ V_{D1} = -(V_{C1} + V_{C2} + V_{C3}); V_{D3} = -(V_{C1} + V_{C3}) \\ V_{D2} = V_{D4} = V_{D6} = 0; V_{D5} = V_{D7} = -V_{C3} \end{array} \right. \quad (1)$$

$$\left\{ \begin{array}{l} L_1 \frac{di_{L1}}{dt} = V_{in} - V_{C1} \\ L_2 \frac{di_{L2}}{dt} = L_3 \frac{di_{L3}}{dt} = 0.5(V_{C1} - V_{C3}) \\ C_2 \frac{dv_{C2}}{dt} + C_3 \frac{dv_{C3}}{dt} - C_4 \frac{dv_{C4}}{dt} = I_{L2} = I_{L3}; C_4 \frac{dv_{C3}}{dt} = -I_{dc} \\ C_1 \frac{dv_{C1}}{dt} + C_3 \frac{dv_{C3}}{dt} = I_{L1} - I_{dc} \\ \hat{V}_{dc} = V_{C3} + V_{C4} \\ V_{D1} = V_{D3} = V_{D5} = V_{D7} = 0; V_{D2} = V_{D4} = 0.5(V_{C1} - V_{C3}) \\ V_{D6} = -V_{C3} = -V_{C4} \end{array} \right. \quad (2)$$

B. Patterns of Various Quantities of Boosting Network

Fig. 3 shows different waveforms of voltage and currents for various passive and active elements of proposed boosting network. There are two shoot-through states in a switching cycle. In the work of this paper, maximum constant boost control (MCBC) [20] pulse width modulation method is used. Here, the relationship between shoot-through duty ratio (D) and modulation index (M) is given by,

$$D = 1 - \sqrt{3}M/2 \quad (3)$$

Fig. 3: Different theoretical waveforms of boosting circuit variables.

C. Voltage Gains

By applying Volt-Sec balance in the cases of inductors, the following equations are obtained as,

$$\begin{cases} D(V_{in} + V_{C2} + V_{C3}) + (1-D)(V_{in} - V_{C1}) = 0 \\ D(V_{C1} + V_{C3}) + 0.5(1-D)(V_{C1} - V_{C3}) = 0 \end{cases} \quad (4)$$

From (4), the capacitor voltages are provided as,

$$\begin{cases} V_{C1} = \frac{1-3D}{1-5D-2D^2} \cdot V_{in}; & V_{C2} = \frac{4D}{1-5D-2D^2} \cdot V_{in} \\ V_{C3} = \frac{1+D}{1-5D-2D^2} \cdot V_{in}; & V_{C4} = \frac{1+D}{1-5D-2D^2} \cdot V_{in} \end{cases} \quad (5)$$

The boosting gain is expressed from (5) as,

$$\hat{V}_{dc} = V_{C3} + V_{C4} = 2V_{C3} = \frac{2(1+D)}{1-5D-2D^2} \cdot V_{in} \quad (6)$$

Thus, boosting gain (B) of proposed impedance network is,

$$B = \frac{\hat{V}_{dc}}{V_{in}} = \frac{2(1+D)}{1-5D-2D^2} \quad (7)$$

The denominator of (7) gives the range of shoot-through duty ratio as, $0 < D < 0.186$.

Here, the net voltage gain (G) is written as,

$$G = M \cdot B/2 = \frac{(1+D) \cdot M}{1-5D-2D^2} \quad (8)$$

D. Design of Passive Parameters of Boosting Circuit

Thus, the inductor values are,

$$\begin{cases} L_1 = \frac{D(1-D^2)}{(1-5D-2D^2)} \cdot \frac{V_{in}}{\Delta I_{L1} F_s} \\ L_2 = L_3 = \frac{D(1-D)}{(1-5D-2D^2)} \cdot \frac{V_{in}}{\Delta I_{L2} F_s} \end{cases} \quad (9)$$

The capacitor values are mathematically represented as,

$$\begin{cases} C_1 = \frac{3}{2} \frac{D(1+D)M^2}{(1-5D-2D^2)^2} \frac{V_{in}}{R \Delta V_{C1} F_s} \\ C_2 = \frac{3}{2} \frac{D(1+D)^2 M^2}{(1-5D-2D^2)^2} \frac{V_{in}}{2R \Delta V_{C2} F_s} \\ C_3 = \frac{3}{4} \frac{(1+D)(1-D)^2 M^2}{(1-5D-2D^2)} \frac{V_{in}}{2R \Delta V_{C3} F_s} \\ C_4 = \frac{3}{4} \frac{(1+D)(1-D)^2 M^2}{(1-5D-2D^2)} \frac{V_{in}}{2R \Delta V_{C4} F_s} \end{cases} \quad (10)$$

III. PERFORMANCES

The voltage and current stresses and losses of different elements are derived and presented here.

A. Voltage and Current Stresses

The voltage and current stresses of various elements of proposed configuration are derived and presented in Table I.

B. Ripple in Input Current

The ripple in the supply-side current of proposed inverter is less due to presence of input-side inductor ' L_1 ', which can be quantified as,

$$\Delta I_{L1} = \frac{D(1-D^2)}{(1-5D-2D^2)} \cdot \frac{V_{in}}{L_1 F_s} \quad (11)$$

C. Comparisons of Various Performances

Plots of voltage gain comparisons are presented in Fig. 4. Various characteristics and features of proposed EUHG-qZSI are compared with that of existing high gain and ultra-high gain topologies in Table I.

Fig. 4: Voltage gains.

D. Computation of Losses

The loss calculations for different components are discussed separately as follows:

1) Losses in Inductors

Here, it is considered that the core losses are very small in comparison to that of conduction losses in inductors. The conduction losses in inductors are given by,

$$P_L = I_{L1(RMS)}^2 r_{L1} + I_{L2(RMS)}^2 r_{L2} + I_{L3(RMS)}^2 r_{L3} \quad (12)$$

In (18), ' r_{L1} ', ' r_{L2} ' and ' r_{L3} ' are series parasitic resistances of three inductors. In (12), RMS values of inductors ($I_{L1(RMS)}$, $I_{L2(RMS)}$, $I_{L3(RMS)}$) are given by,

$$\begin{cases} I_{L1(RMS)} = \frac{2(1+D)}{(1-D)} \frac{1}{(1-5D-2D^2)} I_{DC} \\ I_{L2(RMS)} = I_{L3(RMS)} = \frac{2}{(1-D)(1-5D-2D^2)} I_{DC} \end{cases} \quad (13)$$

2) Losses in Capacitors

The losses of capacitors in terms of ESRs ' r_{C1} ', ' r_{C2} ', ' r_{C3} ' and ' r_{C4} ' are provided by,

$$P_C = I_{C1(RMS)}^2 r_{C1} + I_{C2(RMS)}^2 r_{C2} + I_{C3(RMS)}^2 r_{C3} + I_{C4(RMS)}^2 r_{C4} \quad (14)$$

The above RMS currents ($I_{C1(RMS)}$, $I_{C2(RMS)}$, $I_{C3(RMS)}$, $I_{C4(RMS)}$) are derived as,

$$\begin{cases} I_{C1(RMS)} = \frac{4\sqrt{D/1-D}}{(1-D)(1-5D-2D^2)} I_{DC} \\ I_{C2(RMS)} = \frac{2(1+D)\sqrt{D/1-D}}{(1-D)(1-5D-2D^2)} I_{DC} \\ I_{C3(RMS)} = \frac{(-2D^4 - D^3 + 11D^2 - D + 1)}{\sqrt{D}(1-D)^{3/2}(1-5D-2D^2)} I_{DC} \\ I_{C4(RMS)} = \left(\sqrt{1-D/D}\right) I_{DC} \end{cases} \quad (15)$$

3) Losses in Diodes

The net loss (P_D) in diodes consist of reverse recovery loss, loss due to forward voltage drop and conduction loss, which are mathematically written as,

$$P_D = P_{rr} + P_{fd} + P_{oh} \quad (16)$$

In (16),

$$\begin{cases} P_{rr} = 7Q_{rr} F_s \hat{V}_{dc} \\ P_{fd} = \left(I_{D1(AVG)} + I_{D2(AVG)} + I_{D3(AVG)} + I_{D4(AVG)} \right. \\ \quad \left. + I_{D5(AVG)} + I_{D6(AVG)} + I_{D7(AVG)} \right) \cdot V_F \\ P_{oh} = \left(I_{D1(RMS)}^2 + I_{D2(RMS)}^2 + I_{D3(RMS)}^2 + I_{D4(RMS)}^2 \right. \\ \quad \left. + I_{D5(RMS)}^2 + I_{D6(RMS)}^2 + I_{D7(RMS)}^2 \right) \cdot r_D \end{cases} \quad (17)$$

TABLE I
COMPARISONS OF VARIOUS HIGH/ULTRA-HIGH GAIN TOPOLOGIES

Item	rASLB-qZSI [11]	EB-qZSI [8]	HP-ZSI [12]	HMcaSL/SC-qZSI [18]	UHG-qZSI [19]	Proposed (EUHG-qZSI)
L	3	4	4	2	3	3
C	3	4	3	2	4	4
D	6	5	7	7	5	7
S	7	6	7	8	7	7
B	$\frac{1+D}{1-4D+D^2}$	$\frac{1}{1-4D+2D^2}$	$\frac{2(1+D)}{1-4D+D^2}$	$\frac{1+D}{1-5D}$	$\frac{2}{1-5D}$	$\frac{2(1+D)}{1-5D-2D^2}$
G (MCBC-PWM)	$\frac{M(4-\sqrt{3}M)}{3M^2+4\sqrt{3}M-8}$	$\frac{M}{3M^2-2}$	$\frac{2M(4-\sqrt{3}M)}{3M^2+4\sqrt{3}M-8}$	$\frac{M(4-\sqrt{3}M)}{2(5\sqrt{3}M-8)}$	$\frac{2M}{5\sqrt{3}M-8}$	$\frac{M(4-\sqrt{3}M)}{-3M^2+9\sqrt{3}M-12}$
V_C/V_{in}	$\frac{DB}{(1-D)B}$	$\frac{(1-D)^2 B}{D(1-D)B}$ $\frac{D(2-D)B}{(1-3D+D^2)B}$	$\frac{B}{B/2}$ $\frac{DB/(1-D)}{(1-D)B/(1+D)}$	B	$\frac{B/2}{B}$	$\frac{(1-3D)B/(2+2D)}{2DB/(1+D)}$ $\frac{B/2}{B/2}$
V_D/V_{in}	$\frac{DB}{(1-D)B}$ $\frac{DB(2-D)/(1+D)}{(2-3D+D^2)B/(1+D)}$	$\frac{B}{3DB}$ $\frac{(1-3D)B}{(1-3D)B}$	$\frac{B}{B/2}$ $\frac{DB/(1-D)}{(1-D)B/(1+D)}$	B	$\frac{B/2}{B}$	$\frac{B/2}{2DB/(1+D)}$ $\frac{(1-D)B/(1+D)}{B}$
V_{S7}/V_{in}	B	$B/2$	B	B	B	$B/2$
I_L/I_{dc}	$\frac{B(1-D)}{B(1-D)^2}$	$\frac{B(1-D)}{B(1-D)^2}$	$\frac{(1-D)B/(1+D)}{(1-D)B/(1+D)}$	$\frac{(1-D)B/(1+D)}{(1-D)B/(1+D)}$	$\frac{B(1-D)}{B(1-D)/2}$	$\frac{B/(1-D)}{B/(1-D^2)}$
ΔI_{in}	$DB(1-D)/(1+D)$	ΔI_{L1}	$(1-D)I_L$	$(1-D)I_L$	ΔI_{L1}	ΔI_{L1}

In (17), the average and RMS currents of different diodes are,

$$\begin{cases}
 I_{D1(AVG)} = \frac{2(1+D)}{(1-D)(1-5D-2D^2)} I_{DC}; I_{D1(RMS)} = \frac{2(1+D)}{(1-D)^{3/2}(1-5D-2D^2)} I_{DC} \\
 I_{D2(AVG)} = I_{D4(AVG)} = \frac{2D}{(1-D)(1-5D-2D^2)} I_{DC}; \\
 I_{D2(RMS)} = I_{D4(RMS)} = \frac{2\sqrt{D}}{(1-D)(1-5D-2D^2)} I_{DC} \\
 I_{D3(AVG)} = \frac{2}{(1-5D-2D^2)} I_{DC}; I_{D3(RMS)} = \frac{2}{\sqrt{1-D}(1-5D-2D^2)} I_{DC} \\
 I_{D5(AVG)} = I_{D7(AVG)} = \frac{(-2D^4 - D^3 + 11D^2 - D + 1)}{(1-D)(1-5D-2D^2)} I_{DC}; \\
 I_{D5(RMS)} = I_{D7(RMS)} = \frac{(-2D^4 - D^3 + 11D^2 - D + 1)}{(1-D)^{3/2}(1-5D-2D^2)} I_{DC} \\
 I_{D6(AVG)} = \frac{(-2D^4 - D^3 + 11D^2 - D + 1)}{(1-D)(1-5D-2D^2)} I_{DC}; I_{D6(RMS)} = \frac{(-2D^4 - D^3 + 11D^2 - D + 1)}{\sqrt{D}(1-D)(1-5D-2D^2)} I_{DC}
 \end{cases} \quad (18)$$

4) Losses in MOSFET switches

The average and RMS values of current through the power switch 'S₇' are given by,

$$\begin{cases}
 I_{S7(AVG)} = \frac{(-2D^4 - D^3 + 11D^2 - D + 1)}{(1-D)(1-5D-2D^2)} I_{DC} \\
 I_{S7(RMS)} = \frac{(-2D^4 - D^3 + 11D^2 - D + 1)}{\sqrt{D}(1-D)(1-5D-2D^2)} I_{DC}
 \end{cases} \quad (19)$$

The both losses in 'S₇' (P_{SW7}, P_{COND7}) are,

$$\begin{cases}
 P_{SW7} = \frac{(T_{on} + T_{off})}{2} \cdot F_S \cdot V_{S7} \cdot I_{S7(AVG)} \\
 P_{COND7} = I_{S7(RMS)}^2 \cdot r_{S7}
 \end{cases} \quad (20)$$

The 'T_{on}' and 'T_{off}' indicate delay during turn-on and turn-off of the switch. The 'r_{s7}' represent on-state resistance of switch. The different losses (P_{SW(INV)} - switching loss, P_{COND(INV)} - conduction loss) in the switches of inverter-bridge are given as,

$$\begin{cases}
 P_{SW(INV)} = 6 \cdot \frac{(T_{ON} + T_{OFF})}{2} \cdot F_S \cdot \hat{V}_{DC} \cdot \frac{I_{sh}}{3} \\
 P_{COND(INV)} = 6 \cdot I_{S_{inv}(RMS)}^2 \cdot r_{S_{inv}}
 \end{cases} \quad (21)$$

In (21), 'r_{s_{inv}}' represent on-state resistance of the switch of inverter bridge. The shoot-through current (I_{sh}) and RMS current (I_{S_{inv}(RMS)}) through inverter power switch are,

$$I_{sh} = I_{L1} + I_{L2} + I_{L3} \quad (22)$$

$$I_{S_inv(RMS)} = \sqrt{\frac{D}{9} \cdot I_{sh}^2 + \frac{16(1-D)P_o^2}{9\pi^2 M^2 B^2 V_{DC}^2 \cdot \cos^2 \phi}} \quad (23)$$

IV. VERIFICATIONS AND RESULTS

The working and performances of proposed EUHG-qZSI (parameters are given in Table II) are verified in both simulation and hardware platforms. These are described as follows:

A. Validation in Simulation Platform

The proposed EUHG-qZSI is realized in MATLAB-SIMULINK software platform. The responses of output-side load voltage, current and phase difference are given in Fig. 5 for load resistance and inductance of 50 Ω and 60 mH. Here, per phase load voltage is 110 V (r.m.s.) and corresponding current is 2.89 A (r.m.s.) having lag phase angle of 20.65°. The output-side unfiltered voltage (per phase) of EUHG-qZSI is shown in Fig. 6. The FFT spectrums of the voltage is also shown

TABLE II
SPECIFICATIONS

Parameters	Values
V_o (rms), F_o	110 V, 50 Hz
L_1, L_2, L_3	1 mH,
C_1, C_2, C_3, C_4	470 μ F
L_f	2 mH
C_f	50 μ F
F_s	10 kHz

in Fig. 6. In this context, various responses (inductor currents and capacitor voltages) of proposed impedance network for DC input voltage of 70 V are presented in Fig. 7. The MCBC PWM method is applied here.

In the study, the amplitude of phase voltage equals to 155.5 V (110 V_{rms}). Thus, overall gain for the three-phase EUHG-qZSI is given by, $155.5 / (70/2) = 4.442$. From this net gain, the 'M' is obtained and its value is 0.9918 p.u as per the expression in Table II for MCBC case. Here, boosting factor (B) is found as, $4.442 / 0.9918 = 4.4787$. The corresponding 'D' is 0.098 p.u. as per (7). The voltages of four number capacitors can be computed as 100.69 V, 55.90 V, 156.60 V and 156.60 V respectively as per (5). The expected value of DC link voltage should be $2 \times 156.60 = 313.20$ V as per (6). In the above discussions, steady state values of various variables are calculated on the basis of theoretical analysis of this paper for the selected values of input voltage of 70 V and load voltage of 110 V_{rms} .

The steady state values of different variables of proposed impedance network from the simulation study are checked in respect of above said calculated values. The responses are shown in Fig. 7. Their respective values are marked in Fig. 7. The amplitude of DC-link voltage during non shoot-through period is found as, 312.2 V. The corresponding boosting factor is $(312.2/70) = 4.46$ i.e. the value of 'D' equals to 0.097 p.u. This agrees well with its theoretical value. The steady state values of obtained voltages of different capacitors are found as

100.5 V, 55.7 V, 156.2 V and 156.2 V respectively.

Thus, obtained values of different responses in this study agree with that of respective calculated values.

Fig. 5: Per phase filtered load voltage and current along with phase difference.

Fig. 6: Output phase voltage of EUHG-qZSI and corresponding spectrums.

Fig. 7: Various simulation waveforms for proposed boosting circuit.

B. Validation in Hardware Platform

The operations of proposed inverter are also done using hardware set up. The inverter is framed using power MOSFET (TOSHIBA: 2sk3878) switches. The TLP 250 chips are used to drive various switches. The required PWM signals are generated with the help of dsPIC 30F4011 controller. The proposed inverter is fed from a DC-power supply (ITECH: IT 6514C). Various practical waveforms are graphically traced by means of a digital storage oscilloscope (KEYSIGHT: DSOX2024A).

The DC supply voltage of the power source is fixed at a value of 70 V. Here, the resistor having value of 50Ω and inductor of 60 mH are taken as AC load. Various obtained responses (per phase load voltage and current) of load-side variables are presented in Fig. 8(a). The respective value of voltage, current and phase difference are noticed as 110 V (r.m.s), 2.04A (r.m.s) and 20° (lag). Measured unfiltered voltage (per phase) waveform is shown in Fig. 8(b). Fig. 8(b) also shows its spectrums. In this working point, the captured responses of different important variables (voltages of four capacitors, currents through inductors and intermediate DC-link voltage) are presented in Fig. 9. The amplitude of DC link voltage and voltages of four capacitor are obtained as 301.5 V, 99.1 V, 52.1 V, 151.2 V and 150.5 V respectively. These show little

difference from the respective theoretical values of the variables (313.20 V, 100.69 V, 55.90 V, 156.60 V and 156.60 V respectively). The small errors are due to presence of parasitic elements in the hardware circuit.

Fig. 8: Per phase load voltage and current along with phase difference.

In Fig. 10, the plots of obtained efficiency curves are provided at variable power outputs for different input supply voltages. Here, the efficiency values are reduced with the reduction of DC supply voltage. The reason is due to increased input current of impedance network (due to increment of boosting level), which causes relatively more conduction losses at comparatively lower input voltage condition.

(a) Supply DC voltage

(b) Capacitor voltages

(c) DC-link voltage and current in L_1 and L_2

Fig. 9: Various experimental waveforms for proposed boosting circuit.

The power losses at various components are computed for the proposed EUHG-qZSI. The power condition is chosen as 630 W and DC supply voltage is 70 V. The loss distribution is presented in Fig. 11. In the condition, net loss equals to 68 W. The loss distributions among various components are given as, diode loss of 19.08 W, inductor loss of 18.51 W, capacitor loss of 17.83 W and MOSFET loss of 12.58 W. The different parameters of components are given as, $r_{L1}=r_{L2}=110\text{m}\Omega$, $r_{C1}=r_{C2}=r_{C3}=r_{C4}=100\text{m}\Omega$, $r_D=30\text{m}\Omega$, $r_{S7}=r_{S_{inv}}=r_{DS_ON(max)}=1.3\Omega$, $V_F=1.2\text{V}$.

Fig. 10: Efficiency vs. power.

Fig. 11: Distribution of various losses.

V. CONCLUSION

One enhanced ultra-high gain quasi Z-source inverter is suggested in this paper. It combines single unit of switched inductor with an active switched capacitor unit. Various analyses on its working and performances are done in this paper. The upper limit of shoot-through duty ratio is found as 0.186, which is evident from the derived boosting factor. The numerator of the boosting gain is also reasonably high, which is $2(1+D)$. The number of passive components and active switches are similar to that of recent ultra-high gain power converter topology. Comparative features, characteristics and performances are presented in Table II to point its decent behaviour. The benefits of suggested single-stage inverter are mentioned as,

- It enhances voltage gain (Fig. 4) from that ultra-high / high boost configurations by reducing upper threshold of shoot-through duty ratio ($0 < D < 0.186$) and also, due to simultaneous increase of numerator of the boosting gain.

Thus, boosting factor is enhanced at upper range of modulation index,

- ii. Better output voltage quality i.e. reduction of harmonics can be achieved at a required voltage gain due to its operation at high range of modulation indices,
- iii. Ground sharing with input voltage supply is possible,
- iv. Insignificant amount of shoot-through current is due to suppression effect caused by input-side inductor.

The peak efficiency is found as 92.4%. Both responses of simulation and experimental studies show reasonable accuracy and also, the observations agree quite well with the analysis of the work. Thus, the real-time implementation of the proposed inverter is feasible.

REFERENCES

- [1] M. Shen, A. Joseph, J. Wang, F. Z. Peng, and D. J. Adams, "Comparison of traditional inverters and Z-source inverter for fuel cell vehicles," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1453-1463, Jul. 2007.
- [2] J. Anderson and F. Z. Peng, "Four quasi-Z-source inverters," in *Proc. IEEE Power Electron. Spec. Conf. (PESC'08)*, Jun. 2008, pp. 2743-2749.
- [3] Y. P. Siwakoti, F. Blaabjerg, and P. C. Loh, "New magnetically coupled impedance (Z-) Source networks," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7419-7434, Nov. 2016.
- [4] Y. P. Siwakoti, P. C. Loh, F. Blaabjerg, and G. Town, "Y-source impedance network," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3250-3254, Jul. 2014.
- [5] P. C. Loh, D. Li, and F. Blaabjerg, "T-Z-source inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4880-4884, Nov. 2013.
- [6] N. Zhang, G. Zhang, and K. W. See, "A Δ -Y Hybrid Impedance Network Boost Converter with Reduced Input Current Ripple," *IEEE Trans. on Power Electron.*, Vol. 33, no. 4, 2803-2808, Sep 2017.
- [7] C. J. Gajanayake, F. L. Luo, H. B. Gooi, P. L. So, and L. K. Siow, "Extended-boost Z-source inverters," *IEEE Trans. Power Electron.*, vol. 25, no. 10, pp. 2642-2652, Oct. 2010.
- [8] V. Jagan, J. Kotturu, and S. Das, "Enhanced-Boost Quasi-Z-Source Inverters with Two Switched Impedance Network," *IEEE Trans. on Ind. Electron.*, vol. 64, no. 9, pp. 6885-6897, Mar. 2017.
- [9] M.-K. Nguyen, Y. C. Lim, and J. H. Choi, "Two switched-inductor quasi z-source inverters," *IET Power Electron.*, vol. 5, no. 7, pp. 1017-1025, Aug. 2012.
- [10] A. Ho, T. Chun, and H. Kim, "Extended Boost Active-Switched-Capacitor/Switched-Inductor Quasi-Z-Source Inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5681-5690, Oct 2015.
- [11] X. Zhu, B. Zhang, and D. Qiu, "Enhanced boost quasi-z-source inverters with active switched-inductor boost network," *IET Power Electron.*, vol. 11, no. 11, pp. 1774-1787, Sept. 2018.
- [12] Y. Wang, Q. Bian, X. Hu, Y. Guan, and D. Xu, "A high-performance impedance-source converter with switched inductor," *IEEE Trans. on Power Electron.*, vol. 34, no. 4, pp. 3384-3396, Apr. 2019.
- [13] M. K. Nguyen, T. V. Le, S. J. Park, and Y. C. Lim, "A class of quasi switched boost inverters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1526-1536, Mar. 2015.
- [14] M. K. Nguyen, T. V. Le, S. J. Park, Y. C. Lim, and J. Y. Yoo, "Class of high boost inverters based on switched-inductor structure," *IET Power Electron.*, vol. 8, no. 5, pp. 750-759, May. 2015.
- [15] M. K. Nguyen, T. D. Duong, Y. C. Lim, J. H. Choi, "High Voltage Gain Quasi-Switched Boost Inverters with Low Input Current Ripple," *IEEE Trans. Ind. Informat.*, vol. 15, no. 9, pp. 4857-4866, Sept. 2019.
- [16] Y. W. Gu, Y. F. Chen, B. Zhang, "Enhanced-Boost Quasi-Z-Source Inverter with An Active Switched Z-Network," *IEEE Trans. Ind. Electron.*, vol. 65, no. 10, pp. 8372-8381, Oct. 2018.
- [17] X. Zhu, B. Zhang, D. Qiu, "A high boost active switched quasi-Z-source inverter with low input current ripple," *IEEE Trans. Ind. Informat.*, vol. 15, no. 9, pp. 5341-5354, Sept. 2019.
- [18] R. Majeed and A. H. Chughtai, "Multi-cell schemes for active-switched capacitor and active-switched-capacitor/switched-inductor quasi z-source inverters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 1739-1754, Jun. 2020.
- [19] A. Kumar, Y. Wang, M. Raghuram, P. Naresh, X. Pan and X. Xiong, "An Ultra High Gain Quasi Z-Source Inverter Consisting Active Switched Network," *IEEE Trans. on Circuits and Systems II: Express Briefs*, vol. 67, no. 12, pp. 3207-3211, Dec. 2020.
- [20] M. Shen, J. Wang, A. Joseph, F. Z. Peng, L. M. Tolbert, and D. J. Adams, "Constant boost control of the Z-source inverter to minimize current ripple and voltage stress," *IEEE Trans. Ind. Appl.*, vol. 42, no. 3, pp. 770-778, May/Jun. 2006.