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An Improved T-type Switched-Capacitor Based 3-level 3-Phase Inverter with Common Mode Voltage Elimination and Voltage Boosting Capability

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Abstract— Zero common mode voltage (ZCMV) space vector modulation (SVM) strategy applied to a three-phase multilevel inverter (MLI) eliminates the common mode voltage (CMV). However, the usage of ZCMV-SVM strategy reduces the number of levels in the output voltage and requires higher magnitude dc voltage source due to the reduced modulation depth of the employed PWM scheme. Moreover, the usage of a single dc-source in such systems may have issues with respect to capacitor voltage balancing. Taking into account all the above issues, a 3-level inverter solution is proposed in this manuscript. The complete details of the method used for developing the proposed solution using the ZCMV space vectors is also included in this paper. The proposed topology utilizes a unique combination of a T-type 3-level inverter and a switched-capacitor (SC) circuit to achieve ZCMV performance with a single dc-source of low magnitude at a reduced component count. Analysis of the CMV and terminal voltages along with the design of the SCs are presented in this paper. The proposed topology is compared with the existing topologies to prove its unique merits over the other 3LI solutions with ZCMV capability. All the claims are validated using simulation and experimental results.

Keywords— Three-phase Multilevel Inverter, Switched Capacitor, Common Mode Voltage, Space Vector Modulation, Voltage Boosting.

I. INTRODUCTION

Three-phase Multilevel Inverters (MLI) have become very popular in recent times due to their several advantages like improved THD, reduced losses etc. [1] – [5]. However, like conventional power inverters they also suffer from the issue of common mode voltage (CMV) [4]. The high frequency transition in the CMV causes a residual current or leakage current through the system parasitic capacitors which exist between the ground and system terminals. The flow of leakage or residual current deteriorates the system performance apart arising the issues related to electromagnetic interference (EMI) [6], system health deterioration [7], current distortions, safety issues etc. [8] - [9]. Therefore, it is of utmost concern to eliminate or minimize the CMV during the design of the inverter. This will reduce the size of the EMI filters and common mode chokes required to meet the requisite of various safety compliance and standards. A recent concern for the researchers is to mitigate or minimize the damaging effects of CMV in the MLIs. To avoid the CMV related adverse effects, it is essential to eliminate or reduce the high frequency transition in the CMV.

To address the abovementioned issues there are many potential solutions/methods given in the literature. Some of the solutions are as follows: (a) designing the PWM strategy to reduce the CMV [10]; (b) adding extra hardware circuitry

for reducing the common mode or terminal voltage [11]; (c) using passive components to reduce CMV and resulting leakage current [9], [12] etc. These methods are very effective and are typically employed to mitigate CMV.

Mitigation of the CMV using PWM based strategy is more popular, as it does not add any external hardware or grounding modifications. One such good solution for the complete elimination of CMV is given by the Zhang *et. al.* [10]. The given solution utilizes only the zero CMV (ZCMV) voltage space vectors (SV) in its PWM strategy to produce the required output voltage. However, due to the application of ZCMV SV modulation (SVM) the number of the levels in the output voltage are reduced. Usually the $(2n+1)$ level inverter works as a $(n+1)$ level inverter under the application of ZCMV SVM [10]. For example, a 5-level inverter reported in [13] operates as a 3-level inverter. This is because most of the SVs generated by the inverter are not used. Another major drawback of the ZCMV SVM scheme is the reduced dc-bus utilization. This again adds to the Because of this, the voltage requirement of the dc-bus [10], [13] - [15] increases. This issue can be addressed by stepping up the input voltage using a dc-dc boost converter. However, the use of an extra power converter increases the number of components and reduces efficiency. To address this issue, ZCMV SVM is modified in such a way that whenever the reference vector goes beyond the SV hexagon formed by the ZCMV vectors, nonzero CMV SVs are used [16] – [18]. A similar approach is adopted while using the 3D SVM strategy [19]. Although, these methods work well in improving the dc-bus utilization, CMV is not eliminated completely typically for the high voltage output requirement. Also, the configuration proposed in [19], has the drawback of multiple dc-source requirements.

Most of the above-mentioned problems are collectively addressed by Dagan *et al* [11] and Arun *et al* [20] where the authors have addressed both CMV elimination and dc-bus utilization, apart from requirement of single dc-source. However, the given solutions use higher number of components when compared to number of SVs utilized. Thus, optimization is required with respect to the component count and number of levels achieved in the given topology. To address this issue, Hota *et. al.* have proposed a new MLI topology [8], where the component count is minimized by reducing the number of unused SVs. However, the given system uses more dc-sources and the dc-bus utilization is deteriorated, requiring higher dc-link voltage.

To address the poor dc-link utilization, the switched capacitor (SC) MLIs (SCMLI) may be used which has inherent voltage boosting capability [21] – [25]. A recent SC based 2-level three-phase inverter is capable of reducing the

CMV with capability of boosting input voltage [24]. However, the CMV is not totally eliminated and only 2-level operation is explored. Switched capacitor technique can be also used in generating extra voltage levels along with boosting the input voltage. This feature is explored in another investigation, where a novel SC inverter is proposed with multi-level capabilities [25]. However, the high frequency transition in CMV is not minimized in this solution. From the ongoing discussion it is clear that there is no three-phase inverter solution in the literature which has multilevel operation, optimized switch count, high dc-bus utilization, and a single dc source structure with ZCMV operation. To address this issue, in this paper, a novel T-type switched capacitor based 3-level inverter (TSC3LI) topology is proposed with two major contributions:

1. The reduced dc-bus utilization problem of traditional MLIs when operated with ZCMV SVM is addressed by proposing a novel SC based three-phase three-level inverter supplied with a single dc-source.
2. The proposed topology is constructed optimally, by carefully studying the various sub-circuit configurations relevant to the ZCMV SVs with 3-level performance. Because of this, the number of devices is reduced or optimized in the proposed topology.

As a result the proposed topology enjoys the following merits apart from the complete elimination of CMV:

1. The number of devices is less considering complete CMV elimination and voltage step up operation.
2. The proposed configuration requires only one dc-source.
3. The SC voltages are inherently balanced without requiring any complex voltage balancing strategy.
4. The dc-bus voltage requirement is less compared to the existing 3-level CMV elimination solutions due to the step up operation of the integrated SC circuit.

Thus, the given MLI configuration has most of the benefits. Apart from the proposed configuration, this paper also gives the detail of the strategy to be employed for its development using ZCMV space vectors and their sub-circuit configurations. Further, a simple and unique method for designing SC is also presented. Moreover, the proposed topology is compared with the various existing 3-level inverter solutions with CMV elimination capability to prove its merits. To justify the various claims simulation and experimental results are provided.

II. WORKING PRINCIPLE OF PROPOSED TSC3LI

An SV is typically denoted as $[a \ b \ c]$, where a , b and c are the per unit pole voltages of phases A, B and C respectively in the three-phase MLI shown in Fig. 1(a). Now for the ZCMV SVs, the sum of the three per unit pole voltages ($a+b+c$) is always equal to '0' or a constant value. A typical three phase inverter capable of generating a 3-level output voltage [8], has 19 such ZCMV SVs to eliminate CMV. These 19 SVs can be found by all the permutations of the following sets $\{2,0,-2\}$, $\{2,-1,-1\}$, $\{1,1,-2\}$, $\{1,0,-1\}$, and $\{0,0,0\}$ which are termed as the ZCMV SV sets. As an example the SVs, $[20-2]$, $[2-20]$, etc. can be realized from the permutations of the set $\{2,0,-2\}$. It may be noted that the sum of the elements of any given SV realized using this method is 0. This ensures that the CMV is eliminated and is constant for all the SVs considered. Apart from the zero (constant)

CMV other two major requirements are as follows: (i) the desired topology should have a voltage boosting feature using a single dc source and (ii) inherent capacitor balancing. To accommodate these features 5 sub-circuit conditions are defined for each ZCMV SV set as shown in Figs. 1(b) - (f). The variables p , q , and r correspond to the per-unit pole voltages of the terminals P, Q and R respectively as shown in Figs. 1(b) to (f). The load terminals A, B and C can be connected to terminals P, Q and R by different combinations resulting in different SVs as discussed next.

The sub-circuit configuration of the ZCMV SV set $\{2,0,-2\}$ is shown in Fig. 1(b). Regarding this ZCMV SV set, the series connected capacitors C_1 and C_2 are connected across the dc source with voltage of V_{dc} . Each of the capacitors C_1 and C_2 are charged to $V_{dc}/2$, while the capacitors C_3 and C_4 which are connected in series with them respectively are assumed to be charged to $V_{dc}/2$. This sub-circuit is capable of producing the following SVs: $[20-2]$, $[2-20]$, $[-220]$, $[-202]$, $[0-22]$, and $[02-2]$. Similarly the corresponding SVs for all the ZCMV SV sets can be found out. All the ZCMV SV sets and their corresponding SVs are listed in Table-I along with the associated figure reference number and capacitor charging($\uparrow$)/discharging($\downarrow$) state.

TABLE I. ZCMV SV SETS AND OTHER RELEVANT INFORMATION

ZCMV SV sets	Fig. Ref.	Corresponding SVs	C_3	C_4
$\{2,0,-2\}$	Fig. 1(b)	$[20-2]$, $[2-20]$, $[-220]$, $[-202]$, $[0-22]$, $[02-2]$	$\downarrow$	$\downarrow$
$\{2,-1,-1\}$	Fig. 1(c)	$[2-1-1]$, $[-12-1]$, $[-1-12]$	$\downarrow$	$\uparrow$
$\{1,1,-2\}$	Fig. 1(d)	$[11-2]$, $[1-21]$, $[-211]$	$\uparrow$	$\downarrow$
$\{1,0,-1\}$	Fig. 1(e)	$[-201]$, $[-110]$, $[0-11]$, $[01-1]$, $[1-10]$, $[10-1]$	$\uparrow$	$\uparrow$
$\{0,0,0\}$	Fig. 1(f)	$[000]$	$\uparrow$	$\uparrow$

It may be noted that in all these configuration the dc source is always connected in parallel with the series connected dc-link capacitors C_1 and C_2 , as in case of a 3-level NPC. This helps in balancing the capacitor voltage without using any external charging circuit. The capacitors C_3 and C_4 change their positions as they are charged in parallel with the dc-link capacitors and discharged in series with the input dc source V_{dc} . This technique is typically used in switched capacitor technology and helps in self balancing the capacitor voltage of C_3 and C_4 apart from providing voltage boosting. Another important point is that in case of any sub-circuit, the load-terminals need to be switched in such a way that it is able to generate any desired permutation of the ZCMV SV set. This is only possible by using a 3-level inverter like a T-type inverter or an NPC. Taking a clue from the ongoing discussion, it is obvious that a careful amalgamation of a special switched capacitor circuit and T-type inverter would result into an optimized MLI circuit which can address the issues discussed in the introduction part.

Using the ideas explained above a novel T-type switched capacitor 3-level inverter (TSC3LI) topology is formed as shown in Fig. 2. It can be observed that the proposed TSC3LI consists of a switched capacitor block (SCB) cascaded with a T-type inverter as can be seen from Fig. 2. The SCB comprises of four controlled switches (S_1 , S_1' , S_2 , and S_2') and two diodes (D_1 and D_2). The SCB is capable of boosting the input voltage using the switched capacitor principle. The proposed topology requires only one

dc-source and four capacitors (C_1, C_2, C_3, C_4). The other part of the proposed topology is the T-type inverter. This is made up of 9 switches ($S1A, S2A, S3A, S1B, S2B, S3B, S1C, S2C, S3C$); out of them 3 are bi directional in nature ($S2A, S2B, S2C$). The bidirectional switches can be realized by the anti-series connection of two MOSFETs or IGBTs with anti-parallel diodes. The SCB is connected with the T-type inverter via the three buses (bus 1, bus 2, bus 3) as shown in Fig. 3. The possible voltage levels between bus 1 and bus 2, are $V_{dc}/2$ and V_{dc} . Same holds true for the buses 2 and 3. Hence, between any two subsequent buses two voltage levels $V_{dc}/2$ and V_{dc} can be applied with the help of the SCB represented by four modes in Fig. 3.

Fig. 1. The various sub-circuit configurations corresponding to the ZCMV SV sets: (a) $\{2,0,-2\}$; (b) $\{2,-1,-1\}$; (c) $\{1,1,-2\}$; (d) $\{1,0,-1\}$ and (e) $\{0,0,0\}$.

Four modes of operation and the SV diagram of the proposed topology is shown in Fig. 3. In Fig. 3 only the turned on power semiconductors are made visible for each mode. It can be observed from Fig. 3 that each mode of operation contributes a set of SVs in the SV diagram and they are shown in Fig. 3(e). During Mode-I both of the SCs get charged and the SVs contributed by this mode are denoted with the symbol of a circle. During Mode-II, C_3 gets charged and C_4 gets discharged. The SVs produced during this mode are denoted by a triangle. During Mode-III, C_4 gets charged and C_3 gets discharged and the SVs produced during this mode are denoted using a star. During Mode-IV, both of the SCs are discharged and the SVs produced are denoted using a square symbol.

It may be noted that the function of the SCB is to generate the necessary input condition for the T-type inverter corresponding to any given ZCMV set. The function of the T-type inverter is to generate any ZCMV SV possible with the given ZCMV set. For example, let us consider the SVs $[0\ 2\ -2]$ and $[0\ -2\ 2]$ which belongs to the ZCMV set $\{2,0,-2\}$. The circuit conditions of the SCB and T-type inverter are shown in Fig. 3(f) and Fig. 3(g) for the SVs $[0\ 2\ -2]$ and $[0\ -2\ 2]$ respectively. It can be observed from Figs. 3(f) and (g) that the SCB operation is same. However, the operation of the T-type inverter is different for these two SVs. This is how the proposed inverter generates the various SVs given in Fig. 3(e). It can be observed from Fig. 3(e) that all the ZCMV SVs, take the shape of a 3-level SV hexagon tilted 30 degrees.

The information about the charging and discharging state of the SCs are also given in Fig. 3(e). Both of the SCs get charged and discharged when the TSC3LI operates in the SV

locations with green colour and red colour respectively. The capacitor C_3 charges and C_4 discharges in the blue coloured SV locations and C_4 charges and C_3 discharges in yellow coloured SVs. It can be observed that at each triangle formed by any three closest SVs there is at least one SV where both of the SCs get charged. This ensures reduced voltage ripple in the SCs. Also the PWM strategy itself takes care of the voltage balancing of the capacitors. The PWM scheme is briefly explained in the next subsection.

Fig. 2. The circuit configuration of the proposed TSC3LI.

Fig. 3. Various operating modes of the SCB of the proposed TSC3LI : (a) Mode-I; (b) Mode-II; (c) Mode-III; (d) Mode-IV and (e) the space vector diagram 7only the ZCMV states in relation to the operating modes.

PWM scheme: Standard ZCMV SVM scheme is used to operate the proposed inverter. ZCMV SVM scheme is elaborately presented in [13] - [15]. In this work, traditional SVM technique is used to decompose the reference vector ($\vec{V}_{ref}$) using ZCMV SVs shown in Fig. 3(e). As an example

$\overrightarrow{V_{ref}}$ can be realized using the SVs [10-1], [20-2], and [2-1-1] for the case shown in Fig. 3.

III. CMV ANALYSIS AND SC DESIGN

It is necessary to analyse the CMV and terminal voltage mathematically of the proposed topology. As the proposed configuration is an SC assisted topology, it is also necessary to provide an appropriate SC design method.

A. CMV and terminal voltage analysis:

To analyze the CMV and terminal voltages of the proposed TSC3LI topology, the concept of switching function is used [8]. In this analysis, S_{MN} and S_M (where $M \in (1, 2, 3)$ and $N \in (A, B, C)$) are defined as switching variables which correspond to switches SMN and SM respectively. If the switch SMN is in turn-ON state S_{MN} is equal to '1' and has '0' value during turn-OFF state. Likewise, if the switch SM is turned ON S_M is equal to '1' else S_M is equal to '0'. Using switching variables the three pole voltages for the proposed configuration are given as follows:

$$V_{AO} = S_{1A}(S_1 + 1)(V_{dc}/2) - S_{3A}(S_2 + 1)(V_{dc}/2) \quad (1)$$

$$V_{BO} = S_{1B}(S_1 + 1)(V_{dc}/2) - S_{3B}(S_2 + 1)(V_{dc}/2) \quad (2)$$

$$V_{CO} = S_{1C}(S_1 + 1)(V_{dc}/2) - S_{3C}(S_2 + 1)(V_{dc}/2) \quad (3)$$

Now, common mode voltage or CMV is defined as the voltage across the source neutral point O and load neutral point N and its expression can be obtained by the following expression:

$$V_{NO} = \frac{V_{AO} + V_{BO} + V_{CO}}{3} \\ = \left[\frac{S_{1A} + S_{1B} + S_{1C}}{3} \left(\frac{S_1 + 1}{2} \right) - \frac{S_{3A} + S_{3B} + S_{3C}}{3} \left(\frac{S_2 + 1}{2} \right) \right] V_{dc} \quad (4)$$

Similarly, the source terminal points' (P and Q) voltage differences with O can be obtained as follows:

$$V_{NP} = V_{NO} - V_{dc} \quad (5)$$

$$V_{NQ} = V_{NO} + V_{dc} \quad (6)$$

The switching function analysis presented above is valid for any PWM scheme. However, the proposed TSC3LI is operated using only at the SV locations shown in Fig. 3. This modulation strategy is known as the ZCMV SVM strategy as given in [20]. This results in complete elimination of CMV.

$$\text{Therefore, } V_{NO} = 0 \quad (7)$$

Putting this value of V_{NO} in (5), (6), and (7) the expression for the various other terminal voltages can be derived as follows:

$$V_{NP} = -V_{dc} \quad (8)$$

$$V_{NQ} = V_{dc} \quad (9)$$

Thus, the terminal voltage for the PV array is constant and this further helps in minimizing the leakage current in the proposed MLI.

B. SC design:

In this subsection the SC design procedure is explained. The rated power of the proposed MLI is assumed to be P . Hence,

the current of phase A (i_a) for the UPF operation is given in the following equation:

$$i_a = (P/3V_{dc}) \sin(\omega t) \quad (10)$$

The trajectory of the reference vector from $\omega t = \pi/3$ to $\omega t = 2\pi/3$ resides in a single sector of the SV diagram of the proposed topology which is shown as the shaded portion sector given in Fig. 4. The time instants where $\omega t = \pi/3$ and $\omega t = 2\pi/3$, are indicated in Fig. 4 in the i_a waveform and the SV diagram. Considering the worst case condition and simplicity of the calculation, it is assumed that only the SVs at the boundary of the SV diagram ([20-2], [2-1-1], and [2-20]) are used. In these SV locations, C_3 always gets discharged and the current flowing through C_3 is always i_a as shown in Fig. 4.

Fig. 4. The highlighted sector and sub-circuits describing the assumptions of the SC design procedures.

Hence the energy supplied by the capacitor from $\omega t = \pi/3$ to $\omega t = 2\pi/3$ can be calculated as below:

$$E = \int_{\pi/3\omega}^{2\pi/3\omega} \frac{V_{dc}}{2} i_a dt = \int_{\pi/3\omega}^{2\pi/3\omega} (P/6) \sin(\omega t) dt = \frac{P}{6\omega} \quad (11)$$

The energy supplied by C_3 can also be calculated from the difference of the stored energy in C_3 at instants $\omega t = 2\pi/3$ and $\omega t = \pi/3$ as follows:

$$E = 0.5(CV_1^2 - CV_2^2) \approx 0.5CV_{dc}\Delta V \quad (12)$$

Where, $V_1 - V_2$ are the capacitor voltage at instants $\omega t = 2\pi/3$ and $\omega t = \pi/3$ and $\Delta V = V_1 - V_2$. ΔV is also the voltage ripple of C_3 . By equating (11) and (12) the capacitor value can be calculated as follows:

$$C = \frac{P}{3\omega V_{dc} \Delta V} \quad (13)$$

IV. COMPARISON OF THE PROPOSED TSC3LI WITH EXISTING 3LI TOPOLOGIES WITH CMV ELIMINATION

The proposed topology is also compared with the existing topologies to establish its various advantages over the existing ones. The various parameters or attributes considered for this comparison are given in Table II along with the results of this comparison.

It can be seen from the Table II that the topology proposed by Hota *et. al.* [8] uses minimum number of power semiconductor devices for the elimination of CMV with 3-level performance. Whereas other existing solutions require a higher number of controlled switching power

semiconductors (IGBT) to achieve the same [4], [11], [22]. However, it suffers from two critical drawbacks: The dc-bus requirement and the number of isolated dc-source requirement is still on the higher side compared to the existing solutions. Moreover, the topology proposed in [8] is not inherently capable of capacitor voltage balancing without connecting extra voltage balancing circuits. However, the proposed TSC3LI configuration is capable of addressing all these problems with just an addition of two extra diodes compared to the topology proposed in [8].

It can be observed from Table II, that the number of dc source requirement and dc-bus voltage requirement is minimum in the proposed topology with no capacitor voltage-balancing problem. Apart from this, the number of switches is reasonably lower in count in comparison with most of the existing solutions. It may be noted that if any existing ZCMV 3LI solution needs to be operated with reduced magnitude of dc-source, they need an input side dc-dc boost converter which adds extra losses in the system. The inherent voltage boosting feature of the proposed topology makes it more efficient compared to the existing topologies.

TABLE II. COMPARISON OF THE PROPOSED TSC3LI WITH EXISTING 3LI TOPOLOGIES WITH CMV ELIMINATION

Topology	A	B	C	D	E	F	G
Dagan <i>et.al.</i> [11]	20	12	10	20	1	$3.74V_{dc}$	Not present
CHB used in Nguyen <i>et.al.</i> [4]	24	0	12	24	6	$6V_{dc}$	Requires multiple sources
Kumar <i>et.al.</i> [22]	24	0	12	24	1	$4V_{dc}$	Not present
Hota <i>et.al.</i> [8].	16	0	6	13	4	$4V_{dc}$	Present
Proposed TSC3LI	16	2	8	13	1	$2V_{dc}$	Not present

A: Number of IGBTs; B: Number of diodes; C: Number of capacitors; D: Number of driver circuit requirement; E: Isolated dc-source requirement if no balancing circuit is employed; F: dc bus voltage requirement, G: Capacitor voltage-balancing problem if only one isolated dc source is employed without any balancing circuit;

V. SIMULATION AND EXPERIMENTAL RESULTS OF TSC3LI

The proposed TSC3LI is simulated on PLECS software platform for different values of modulation indices (m_a) using the parameters and system specifications given in Table III. Various simulation results (phase voltages, line voltage, pole voltages, CMV and SPTV (solar PV terminal voltage), phase currents, SC voltages and currents, and leakage current) corresponding to unity modulation index are shown in Fig. 5. It may be observed from Fig. 5 that the phase voltage and pole voltages have identical shape. This is only possible in an inverter where CMV is zero. This is also supported by the CMV waveform which is clamped to zero. This allows the SPTV to be oscillation free and constant as shown in Fig. 5. The sinusoidal nature of the phase currents validates the effectiveness of the PWM scheme. The nature of the SC current is such that it has a finite positive value in every switching period. This proves that the proposed topology can charge the SCs in each switching cycle. This also helps in minimizing the SC voltage ripple which can be

observed to be around 2.5V in Fig. 5. From (13) the SC voltage ripple may be calculated as 2.82V using the parameters given in Table III. This supports the effectiveness of the SC design procedure. Another important observation can be made from Fig. 5 that the leakage current is almost negligible having an rms value as low as 1.5mA. This shows that the proposed topology can be effectively used in transformer-less solar PV applications. The FFT of the phase voltage, phase current, CMV and leakage current are given in Fig. 6. It may be observed that in the case of phase currents, CMV and leakage current the harmonic contents are almost negligible which is very desirable for reducing the EMI.

TABLE III. SIMULATION PARAMETERS

Parameters	values	Parameters	Values
f_m	50 Hz	f_{sw}	5 kHz
R_{PV}	10 Ω	C_{PV}	100 nF
V_{dc}	400 V	Power @ $m_a=1$	5kW
R_L	47 Ω	IGBT model	IKW30N60T IGBT
L_L	10 mH	Diode model	IKW30N60T Diode
		C_1, C_2, C_3, C_4	4.7 mF

f_m : frequency of the modulation signal; f_{sw} : switching frequency; R_L : load resistance; L_L : load inductance; R_{PV} : PV parasitic resistance, C_{PV} : PV parasitic capacitance; m_a : modulation index.

Fig. 5. Various simulation results with respect to unity modulation index ($m_a = 1$).

Fig. 6. Fourier spectra of phase voltage, phase current, CMV and leakage current for unity modulation index.

To prove the effectiveness of the proposed topology it is operated in lower modulation indices (0.75 and 0.25) as well and the corresponding results are shown in Fig. 7. It may be observed from Fig. 7 that the CMV and SPTV maintain the same value as in the case of unity modulation index. This

again results in negligible leakage current as observed from Fig. 7.

Fig. 7. Various simulation results with respect to lower modulation indices.

A detailed loss analysis is carried out in PLECS software using the following power device models: IKW30N60T_IGBT and IKW30N60T_Diode. The loss breakdown for various switches in the proposed topology along with its efficiency are shown in Fig. 8 for $m_a = 1, 0.75$ and 0.25 . It may be observed that the proposed topology exhibits 98.34% efficiency at 5kW output power which is considerably high. At lower modulation index operation (0.25) the efficiency is still quite high (96.92%) considering the output power is as low as 314W.

Fig. 8. Loss breakdown in the proposed topology and its efficiency for various modulation indices (m_a). ϕA , ϕB , and ϕC denotes the assembly of switches belong to phase A, B and C legs respectively.

The blocking voltages of the various switches from the SC block and the T-type inverter are shown in Fig. 8. It may be observed that the switches of the SC block has lower blocking voltage from the T-type inverter. This implies that the switches with higher blocking voltage has lower effective switching frequency and vice versa.

Fig. 9. Loss breakdown in the proposed topology and its efficiency for various modulation indices (m_a). ϕA , ϕB , and ϕC denotes the assembly of switches belong to phase A, B and C legs respectively.

Along with the simulation validation, a laboratory prototype has been fabricated for the proposed TSC3LI configuration using the MOSFET IRF840 and driver IC HCPL-A3120. A programmable DC source, manufactured by TDK Lambda is used for input DC power supply to the inverter. The ZCMV SVM based PWM scheme is programmed in Digilent Atlys Spartan 6 FPGA. The various parameters of the laboratory prototype of the proposed inverter are shown in Table IV.

TABLE IV. PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Parameters	values	Parameters	values
f_m	50 Hz	L	4 mH
f_{sw}	5 kHz	SC (C_1, C_2, C_3, C_4)	1 mF
V_{DC}	50 V	PV parasitic capacitance	100 nF
R_L	350 Ω	PV parasitic resistance	10 Ω

The line voltage, CMV and phase currents are shown in Fig. 9. It may be observed that the CMV is constant which is the key merit of the proposed converter.

Fig. 10. Experimental results showing (a) the line to line and common mode voltage; and (b) phase currents for $m_a = 1$.

The phase voltage, phase current, terminal voltage and leakage current are recorded and shown in Fig. 10 for $m_a = 1, 0.75$, and 0.25 . It may be observed that for every case the terminal voltage is constant and leakage current is negligible. This allows the proposed TSC3LI to be used in transformer-less solar PV applications. All the experimentally obtained waveforms match with their simulation-obtained counterpart.

Fig. 11. Experimental results showing (a) the phase voltage and phase current; and (b) the solar PV terminal voltage (SPTV) and leakage current (i_{leak}) for (i) $m_a = 1$, (ii) $m_a = 0.75$, (iii) $m_a = 0.25$.

The blocking voltages of the various power switches are shown in Fig. 11. It may be observed that various waveform of the blocking voltages are in close match with the

simulation results shown in Fig. 8. The SC voltages and currents are also presented in Fig. 11.

Fig. 12. Experimental results showing (a) v_{S1} , $v_{S1'}$; (b) v_{S1A} , v_{S2A} , v_{S3A} ; (c) v_{C3} , v_{C4} , i_{C3} , i_{C4} . (v_{S1} , $v_{S1'}$, v_{S1A} , v_{S2A} , and v_{S3A} are the blocking voltages of switches S1, S1', S1A, S2A, S3A)

VI. CONCLUSIONS

This paper presents and validates a novel 3-phase T-type switched capacitor based 3-level inverter (TSC3LI). The given simulation and experimental results confirms that the proposed TSC3LI is capable of eliminating the CMV with voltage boosting capability, reduced number of power semiconductor switches and a single dc-source. A major advantage of the proposed topology is that it does not require any external voltage balancing circuit as it balances the input capacitor voltages with switched capacitor principle. Employed ZCMV SVM strategy completely eliminates the high frequency oscillations from CMV and source terminal voltages. A unique advantage of the proposed TSC3LI is that the reduced dc-bus utilization issue of the ZCMV SVM scheme is compensated with its inherent voltage boosting capability. A detailed comparison with the existing 3-level inverter solutions with CMV elimination feature is also done. A unique advantage of the proposed topology is that there is charging state availability for the switched capacitors at every switching cycle.

This manuscript also gives the fundamental details with respect to the derivation of the proposed topology. The proposed topology is derived by carefully studying all the sub-circuits related to the various ZCMV SV locations pertaining to a 3-level inverter. Elimination of CMV makes the proposed topology very suitable for motor drive applications. It is also shown that the ground leakage current is significantly minimized making the proposed converter a worthy candidate for a transformer-less PV-grid interface. Various claims are validated using simulation and experimental studies.

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