An Intelligent Electronic Fuse (iFuse) to Enable Short-Circuit Fault-Tolerant Operation of Power Electronic Converters

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Abstract— The present paper proposes a novel device defined as an intelligent electronic fuse (iFuse) meant to be connected in series with any current-bidirectional voltage-unidirectional active switch present in a given converter. The iFuse duty is to isolate its series-associated switch from the rest of the converter circuit immediately after detecting that said switch has failed in short circuit. Nonetheless, it maintains the reverse (free-wheeling) current path originally offered by the failed switch. The failure detection is performed when the failed switch causes a shoot-through event. Therefore, the iFuse is designed to be able to block the elevated current occurring in such event. The iFuse allows increasing the fault-tolerant capability and the reliability of power converters where such qualities are hindered by switch short-circuit failures, as in converters featuring parallelized switches, neutral-point-clamped multilevel topologies, or redundant legs. The feasibility of the iFuse device is verified through experimental tests, proving that the device is able to detect the failure of its associated switch and isolate it from the rest of the converter circuit in 6 μ s, while stopping short-circuit currents of up to 1 kA without incurring in harmful di/dt values.

Index Terms— Electronic fuse, fault diagnosis, fault tolerance, power converters, redundancy, switch short-circuit fault.

I. INTRODUCTION

AT present day, power electronics is an essential subsystem in an extensive range of applications and power ratings [1]. Some of these applications are categorized as critical, that is, the continuity of the service must be assured at all time, mainly because of safety or economic reasons [2], not allowing an unexpected system shutdown, although a

degraded operation can be eventually accepted [3]. Therefore, fault-tolerant operation of the system, and specifically of the power electronics converter, is required [3]. For example, in electric vehicles, a motor drive failure may risk the passenger safety [2]–[4], and a limp-home mode is desirable.

It is estimated that at least 80% of faults in power converters are due to power switch failures [5], which can be classified basically in switch open-circuit failures (OCFs); i.e., the power switch remains in a permanent OFF state, and switch short-circuit failures (SCFs); i.e., the power switch remains in a permanent low-ohmic ON state [6].

Three steps must be sequentially applied to achieve fault-tolerant power converter operation when a fault occurs: fault diagnosis, fault isolation, and system reconfiguration [2], [3], [7].

The ease in achieving fault tolerance depends on the type of switch fault. In a voltage-source converter topology, a switch OCF provides inherent fault isolation. On the other hand, a switch SCF implies the short-circuit of a voltage source; i.e., a shoot-through event, when the switch complementary to the failed switch is turned on. This imposes the risk of damaging the healthy devices located in the path of the short-circuit current, causing a sequence of faults. This can occur even if the healthy-switch drivers include over-current detection with proper switch-off capability [8], since this protection might not be fast enough to avoid damage or because the shoot-through event may repeat in time. Hence, if the short-circuit failed device is not properly identified and isolated, the converter health and performance could rapidly deteriorate.

Fault diagnosis can be performed at component level or system level [7]. At component level, for each power semiconductor, the proper switch variables (current, voltage, etc.) are monitored to rapidly detect switch malfunction and the type of failure [6], [9]. At system level, the fault is identified by analyzing the power converter waveforms or by algorithmic methods [9], although these techniques present increasing complexity to avoid incorrect fault diagnosis and may require several ms to perform the diagnosis [6], [10].

Fault isolation and system reconfiguration are carried out in different ways depending on the converter redundancy, which can be classified as system-level, leg-level, module-level, and switch-level redundancy [2]. These redundancy levels can be inherent to the converter topology or can be achieved through

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the inclusion of additional hardware in the converter.

System-level redundancy typically consists on replicating the converter topology and connecting them in cascade or in parallel [2], increasing the system reliability only to a small degree.

Leg-level redundancy typically consists on isolating the faulty branch and reconfiguring the converter by connecting the faulty-branch output terminal to a redundant leg [2], [10] or to the dc-link midpoint [9], [11]. These solutions are simple but rely on thyristors, which may not be sufficiently fast to reconfigure the converter topology to avoid further damage of the system after a switch SCF.

Module-level redundancy is inherent to cascaded H-bridge and modular multilevel converter topologies. In these cases, faulty modules are easily bypassed with thyristors or relays, and operation is continued by either enabling redundant modules or by reconfiguring the switching strategy [2], [7], taking advantage of the inherent switching-state redundancy of these multilevel converters. Faulty modules due to switch SCF may require some sort of isolation procedure before its bypass.

Neutral-point-clamped (NPC) and flying-capacitor (FC) multilevel topologies feature inherent switch-level redundancy. The solutions proposed in the literature usually do not require additional hardware and basically consist on the modification of the switching strategy [2], [7], [12]–[14]. Nevertheless, after a fault occurs, the converter will operate with reduced performance, which depends on the number, type, and location of the faults. In terms of fault tolerance, NPC topologies are more vulnerable to switch SCFs than to switch OCFs. Moreover, when one or two switches fail in short circuit, the resulting switching states feature on average less available connections to the dc-link voltage levels than in the switch OCF case [14]. In FC topologies, as opposed to NPC topologies, switch OCFs are more critical than switch SCFs because these topologies feature series-switch redundancy. In any case, a switch OCF in a FC topology without additional hardware redundancy forces to stop operation [7], [13]. Nonetheless, switch SCFs lead to the short circuit of the converter capacitors, thus requiring a mechanism to avoid it.

It is then fair to conclude that, except for system-level redundancy and the switch-level redundancy offered by FC topologies, switch SCFs are more critical than switch OCFs in the described converter redundancy levels. Therefore, in voltage-source converters it would be desirable to have a mechanism to force that all switch failures end up being equivalent to a switch OCF, thus avoiding the short circuiting of voltage source elements. This is accomplished in literature by introducing additional hardware in order to isolate the switch in SCF from the rest of the circuit. For instance, [11] employs a fast fuse in series with each active switch on a three-level three-phase dc-ac converter, such that when a shoot-through event occurs due to a switch SCF, the fuses are blown. However, there is no guarantee that the fuse in series with the short-circuited switch will blow, since the fuse of the complementary switch could blow first. A more advanced solution is proposed in [15] for the same topology, where

again a fast fuse is placed in series with each active switch but these are selectively fused with a robust active switch (thyristor) and the energy stored in the dc link. In contrast, [16] presents a two-level three-phase dc-ac converter employing two switches in series per position (one of them in permanent ON state) and two legs per phase (one of them in stand-by), therefore featuring leg-level and series-switch-level redundancy. When a switch SCF or OCF occurs on the active leg, all switches in this leg are turned off and the redundant leg is enabled and operated with the same switching strategy as the faulty leg previous to the fault. Other solutions consist on isolating the connections of the active switches to the dc-link capacitors in NPC topologies or the flying capacitors in FC topologies through fast fuses deliberately fused with thyristors [17] or through current-bidirectional voltage-unidirectional (CBVU) and four-quadrant (4Q) active switches [14], [18].

The presented solutions mitigate the consequences of switch SCFs, but present some drawbacks. For instance, fuses are bulky [19] and its typical melting profile requires a short-circuit current much higher than the nominal current to have reduced melting times [19], which could lead to any healthy devices in the short-circuit current path to fail. Also, the fuse resistance and stray inductance increase the conduction losses and voltage spikes during switching transitions in normal operation [2]. On the other hand, replacing fuses with switches allows performing the isolation action in less time and yields less conduction losses during normal operation [16]. Nonetheless, all the solutions employing switches to isolate a switch in SCF [14], [17], [18] rely on a centralized control that first has to detect the failure and then commands the turn off of the corresponding redundant switch.

A natural solution to isolate a switch in SCF employing semiconductor active switches without relying on a centralized control, are solid-state circuit breakers [20] and electronic fuses [21]. Nonetheless, these devices actuate whenever any overcurrent is detected and they are not able to selectively isolate only those switches that have failed in short circuit.

The present work proposes a new device defined as an intelligent electronic fuse (iFuse), envisioned to provide switch-level redundancy to any type of converter employing CBVU active switches and conceived to be connected in series with said active switches. The iFuse performs an automatic diagnosis at component level of its associated active switch in order to assert its SCF. This diagnosis is performed during the shoot-through event caused by the failed switch. In case the diagnosis is positive, the iFuse proceeds to block the forward current path of its associated switch, stopping the short-circuit current and preventing future shoot-through events, but maintains the free-wheeling path that was offered by the active switch previous to the fault. The iFuse allows the fault-tolerant operation of the power converters under switch SCFs, improving significantly the reliability of the converter itself and the system where it is employed.

The manuscript is organized as follows. Section II describes the functional blocks constituting the iFuse and its working principle. Section III describes which kind of power converters would be most benefited in terms of fault-tolerance

by incorporating iFuses. Section IV presents experimental results to demonstrate the feasibility of the proposed iFuse device. Finally, section V outlines the conclusions.

II. IFUSE CONFIGURATION AND OPERATING PRINCIPLE

Fig. 1 presents a diagram of the series connection of an iFuse with a CBVU active switch (S_m). This series connection can be regarded as a new compound device featuring power terminals pt1 and pt2, input binary signal S for the control of S_m , and output binary signal st to report the health status of S_m . The iFuse is composed of a normally-ON active switch (S_{iF}) together with its driving circuitry, the circuitry to quickly diagnose S_m faults, and the iFuse power supply. S_{iF} is a CBVU switch. This allows maintaining the freewheeling path after S_m SCF, which in pre-fault condition is offered by S_m antiparallel diode. The diode shown in the iFuse symbol of Fig. 1(a) denotes the availability of the abovementioned free-wheeling path.

The self-power-supply circuit conceived in [22] can be used to power the isolated gate driver of S_m (GDPS) and the iFuse circuitry (iFPS) by recycling S_m turn-off switching losses. Isolated drivers are required to transfer digital signals across the isolation barrier between the converter control and the converter power circuit.

Fig. 2 and Fig. 3 show in full detail the circuit of the four main functional blocks making up the proposed iFuse. An n-channel metal-oxide-semiconductor field-effect transistor (MOSFET) is here selected to implement S_{iF} switch. The S_m -fault automatic-detection circuitry is composed of the forward-current detection circuit (FCDC) and the fault detection logic (FDL). Fig. 3 shows the circuit of the iFPS, following the design of [22] but modified to deliver two voltage supplies

(V_{fuse} and V_{cc}), one of them stabilized with linear voltage regulator U_5 . Fig. 4 shows the evolution of the main iFuse analog and digital signals described in this section.

The compound device shown in Fig. 1(a) will be integrated in a power converter. A SCF of S_m , will be typically followed by a switching state where S_m control signal is low ($S = 0$) and a positive current i_s flows through S_m , with reference to Fig. 1(b). The proposed iFuse solution will stand-alone detect this situation to diagnose the SCF of S_m , to then immediately isolate it from the rest of the circuit by blocking its forward current path.

In normal operation, S_{iF} is kept permanently ON thanks to voltage V_{fuse} feeding S_{iF} 's gate through fuse F_{latch} (see Fig. 2). During this condition and since MOSFET S_{iF} acts as shunt when ON, the FCDC senses the current i_s by amplifying the voltage across S_{iF} with the circuit formed by OP operational amplifier and resistors R_f - R_g . The sensed current is then compared through comparator COMP and resistors R_{IS1} - R_{IS2} to the threshold value $I_{S,th}$, in order to determine if a positive current is flowing through S_m . This is indicated by Boolean variable IS , such that

$$\begin{aligned} IS &= 0 \text{ when } i_s < I_{S,th} \\ IS &= 1 \text{ when } i_s \geq I_{S,th}. \end{aligned} \quad (1)$$

It seems straightforward that then the FDL just needs to look for a concurrent $S = 0$ and $IS = 1$ to determine the SCF of S_m . However, it must be taken into account that the described conditions can also be met during S_m turn-off transition in normal operation. Therefore, to avoid a false S_m -failure detection, the fault detection must be disabled during this time interval. To do so, a disable signal

Fig. 1. Diagram of the compound device constituted by switch S_m and the proposed iFuse. (a) Compact representation of the compound device, showing the iFuse symbol. (b) Expanded view of the iFuse device, showing its internal functional blocks. Relevant digital signals appear in red.

Fig. 2. Schematic of the fault detection logic, the driving, latching, and status-reporting circuit, and the forward-current detection circuit. Relevant digital signals appear in red.

$$D = \bar{S} \cdot S_{dly} \quad (2)$$

is defined, where S_{dly} is a replica of S delayed T_{dis} seconds and generated with R_{dly} and C_{dly} RC network.

Finally, the switch fault detection signal

$$SFD = \bar{D} \cdot \bar{S} \cdot IS \quad (3)$$

is generated, where $SFD = 1$ indicates the detection of S_m SCF. When signal SFD transitions from 0 to 1, it latches signal $\bar{O_iF}$ to zero with the D bistable U_3 . Therefore, when a fault is detected $\bar{O_iF} = 0$ permanently, causing MOSFET S_{off} to turn on, which performs two actions: turning S_{iF} off by discharging its gate and fusing F_{latch} . Moreover, pull-up resistance R_{pu1} ensures that, in case of failure of the FDL block, the iFuse is engaged, turning S_{iF} off. The D bistable is reset to $\bar{O_iF} = 1$ during the iFuse device power up with R_{rst} and C_{rst} RC network.

Since S_m SCF may result in a short-circuit current flowing through the failed switch as well as other switches, the failure detection procedure must occur before the triggering of the gate-driver overcurrent protection of the healthy switches in the short-circuit current path, such that the short-circuit current is sustained the necessary time for O_iF to engage.

Moreover, the short-circuit current scenario also imposes that S_{iF} turn off must be performed taking into account two considerations. First, S_{iF} turn off must be quick enough to avoid damage of S_{iF} and other healthy switches located in the short-circuit current path. The maximum energy absorption capability of MOSFET and IGBT chips is around 4 to 5 J per

cm² of die surface, resulting in a maximum permissible short-circuit event duration around 10 μ s [6], [23]. However, on a second consideration, S_{iF} turn off must be slow enough to avoid high dis/dt values that could cause voltage spikes in the parasitic inductances present in the short-circuit current path, damaging S_{iF} and other healthy devices due to overvoltage. For this reason, the turn off of S_{iF} is performed in two stages. In the first stage, S_{iF} gate is discharged until its gate-to-source voltage $v_{GS,SiF}$ reaches the threshold value $V_{GS,th}$. In this interval, S_{iF} remains ON since $v_{GS,SiF} > V_{GS,th}$ and S_{iF} 's gate discharge is performed quickly to account for the first consideration. In the second stage, $v_{GS,SiF}$ is discharged from $V_{GS,th}$ to zero volts. This is the interval where the true turn off takes place. To account for the second consideration, the gate discharge is performed slower than in the first stage. The abovementioned discharge process is accomplished through

Fig. 3. Schematic of the iFPS circuit.

Fig. 4. Typical evolution of the main analog and digital signals from the iFuse circuitry during a shoot-through event due to a SCF of the switch associated to the iFuse, as in the circuit shown in Fig. 6(a).

the network composed of $R_{\text{off-slow}}$, $R_{\text{off-fast}}$, and zener diode Z_1 , with $R_{\text{off-slow}} \gg R_{\text{off-fast}}$ and zener voltage $V_Z \approx V_{\text{GS,th}}$. This way, S_{IF} gate is initially discharged fast thanks to the low-impedance path offered by the series connection of $R_{\text{off-fast}}$ and Z_1 until $v_{\text{GS},S_{\text{IF}}} \approx V_Z$, when Z_1 turns off. Afterwards, S_{IF} 's gate is discharged slowly through $R_{\text{off-slow}}$, to ensure a low- di/dt turn-off transition.

The purpose of F_{latch} is to serve as a one-time latch. When S_{off} is turned on, V_{fuse} voltage supply is short-circuited through S_{off} and F_{latch} , effectively fusing F_{latch} . Once F_{latch} is fused, S_{IF} is permanently maintained OFF with pull-down resistor R_{pd1} , thus permanently blocking any forward current through S_{m} . F_{latch} current rating can be quite small since the fuse does not have a current limiting function, which allows a low capacitance value for C_{fuse} in Fig. 3.

The steady-state drain-to-source voltage of S_{off} ($V_{\text{DS},S_{\text{off}}}$) reflects the state of F_{latch} and hence, the health status of S_{m} . For convenience, output health-status reporting binary variable st is defined from this voltage. The value of this variable is $st = 1$ when $V_{\text{DS},S_{\text{off}}} = V_{\text{fuse}}$ (F_{latch} is unfused and S_{m} is in healthy condition) and it is $st = 0$ when $V_{\text{DS},S_{\text{off}}} = 0$ V (F_{latch} is fused and S_{m} has failed). Variable st can be fed back to the power converter control such that the converter structure and/or switching strategy can be reconfigured after the failure, if necessary.

Referring to Fig. 4, the detection time T_{det} is the time the automatic-diagnosis circuit takes to identify S_{m} SCF, and the actuation time T_{act} is the time it takes for the driving circuit to turn off S_{IF} .

The main requirements of S_{IF} CBVU switch are:

- On-state voltage drop should be as small as possible in order to minimize the increment of converter conduction losses incurred when adding the iFuse.
- It should be able to withstand short-circuit currents for a few μs .
- It should be able to perform fast turn-off transitions.
- Drain-to-source breakdown voltage should match the associated switch S_{m} breakdown voltage.

MOSFETs and IGBTs are good candidates. MOSFETs excel in turn-off speed, while IGBTs feature low conduction losses at device voltage ratings ≥ 600 V and current ratings ≥ 50 A. SiC and GaN MOSFETs present superior switching speeds and lower conduction losses. However, recent studies have reported a low capability of these devices to withstand short-circuit currents [24].

A low conduction voltage drop generally implies high switching losses. However, S_{IF} switching losses can be neglected, since it will only turn on at zero current during the converter power up and it will turn off only once, when the fault of its associated switch is detected. Moreover, low-conduction-loss devices are also more robust in front of short-circuit currents since they feature a higher current rating than low-switching-loss devices for the same voltage rating and semiconductor technology.

III. APPLICATIONS

The proposed iFuse device is meant to be employed in power converters where the forward current of the short-circuit-failed switches must be blocked in order to impede the short circuit of any converter voltage source. When these converters feature some sort of redundancy, such action allows continuing the operation with possible reduced performance.

In the following, some cases where these conditions are met are presented.

- A first case are power converters employing parallelized switches in order to reduce conduction losses, as in the Tesla Model S two-level three-phase inverter, which features six parallelized discrete IGBTs per switch position [25]. In these converters, a SCF of one of the switches disables the whole parallelized group and operation must stop. Employing an iFuse in series with each switch, or at least with those less reliable switches, enables the fault-tolerant operation of the converter and takes full advantage of the converter inherent switch-level redundancy. This is illustrated in Fig. 5(a) which presents an example of a two-level leg with two parallelized switches per position and with switch S_{2a} failed in short circuit. When the leg output terminal is connected to dc-link node 2 and $i_o < 0$, current will partially flow through the S_{2a} iFuse free-wheeling diode.
- A second case are active NPC topologies. As explained in Section I, these topologies offer inherent switch-level redundancy, but are more vulnerable to switch SCF than to switch OCF, since the former renders less available switching states than the latter. As a first example, Fig. 5(b)-(c) shows a three-level active NPC converter leg [14] where two switches have failed in short circuit: S_{p12} and S_{n22} . The switching states defined in [14] ensure that in fail-free operation, the blocking voltage of all off-state switches equals the elementary voltage across adjacent input terminals. This is accomplished by turning on certain switches that are not in the output current path (ON devices over the wide black lines in Fig. 5(b)-(c)). In Fig. 5(b), without the iFuses, a short circuit of the dc-link capacitors occurs when the leg is connected to dc-link nodes 1 and 3. Therefore, the leg is inoperable since only connection to one of the dc-link nodes remains. In Fig. 5(c), with the iFuses, the short circuit of the dc-link capacitors is avoided, and the connection of the output terminal to the three dc-link points is preserved, without the need to modify the switching states. As a second example, Fig. 5(d) shows a T-type three-level active NPC converter leg with one of the switches failed in short circuit: switch S_{2b} , which is part of the middle four-quadrant switch. Without iFuses, connection to node 1 is lost due to the short circuit of the lower dc-link capacitor and the converter power rating is reduced to a half of the pre-fault value. Thanks to the iFuse in series with the failed switch, the converter is still able to operate, preserving the connection to nodes 1 and 3 and

Fig. 5. Examples of converter legs where the iFuse device can be employed to take advantage of switch-level redundancy. Switches failed in short circuit and the short circuit paths are marked in red. The iFuses that have been engaged (off state) are marked in blue. Current paths for $i_o \geq 0$ are marked in green solid lines. Current paths for $i_o < 0$ are marked in green dashed lines. (a) Two-level leg with two parallelized switches per position. (b) Three-level active NPC leg without iFuses. (c) Three-level active NPC leg with iFuses. (d) T-type three-level active NPC leg.

maintaining the converter power rating after the fault. Moreover, the connection to node 2 is still possible but only with $i_o < 0$. The present example also demonstrates that the proposed iFuse can be employed in other converters featuring 4Q active switches; e.g., matrix converters.

- A third case are multi-phase dc-ac converters featuring leg-level redundancy [2], [3], [7]. Conventional solutions employ fast fuses to isolate short-circuit-failed switches. As explained in Section I, employing fast fuses presents many weaknesses. The proposed iFuse can replace these fast fuses, improving

substantially the performance of the fault-tolerance mechanism.

- A fourth case are interleaved dc-dc converters, as for example two-level multiple-phase boost converters [3], [26]. In such converters, a SCF of an active switch leads to the saturation of the inductor and eventually the short circuit of the input power supply. Employing an iFuse in series with each switch avoids this situation and allows reporting the failure to the converter closed-loop control, through signal st , such that proper action can be taken to continue operation with the remaining phases.

Fig. 6. Experimental test schematics. (a) Reproduced scenario. (b) Simplified circuit configuration used for the experimental tests.

IV. EXPERIMENTAL RESULTS

Experimental tests have been carried out to demonstrate the feasibility and effectiveness of the proposed solution. A SCF is forced in the bottom switch S_1 of the two-level converter leg shown in Fig. 6(a). A shoot-through event will subsequently occur when the leg output transitions from the connection to the negative dc-link rail to the connection to the positive dc-link rail; i.e., when S_1 transitions from high to low and then S_2 transitions from low to high. At S_2 turn on, the dc-link capacitor will be short circuited and then iFuse iF_1 should turn off after a short time interval.

This scenario has been reproduced with the simplified circuit configuration of Fig. 6(b). In this circuit, both S_1 and iF_2 have been replaced by a short, since they behave as a low-ohmic contact. Signal S in iF_1 is set low. Signal D will then

TABLE I
EXPERIMENTAL TEST PARAMETER VALUES

Parameter	Value
$V_{S,init}$	50 V
C	440 μ F (electrolytic cap.) + 13.2 μ F (PET film cap.)
R_{sense}	2.5 m Ω $\pm$ 1%
$R_{off-fast}$	10 Ω
$R_{off-slow}$	330 Ω
V_Z	5.1 V
V_{fuse}	15 V
$I_{S,th}$	200 A
$R_{DS,on} (S_2)$	11.1 m Ω
$R_{DS,on} (S_{iF})$	1.3 m Ω

always be zero since signal S does not change. In the experiment, the dc-link capacitors, formed by a parallel connection of electrolytic and PET film capacitors, are first pre-charged to voltage $V_{S,init}$. Then, shortly after, S_2 is turned on. Resistor R_{sense} is employed to measure current i_s .

Switches S_2 and S_{iF} are implemented with MOSFETs IRFR4510 and IPT015N10N5, respectively, both rated at 100 V. Table I shows the main component parameter values of Fig. 6(b). As it can be seen, IPT015N10N5 $R_{DS,on}$ is very low. In fact, it was the commercial 100 V-rated Si MOSFET with the lowest on-state channel resistance at the time of the experimental tests. With the abovementioned S_2 and S_{iF} MOSFET selection, a power converter incorporating an iFuse in series with each switch, would only experience a 12% increase in their conduction losses.

Fig. 7 shows the results of the described experimental test. As it can be observed, once S_2 gate-to-source voltage $v_{GS,S2}$ begins to rise, shoot-through current i_s rises abruptly, reaching a peak value of 1.1 kA. After 1.7 μ s, digital signal IS goes high indicating that current $i_s > I_{S,th}$ (a certain delay is introduced by the detection circuit), followed by the activation of SFD and OiF signals. Once $\overline{OiF} = 0$, the S_{iF} turn-off procedure begins by discharging its gate in two stages, as can

be observed in $v_{GS,SiF}$ and as explained in Section II. S_{iF} true turn off starts when $v_{GS,SiF}$ reaches $V_{GS,th}$ (around 4 V) with its drain-to-source voltage ($v_{DS,SiF}$) and current (i_s) presenting slopes of approximately 30 V/ μ s and -340 A/ μ s, respectively. Thanks to the moderate di/dt value, the peak value of $v_{DS,SiF}$ during the turn off process is limited to 57 V, corresponding to an overshoot of only 14%.

The time intervals for T_{det} and T_{act} are 2.4 μ s and 3.6 μ s, respectively. Therefore, the iFuse is capable of detecting the switch in SCF and blocking the forward current path of its associated switch in 6 μ s. Time interval T_{det} is shorter than the typical response time of the overcurrent protection of the healthy-switches gate driver, which typically is between 8 to 10 μ s. Therefore, the iFuse is able to engage successfully without the negative interference of said overcurrent protection.

During the shoot-through, S_2 drain-to-source voltage $v_{DS,S2}$ reaches an average value of approximately 25 V, indicating that the device is working in the saturation region. During this interval, S_2 junction temperature increases rapidly due to the high power loss, which in turn decreases the saturation current. This phenomenon is consistent with the findings in [23] and explains why i_s current starts decreasing before S_{iF} starts turning off.

The capacitor voltage (V_S) decreases 8 V after the shoot-through event, indicating that approximately 15 mJ have been dissipated in R_{sense} , S_2 , S_{iF} , and the parasitic elements of the circuit. This energy value is far below the maximum short-circuit energy that S_2 and S_{iF} can withstand, which is around 750 mJ and 2.5 J, respectively, considering a die surface of approximately 0.15 cm² for IRFR4510 and 0.5 cm² for IPT015N10N5.

V. CONCLUSION

A novel device has been proposed to improve the fault tolerance and reliability of power converters where switch SCF are especially detrimental. This novel device, designated

Fig. 7. Experimental results showing digital (top) and analog (channels 1 to 4 and R1) signals.

as iFuse, operates by very quickly transforming an original switch SCF into a switch OCF while at the same time enabling a free-wheeling current path on the failed device. For a converter to present such improved fault tolerance and reliability, an iFuse must be connected in series with each CBVU switch, or at least with those more critical in terms of fault tolerance. Its operating principle is similar to conventional electronic fuses, but it allows selective turn off of only those iFuses whose associated switch has failed in short circuit, all performed in a standalone fashion. Moreover, the iFuse can properly handle the turn off of high short-circuit currents flowing through it, the failed switch, and other healthy devices in the current path. Special care has been taken in the design of the iFuse turn-off procedure so that it is fast enough to avoid the damage of healthy devices due to sustained overcurrent, and so that it does not incur in elevated di/dt that could damage healthy devices due to overvoltage. A signal reporting the health-status of the associated switch has been added. Moreover, the power required for the iFuse operation is provided by recycling the turn-off losses of the associated converter switch. Therefore, there is no need for an additional power supply, allowing its application in all types of converters and simplifying to a great extent the integration of the iFuse into a compact assembly. The health-status reporting functionality can be easily complemented with the OCF detection, by simply monitoring the associated switch voltage across the power terminals.

The iFuse enables the highest improvements in fault tolerance in converters with parallelized power devices, employing NPC multilevel topologies, with redundant legs and/or with multiple phases. If incorporated in multiple power switches, the converter will be able to withstand multiple switch faults.

Experimental results demonstrate that the designed circuit allows a fast detection and isolation of a short-circuit-failed switch, while properly stopping currents up to 1 kA without damaging healthy devices.

VI. REFERENCES

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