Analytical Expressions for Voltage Controller Coefficients to Attain Desired Values of Total Harmonic Distortion and DC Link Voltage Undershoot in Power Factor Correction Rectifiers

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ABSTRACT

The paper reveals analytical expressions linking the coefficients of PI controller, typically employed as voltage loop compensator of power factor correction rectifiers (PFCR), with two major performance merits (namely, total harmonic distortion (THD) of grid-side current and DC-link voltage deviation upon sudden load increase) and DC link capacitance – to – rated power ratio. The proposed methodology allows to concretize the commonly used "8 – 10Hz crossover frequency, 45° – 70° phase margin" rule-of-thumb, typically utilized in application notes of commercial PFC controllers. Relations between voltage loop gain crossover frequency and phase margin as well as settling time of DC-link voltage response to a step load increase to the above mentioned performance merits are also derived in the paper. Provided design guidelines allow to precisely achieve desired values of the two mentioned performance merits and indicate the feasible range of possible DC link capacitance values. Proposed quantitative design guidelines are well-supported by experiments.

INDEX TERMS— Power factor correction, THD, Transient response, Control design.

I. INTRODUCTION

Strict power quality requirements of modern grid codes force mains-interfacing converters to interchange current of predetermined shape with the utility [1], [2]. In case energy is drawn from the grid, power factor correction rectifiers (PFCR) (typically possessing boost topology [3]) are typically employed as grid-interfacing AC/DC converters [4]. As a result of unity power factor operation, instantaneous grid power contains both DC and double-grid-frequency pulsating components. On the other hand, the power drawn by the load fed by grid-connected power conversion system may be either pulsating component free or contain one with different characteristics than that of the grid. Consequently, short-time energy storage element is typically required in order to cope with the sum of grid and load pulsating power components since DC power constituents sum up to zero in steady state to preserve energy balance [5]. Bulk (typically electrolytic) capacitors, connected across the DC link of the power conversion system are typically utilized for this purpose [6]. Pulsating power components, absorbed by the short-time energy storage element, generate DC link voltage ripple proportional to system power rating and inversely correlated to the DC link capacitance value [7] (with the exception of balanced three-phase system, where DC link-side pulsating power component is zero [8], [9]). Moreover, DC link voltage deviation from its nominal value caused by load variations is also inversely related to the DC link capacitance value. On the other hand, DC link voltage should remain bounded both in steady state and during transients to comply with power conversion system functionality and voltage rating of the DC link capacitor. This is why electrolytic capacitors are utilized in DC links of systems rated above several tens of watts. It should be emphasized that due to well-known weight, volume and reliability problems associated with electrolytic capacitors [10] – [12], electronic capacitors, capable of mimicking the operation of large capacitors while utilizing much smaller ones were recently suggested [13] – [15]. Nevertheless, even though an electronic capacitor is utilized, grid-side power quality and DC link voltage restrictions must be respected by the system.

The trade-off between grid-side power quality (in terms of current THD) and DC link voltage deviation (typically in terms of undershoot) clearly pointed out in [16], forces PFCR DC link voltage control loop bandwidth to be restricted in order to keep the near unity grid-side power factor. It should be noted that most of existing practical designs begin with setting the PFCR DC link voltage control loop crossover frequency to a typical value of 8-10Hz and selecting 45-70 degrees phase margin. However, these values are rather rules-of-thumb than clear design guidelines. Recently, the authors of [17] made an attempt to link grid-side current THD and DC link voltage overshoot with DC link voltage control loop compensator (typically PI or type-II) coefficients. However, the methodology was applied to grid-connected photovoltaic inverters, which unlikely to be exposed to step-like variation of DC-side power (as shown in [18], ramp-like power transients are more realistic to be assumed in such applications). Moreover, graphical solution was proposed in [17] and hence region of feasible solutions was not revealed.

It is interesting to note that while a variety of solutions aiming to weaken the above-mentioned trade-off was proposed in the literature [19] – [23], modern analog controllers still use classical PI or type-II compensation networks while digital controllers typically utilize some kind of gain scheduling to improve DC link voltage behavior during transients thus sacrificing the THD [24]. Thus, the inherent trade-off between grid-side power quality and DC link voltage deviation during load variation still exists.

In order to allow better understanding of the phenomena, several practical assumptions are made in the paper in order to establish clear analytical relations between grid-side current THD, DC link voltage overshoot and settling time following a step-like load change, amount of DC link capacitance utilized per kW rating, voltage loop crossover frequency and phase margin. It is shown that for a given THD, multiple values of DC link undershoot may be attained. However, region of feasible solutions is quite narrow and settling time is different for each selected performance merits pair.

The rest of the paper is organized as follows. PFCR essentials are briefly reviewed in Section II. Steady-state and transient performances are discussed in Sections III and IV, respectively. Guidelines

for voltage controller design based on revealed analytical expressions are given in Section V. Region of convergence is obtained in Section VI. Several practical examples are elaborated in Section VII and experimentally validated in Section VIII using a typical 500W bridge-PFCR prototype. The paper is concluded in Section IX.

II. POWER FACTOR CORRECTION RECTIFIER ESSENTIALS

A typical grid-connected AC/DC power conversion system is depicted in Fig. 1(a). The system consists of a PFCR, bulk DC link capacitance C_{DC} and (optional) down-stream DC/DC converter (DSC). Corresponding functional diagram of the system is given in Fig. 1(b) [5]. In the following discussion, both converters are assumed ideal for simplicity (without loss of generality).

(a) Generalized topology.

(b) Low-frequency functional diagram.

Fig. 1. Typical grid-connected dual-stage power conversion system with PFCR.

Fig. 2. Typical PFCR voltage loop structure.

Typical PFCRs employ dual-loop controller structure, shown in Fig. 2 [17], with outer (voltage) loop regulating the DC link voltage to the set point value V_{DC}^* via using a PI controller

$$C_V(s) = K \frac{\tau s + 1}{s} \quad (1)$$

as voltage loop compensator. The controller calculates desired grid-side current magnitude i_{GM}^* , which is then multiplied by unity-grid-voltage template $\sin(\omega_G t)$ to create grid-side current reference i_G^* , which is then tracked by inner (current) loop. Since only the voltage controller is of interest in this work, current loop is represented in Fig. 2 by its complementary sensitivity function $T_i(s)$. Moreover, current loop bandwidth is typically much higher than grid frequency, hence

$$T_i(s) \approx 1 \quad (2)$$

may be assumed for frequencies up to ω_G [18]. PFCR grid-side voltage and current are given by

$$v_G(t) = v_{GM}(t) \sin(\omega_G t), \quad i_G(t) = i_{GM}(t) \sin(\omega_G t) \quad (3)$$

with ω_G denoting grid frequency and $v_{GM}(t)$ and $i_{GM}(t)$ representing corresponding slow-varying (constant in steady-state) magnitudes. Instantaneous grid-side power is then

$$\begin{aligned} p_G(t) &= v_G(t) i_G(t) = \underbrace{0.5 v_{GM}(t) i_{GM}(t)}_{p_{GM}(t)} + \underbrace{\left(-0.5 v_{GM}(t) i_{GM}(t) \cos(2\omega_G t) \right)}_{p_{GM}(t)} \\ &= p_{GM}(t) + \underbrace{\left(-p_{GM}(t) \cos(2\omega_G t) \right)}_{\Delta p_G(t)} = p_{GM}(t) + \Delta p_G(t) \end{aligned} \quad (4)$$

with $p_{GM}(t)$ representing slow-varying (constant in steady-state) average power and $\Delta p_G(t)$ signifying pulsating power component. Denoting slow-varying (constant in steady-state) load-side instantaneous power as $p_L(t) = v_L(t) i_L(t)$, DC-link power balance (cf. Fig. 1b) is given by

$$p_{DC}(t) = v_{DC}(t) i_{DC}(t) = p_G(t) - p_L(t) = p_{GM}(t) - p_L(t) + \Delta p_G(t). \quad (5)$$

Corresponding DC link energy and voltage are obtained as

$$e_{DC}(t) = e_{DC}(0) + \int_0^t p_{DC}(\tau) d\tau = e_{DC}(0) + \int_0^t (p_{GM}(\tau) - p_L(\tau) + \Delta p_G(\tau)) d\tau \quad (6)$$

and

$$v_{DC}(t) = \sqrt{\frac{2e_{DC}(t)}{C_{DC}}} = v_{DC}(0) \sqrt{1 + \frac{2}{v_{DC}^2(0) C_{DC}} \int_0^t (p_{GM}(\tau) - p_L(\tau) + \Delta p_G(\tau)) d\tau}, \quad (7)$$

respectively, with $v_{DC}(0) = \sqrt{\frac{2e(0)}{C_{DC}}}$.

III. STEADY-STATE PERFORMANCE

In steady state $p_{GM}(t)$ and $p_L(t)$ are constant

$$p_{GM}(t) = P_{GM} = P_L = p_L(t), \quad (8)$$

with

$$v_{GM}(t) = V_{GM}, \quad i_{GM}(t) = I_{GM}, \quad P_{GM} = 0.5V_{GM}I_{GM}. \quad (9)$$

Thus, (7) reduces to [25]

$$v_{DC}^{ss}(t) = V_{DC,rms}^* \sqrt{1 - \frac{P_L}{\omega_G (V_{DC,rms}^*)^2 C_{DC}} \sin(2\omega_G t)}, \quad V_{DC,rms}^* \approx V_{DC}^* \sqrt{1 + \left(\frac{P_L}{2\sqrt{2}\omega_G C_{DC} (V_{DC}^*)^2} \right)^2} \quad (10)$$

with V_{DC}^* denoting DC link voltage set point (cf. Fig. 2). In typical cases, DC link voltage ripple magnitude (ΔV_{DC} in (11)) is much smaller than DC link voltage set point. Therefore, (9) and (10) may be further simplified as

$$v_{DC}^{ss}(t) \approx V_{DC}^* - \underbrace{\frac{P_L}{2\omega_G V_{DC}^* C_{DC}}}_{\Delta V_{DC}} \sin(2\omega_G t) = V_{DC}^* - \Delta V_{DC} \sin(2\omega_G t). \quad (11)$$

Hence, steady-state operation point is a superposition of DC and double-grid-frequency terms, given by (cf. (1), (9) and (12))

$$\begin{aligned} V_{DC}|_{\omega=0} &\approx V_{DC}^*, \quad I_{GM}|_{\omega=0} \approx I_{GM}^*|_{\omega=0} \approx \frac{2P_L}{V_{GM}}, \\ \vec{V}_{DC}|_{\omega=2\omega_G} &\approx \frac{P_L}{2\omega_G V_{DC}^* C_{DC}} \angle \pi. \end{aligned} \quad (12)$$

The steady-state double-grid-frequency component of i_{GM} is obtained as

$$\vec{I}_{GM}|_{\omega=2\omega_G} \approx \vec{I}_{GM}^*|_{\omega=2\omega_G} = \vec{V}_{DC}|_{\omega=2\omega_G} \cdot C_V(2\omega_G) = \frac{2P_L K \sqrt{(2\omega_G \tau)^2 + 1}}{8\omega_G^2 V_{DC}^* C_{DC}} \angle \left(0.5\pi + \tan^{-1}((2\omega_G \tau)^2) \right) \quad (13)$$

and hence

$$i_{GM}^{ss}(t) \approx i_{GM}^{*ss}(t) = \frac{2P_L}{V_{GM}} \left(1 + \frac{V_{GM} K \sqrt{(2\omega_G \tau)^2 + 1}}{8\omega_G^2 V_{DC}^* C_{DC}} \cos\left(2\omega_G t + \tan^{-1}((2\omega_G \tau)^2)\right) \right). \quad (14)$$

Steady-stage grid-side current is then obtained as (cf. Fig. 2 and (14))

$$\begin{aligned}
i_G^{ss}(t) &\approx i_G^{*ss}(t) = i_{GM}^{*ss}(t) \sin(\omega_G t) = \frac{2P_L}{V_{GM}} \left(1 + \frac{V_{GM} K \sqrt{(2\omega_G \tau)^2 + 1}}{8\omega_G^2 V_{DC}^* C_{DC}} \cos\left(2\omega_G t + tg^{-1}\left((2\omega_G \tau)^2\right)\right) \right) \sin(\omega_G t) = \\
&= \frac{2P_L}{V_{GM}} \left(\sin(\omega_G t) - \frac{V_{GM} K \sqrt{(2\omega_G \tau)^2 + 1}}{16\omega_G^2 V_{DC}^* C_{DC}} \sin\left(\omega_G t - tg^{-1}\left((2\omega_G \tau)^2\right)\right) + \right. \\
&\quad \left. + \frac{V_{GM} K \sqrt{(2\omega_G \tau)^2 + 1}}{16\omega_G^2 V_{DC}^* C_{DC}} \sin\left(3\omega_G t + tg^{-1}\left((2\omega_G \tau)^2\right)\right) \right). \tag{15}
\end{aligned}$$

Consequently, grid-side current THD is given by

$$\begin{aligned}
THD &= \frac{\frac{V_{GM} K \sqrt{(2\omega_G \tau)^2 + 1}}{16\omega_G^2 V_{DC}^* C_{DC}}}{\sqrt{1 - \frac{V_{GM} K \sqrt{(2\omega_G \tau)^2 + 1}}{8\omega_G^2 V_{DC}^* C_{DC}} \cos\left(tg^{-1}\left((2\omega_G \tau)^2\right)\right) + \left(\frac{V_{GM} K \sqrt{(2\omega_G \tau)^2 + 1}}{8\omega_G^2 V_{DC}^* C_{DC}}\right)^2}}. \tag{16}
\end{aligned}$$

In practical systems, the following approximation holds [19]

$$\frac{V_{GM} K \sqrt{(2\omega_G \tau)^2 + 1}}{8\omega_G^2 V_{DC}^* C_{DC}} \ll 1, \tag{17}$$

thus (16) may further be simplified as

$$THD \cong \frac{V_{GM} K \sqrt{(2\omega_G \tau)^2 + 1}}{16\omega_G^2 V_{DC}^* C_{DC}}. \tag{18}$$

IV. TRANSIENT PERFORMANCE

Combining (2) and (3), there is

$$C_{DC} \frac{dv_{DC}(t)}{dt} v_{DC}(t) = 0.5 v_{GM}(t) i_{GM}(t) - p_L(t) + \Delta p_G(t). \quad (19)$$

Perturbing the variables in (11) as

$$\begin{aligned} v_{DC}(t) &= V_{DC} + \tilde{v}_{DC}(t), \quad v_{GM}(t) = V_{GM} + \tilde{v}_{GM}(t), \quad i_{GM}(t) = I_{GM} + \tilde{i}_{GM}(t), \quad p_L(t) = P_L + \tilde{p}_L(t), \\ \Delta p_G(t) &= -\underbrace{0.5 V_{GM} I_{GM}}_{P_G} \cos(2\omega_G t) - \underbrace{0.5 (V_{GM} \tilde{i}_{GM}(t) + I_{GM} \tilde{v}_{GM}(t))}_{\tilde{p}_{GM}(t)} \cos(2\omega_G t) = -(P_L + \tilde{p}_{GM}(t)) \cos(2\omega_G t) \end{aligned} \quad (20)$$

and linearizing around the operation point (12) yields

$$\frac{d\tilde{v}_{DC}(t)}{dt} = \frac{1}{C_{DC} V_{DC}^*} \left(0.5 (V_{GM} \tilde{i}_{GM}(t) + I_{GM} \tilde{v}_{GM}(t)) - \tilde{p}_L(t) - \underbrace{\tilde{p}_{GM}(t) \cos(2\omega_G t)}_{\tilde{p}_{GM2}(t)} \right). \quad (21)$$

In practice, grid voltage magnitude variations are infrequent and rather slow, hence

$$v_{GM}(t) = V_{GM} = \text{const} \Rightarrow \tilde{v}_{GM}(t) = 0 \quad (22)$$

is further assumed. Corresponding small-signal representation of the system is depicted in Fig. 3.

Fig. 3. Small-signal representation of PFCR voltage loop structure.

Load power-to-DC link voltage transfer function is then derived as

$$\frac{\tilde{v}_{DC}(s)}{\tilde{p}_L(s)} \approx -G_n \frac{s}{s^2 + 2\xi_n \omega_n s + \omega_n^2} \quad (23a)$$

with

$$G_n = \frac{1}{C_{DC} V_{DC}^*}, \quad \omega_n = \sqrt{\frac{0.5 K V_{GM}}{C_{DC} V_{DC}^*}}, \quad \xi_n = \sqrt{\frac{0.5 K V_{GM}}{C_{DC} V_{DC}^*}} \frac{\tau}{2} = \omega_n \frac{\tau}{2}. \quad (23b)$$

Consequently, a step-like load power increase ΔP_L leads to DC link voltage perturbation given by

$$\tilde{p}_L(s) = \frac{\Delta P_L}{s} \Rightarrow \tilde{v}_{DC}(s) = -\frac{G_n \Delta P_L}{s^2 + 2\xi_n \omega_n s + \omega_n^2} \quad (24)$$

or

$$\tilde{v}_{DC}(t) = -\frac{G_n \Delta P_L}{\omega_n \sqrt{1-\xi_n^2}} e^{-\xi_n \omega_n t} \sin\left(\omega_n \sqrt{1-\xi_n^2} t\right). \quad (25)$$

Maximum DC link voltage deviation caused by the load step is then given by

$$\max |\tilde{v}_{DC}(t)| = \frac{G_n |\Delta P_L|}{\omega_n} e^{-\frac{\xi_n \cos^{-1} \xi_n}{\sqrt{1-\xi_n^2}}}. \quad (26)$$

The worst case load step is the no-load-to-full load transition. Hence, for a P_{LR} -rated system, (26)

becomes

$$\max |\tilde{v}_{DC}(t)| = \frac{G_n P_{LR}}{\omega_n} e^{-\frac{\xi_n \cos^{-1} \xi_n}{\sqrt{1-\xi_n^2}}}. \quad (27)$$

Taking into account the pulsating voltage component in (11), minimum value of DC link voltage may be approximated by

$$\min |v_{DC}(t)| \approx V_{DC}^* - P_{LR} \left(\frac{G_n}{\omega_n} e^{-\frac{\xi_n \cos^{-1} \xi_n}{\sqrt{1-\xi_n^2}}} + \frac{1}{2\omega_G V_{DC}^* C_{DC}} \right). \quad (28)$$

Consequently, the worst-case DC link voltage undershoot is defined as

$$US = \frac{V_{DC}^* - \min |v_{DC}(t)|}{V_{DC}^*} = \frac{P_{LR}}{C_{DC} (V_{DC}^*)^2} \left(\frac{1}{\omega_n} e^{-\frac{\xi_n \cos^{-1} \xi_n}{\sqrt{1-\xi_n^2}}} + \frac{1}{2\omega_G} \right). \quad (29)$$

V. CONTROLLER COEFFICIENTS DERIVATION

For a given desired performance merits pair (THD^* , US^*), design equations set is given by (cf.

(18), (23) and (29))

$$\frac{P_{LR}}{C_{DC}(V_{DC}^*)^2} \left(\frac{1}{\omega_n} e^{-\frac{\xi_n \cos^{-1} \xi_n}{\sqrt{1-\xi_n^2}}} + \frac{1}{2\omega_G} \right) = US^*, \quad (30a)$$

$$\frac{V_{GM} K \sqrt{(2\omega_G \tau)^2 + 1}}{16\omega_G^2 V_{DC}^* C_{DC}} = \frac{\omega_n^2}{8\omega_G^2} \sqrt{\frac{16\xi_n^2 \omega_G^2}{\omega_n^2} + 1} = THD^*. \quad (30b)$$

According to Fig. 3 and (23b), voltage loop gain is given by

$$L(s) = \omega_n^2 \frac{\tau s + 1}{s^2}. \quad (31)$$

Denoting the crossover frequency and phase margin as ω_c and PM , respectively, the following holds

$$\angle L(\omega_c) = tg^{-1}(\omega_c \tau) - \pi = -\pi + PM \Rightarrow PM = tg^{-1} \left(2\sqrt{2}\xi_n^2 \sqrt{1 + \sqrt{1 + \frac{1}{4\xi_n^4}}} \right). \quad (32a)$$

$$|L(\omega_c)| = \frac{\omega_n^2}{\omega_c^2} \sqrt{(\omega_c \tau)^2 + 1} = 1 \Rightarrow \omega_c = \xi_n \omega_n \sqrt{2 + 2\sqrt{1 + \frac{1}{4\xi_n^4}}} \quad (32b)$$

In practical systems, $PM > 40^\circ$ is typically considered [3], i.e. (cf. (32a)) $\xi_n > 0.4$ should be taken into account. Denoting (cf. (30a))

$$-\frac{\xi_n \cos^{-1} \xi_n}{\sqrt{1-\xi_n^2}} = x \quad (33)$$

and plotting x versus ξ_n within the region of interest (see Fig. 4) allows to approximate

$$x = -\frac{\xi_n \cos^{-1} \xi_n}{\sqrt{1-\xi_n^2}} \approx -0.82\xi_n - 0.2, \quad 0.4 \leq \xi_n \leq 1. \quad (34)$$

Moreover, taking into account the fact that in practice $\omega_c \ll \omega_G$ and noticing that (cf. (32b)) $\omega_n < \omega_c$ for $\xi_n > 0.4$, it may be concluded that

$$16 \frac{\xi_n^2}{\omega_n^2} \omega_G^2 \gg 1. \quad (35)$$

Fig. 4. Linear fit of x in (34).

Thus, (30b) may be further simplified as

$$THD^* \approx \xi_n \frac{\omega_n}{2\omega_G}, 0.4 \leq \xi_n \leq 1. \quad (36)$$

Substituting (36) and (34) into (30a) and solving yields

$$\begin{aligned} \xi_n &= -\frac{1}{0.82} W \left\{ THD^* \left(1 - \frac{2\omega_G C_{DC} (V_{DC}^*)^2}{P_{LR}} US^* \right) \right\} \\ \omega_n &= \frac{2\omega_G}{\xi_n} THD^*, \end{aligned} \quad (37)$$

where $W\{ \}$ signifies the Lambert-W function [26]. Coefficients of the voltage loop compensator (1) are then derived as (cf. (23b))

$$K = \frac{2C_{DC}V_{DC}^*}{V_{GM}} \omega_n^2, \quad \tau = \frac{2\xi_n}{\omega_n}. \quad (38)$$

VI. REGION OF CONVERGENCE

In order to have $0.4 < \xi_n < 1$ in (37),

$$0.236 < THD^* \left(2\omega_G \left(V_{DC}^* \right)^2 \frac{C_{DC}}{P_{LR}} US^* - 1 \right) < 0.361 \quad (39)$$

must hold. Hence, attainable undershoot values are bounded by

$$US^* > \frac{1}{2\omega_G \frac{C_{DC}}{P_{LR}} \left(V_{DC}^* \right)^2} = US_{\min}^*. \quad (40)$$

Fig. 5. Region of feasible performance merit pairs for different C_{DC}/P_{LR} values.

Fig. 5 presents regions of feasible performance merit pairs for different C_{DC}/P_{LR} values (cf. (39)) for $V_{DC}^* = 400V$ and 50Hz mains and $3\% < THD^* < 7\%$. It may be concluded that increasing the amount of DC link capacitance per kW utilized improves the attainable $THD - US$ trade-off. It is important to emphasize that C_{DC}/P_{LR} influences not only the region of convergence, but also the steady-state DC link voltage ripple magnitude ΔV_{DC} (cf. (11)) and the hold-up time. Fig. 6 depicts the steady-state DC link voltage ripple magnitude versus different C_{DC}/P_{LR} values for $V_{DC}^* = 400V$ and 50Hz mains neglecting the DC link capacitor ESR. It may be concluded that increasing the amount of DC link capacitance per kW utilized reduces the steady-state DC link voltage ripple magnitude.

Fig. 6. Steady-state DC link voltage ripple magnitude vs. different C_{DC}/P_{LR} values.

Once C_{DC}/P_{LR} value is decided on and one of the two performance merits (typically the THD^*) is imposed, the value of the other performance merit may be selected within the region given by (39). It must be emphasized that selection of the second performance merit would affect the phase margin, loop gain crossover frequency and the $y\%$ -settling time $T_s^{y\%}$, obtained using (25) as

$$T_s^{y\%} = -\frac{1}{\xi_n \omega_n} \ln \left(\frac{y\%}{100} \left(V_{DC}^* \right)^2 \omega_n \sqrt{1 - \xi_n^2} \frac{C_{DC}}{P_L} \right). \quad (41)$$

VII. EXAMPLES

In practical single phase PFCRs, DC link voltage reference is typically set to $360V \leq V_{DC}^* \leq 400V$. Moreover, supported grid magnitudes may reside within $85\sqrt{2}V \leq V_{GM} \leq 265\sqrt{2}V$. In order to assure correct operation of PFCR (typically possessing boost topology), instantaneous value of DC link voltage should remain above its grid-side counterpart both in steady-state and during transients. On the other hand, $v_{DC}(t)$ should also remain below the rated voltage of DC link capacitors utilized, in order to prolong their lifetime.

Fig. 7. Region of feasible performance merit pairs for $C_{DC}/P_{LR} = 570 \mu F/kW$.

Considering 50Hz, 230Vrms mains and allowing typical 10% grid voltage magnitude deviation, the maximum expected PFCR input voltage would be around 358V. On the other hand, 450V-rated capacitors are commonly used. Therefore, tolerated DC link undershoot would be 0.1 at most. On the other hand, power quality standards impose strict THD upper limits depending on the application and power level with 5% value being one of the common values [27]. Consequently, $(THD^*, US^*) = (0.05, 0.1)$ is a common desired performance merits pair. According to (39), the minimum value of C_{DC}/P_{LR} allowing to attain this performance merits pair is $570 \mu F/kW$. Corresponding region of feasible performance merit pairs (cf. (39)) is shown in Fig. 7. This amount of DC link capacitance per kW

imposes steady-state DC link voltage ripple magnitude of 7V (cf. (11), neglecting the DC link capacitor ESR), 2%-settling time of 65ms (cf. (41)) and hold-up time of 7.1ms. Bode diagram of resulting voltage loop gain (cf. (31)) is depicted in Fig. 8, with $\omega_c = 2\pi \cdot 14.6 \text{ rad/s}$ and $PM = 43.2^\circ$ values, accurately predicted by (32). Simulated system response to zero – to – 100% load step applied at 0.05s is shown in Fig. 9. It is well-evident that the desired performance merits pair, steady-state DC link voltage ripple magnitude and predicted 2%-settling time are accurately respected.

Fig. 8. Bode diagram of the voltage loop gain for $C_{DC}/P_{LR} = 570 \mu\text{F/kW}$.

Fig. 9. Closed-loop system response to no load – to – full load step for $C_{DC}/P_{LR} = 570 \mu\text{F/kW}$.

In case 10ms hold-up time is required (mains half-cycle), the required capacitance raises to about 770 μ F/kW. This amount of DC link capacitance per kW rating imposes steady-state DC link voltage ripple magnitude of 5.2V (cf. (11), neglecting the DC link capacitor ESR). Corresponding region of feasible performance merit pairs (cf. (39)) is shown in Fig. 10. It may be concluded that for 0.1 undershoot, the system may attain *THD* theoretical minimum of 3.5%.

Fig. 10. Region of feasible performance merit pairs for $C_{DC}/P_{LR} = 770\mu\text{F/kW}$.

Fig. 11. Current spectra (excluding the fundamental harmonic of 2.3A) of a commercial PFCR [27], [28].

It should be emphasized that even though (15) indicates that only the 3rd harmonic contributes to

grid current THD , in practical systems additional odd and even harmonics (of lower magnitudes) typically appear due to parameter non-idealities, circuit non-linearity, etc. Fig. 11 depicts the grid-side current spectra of Texas Instruments Evaluation Module [27] for UCC28180 Power Factor Correction Controller [28], operated from 50Hz, 230Vrms mains. The 5th harmonic is the most significant one (after the 1st and the 3rd), increasing the THD value predicted by (18) by $\sim 10\% - 15\%$. Consequently, in order to obtain grid-current THD of 5%, THD^* should be set to 4.3% – 4.5%.

(a) vs US^* for $THD^* = 4.5\%$.

(b) vs THD^* for $US^* = 0.1$.

Fig. 12. Settling time for $C_{DC}/P_{LR} = 770\mu F/kW$.

Fig. 12(a) depicts the relation between 2%-settling time and US^* for $THD^* = 4.5\%$ while Fig. 12(b) presents 2%-settling time vs US^* for $THD^* = 4.5\%$. It may be concluded that for a fixed THD^* , rising US^* yields settling time increase. On the other hand, $T_s^{2\%}$ vs THD^* plot possesses a certain minimum for a given US^* . Bode diagrams of corresponding voltage loop gains is depicted in Fig. 13 with desired performance pair $(THD^*, US^*) = (0.045, 0.08)$ attaining the highest crossover frequency and lowest phase margin of $(\omega_c, PM) = (2\pi \cdot 13.3 \text{ rad/s}, 42.5^\circ)$ and desired performance pair $(THD^*, US^*) = (0.045, 0.116)$ attaining the lowest crossover frequency and highest phase margin of $(\omega_c, PM) = (2\pi \cdot 9.29 \text{ rad/s}, 75.6^\circ)$.

Fig. 13. Bode diagrams of the voltage loop gain for different performance merit pairs and $C_{DC}/P_{LR} = 770\mu\text{F/kW}$.

VIII. EXPERIMENTAL RESULTS

In order to experimentally verify the proposed methodology, a 500W boost converter-based PFCR was employed, as shown in Fig. 14. The control system was implemented digitally using TMS320F28335 DSP-based control card. Average current control at a fixed switching frequency of 150 kHz was adopted in the inner loop. The PFCR was fed by APS-7100 Gwinstek programmable AC power source set to operate as 50Hz, 230V mains and terminated by M9715B Maynuo DC electronic load set to operate in constant power mode.

Fig. 14. Experimental setup schematic.

The total DC link capacitance value (including electronic load input capacitance) was $C_{DC} = 385\mu\text{F}$, realizing $C_{DC}/P_{LR} = 770\mu\text{F/kW}$ in order to match the Example in the preceding Section and the DC link voltage was regulated to $V_{DC}^* = 400\text{V}$. Five sets of controller coefficients derived according to the five desired performance pairs indicated in Fig. 10 were utilized. During experiments, system responses to zero – to – 100% load step were logged to quantity DC link voltage undershoot and settling time. Moreover, steady-state grid-side current spectra were recorded to obtain 1st, 3rd and 5th harmonic magnitudes and corresponding THD values were measured.

Experimental results are shown in Figs. 15 – 19. Steady-state DC link voltage ripple magnitudes were around 5.5V in all cases, which is slightly higher than the expected 5.2V due to DC link capacitor ESR. While the resulting undershoot values accurately followed the desired values, the resulting THD values are up to 15% higher than the desired ones due to additional harmonics present

in current spectra, as predicted. Nevertheless, in case the value of the 3rd harmonic only is taken into account for *THD* calculation, the outcomes closely follow the desired values. Measured settling times are indicated in Fig. 12, accurately matching corresponding analytical predictions.

Fig. 15. Experimental results, $(THD^*, US^*) = (0.045, 0.08)$.

Fig. 16. Experimental results, $(THD^*, US^*) = (0.045, 0.1)$.

Fig. 17. Experimental results, $(THD^*, US^*) = (0.045, 0.116)$.

Fig. 18. Experimental results, $(THD^*, US^*) = (0.035, 0.1)$.

Fig. 19. Experimental results, $(THD^*, US^*) = (0.04, 0.1)$.

IX. CONCLUSION

In this paper, analytical expressions linking grid-side current THD and DC link voltage undershoot of a power factor correction rectifier with corresponding settling time, voltage loop gain crossover frequency and phase margin were established and utilized for PI voltage controller coefficients derivation. Region of feasible solutions was also determined and defined analytically. It was shown that amount of DC link capacitance per kW rating influences the trade-off between the two performance merits. Revealed findings were successfully verified by simulations and experiments.

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