Design Project Using 45nm CMOS

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Design Project Using 45nm CMOS

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Abstract— this project is aimed to design two impedances matching network to let the source degeneration and common gate amplifier to achieve the ideal characteristic. In the source degeneration case as the resistance is so small, so we just use down converting matching network. As the source degeneration gives us a high resistance, we just match with a up converting network.

Index Terms— source degeneration, common gate amplifier, LNA.

I. INTRODUCTION

The objective is to minimize the input noise figure and S11 and maximize the voltage gain for a source degeneration amplifier and a common gate amplifier operating at 10GHz from 1.2V supply voltage using 45nm CMOS gpdk. There are four characteristics should be follow. S11 at 10GHz should less than -40dB, voltage gain should more than 20dB, Noise figure should less than 2dB, DC power should less than 1mW.

In the source degeneration case, L_g and L_d are ideal induction, the other components are all non-ideal which means the other components may have noise in it and the value of these components vary in a small range. As we know that the source degeneration amplifier's gain is related to the impedance at source node and the impedance at drain node, so we may easily calculate the gain $= -L_d/L_s$ and this may help us to select the value of L_d cause L_s is a non-ideal inductor and we should select L_d to match the L_s value.

In the common gate amplifier, L_d is an ideal inductor but the other components are non-ideal. As we know that the common gate gain $= g_m \cdot r_{ds}$, and $R_{in} = g_m \cdot L_s / C_{gs}$, we may know how to select the width and length of the mosfet to get the proper g_m , r_{ds} and C_{gs} .

II. PROCEDURE FOR PAPER SUBMISSION

A. Review Stage

To finish the project, there are so many step should follow.

--First, analysis the circuit and build up the proper test bench, then us the DC analysis in cadence to let the nmos transistor works in saturation region.

--Second, knowing that in source degeneration case, we should use up converting matching network so we just use narrow band matching network to match the test port's 50Ω to the impedance seen from gate. As we should let the whole

circuit have low noise factor which means we should use less components to finish the matching.

--Third, then we just use ADE in cadence and use AC analysis to select the port 1 and port 2 to calculate the S-parameter.

--Fourth, we select the input port and output port to calculate the voltage gain.

--Fifth, change the test bench by deleting the two port and select the supple by adding noise then use ADE to see the noise factor.

--Sixth, as noise factor is related not only by noise at source, but also related to the amplifier's gain, so we just changed the value of inductor and mosfet's width and length to get the better value of noise factor.

--Seventh, the common gate amplifier has the same procedure as the source degeneration.

III. FINAL DESIGN RESULT

In source degeneration case:

Fig. 1 figure for CS test bench when calculate S11.

MOS	Length 45nm Width 2um
L_g	10mH
L_i	4.2nH
C_i	3.505fF
L_s	2.527nH
L_d	10mH

Table1 for the value of component

Fig. 2 figure of S11.

Fig. 5 smith chart

Fig. 3 figure for the result of gain

Fig. 4 figure of noise factor

Edit Object Properties

Apply To:

Show: ☐ system ☒ user ☒ CDF

Property	Value	Display
Library Name	gpdK045	off
Cell Name	ind_a	value
View Name	symbol	off
Instance Name	L10	off

CDF Parameter	Value	Display
Inductance (H)	4.20578e-09	off
Inner Radius	29.0u M	off
Inductor Width	3u	off
Inductor Space	1.5u M	off
Model	ind_a	off
multiplier	1	off
Number Of Turns	5.5	off

Fig. 6 inductor Li

Edit Object Properties

Apply to: ☐ system ☒ user ☒ CDF

Show: ☐ system ☒ user ☒ CDF

Browse Reset Instance Labels Display

Property	Value	Display
Library Name	gpdK045	off
Cell Name	mimcap	value
View Name	symbol	off
Instance Name	C0	off

Add Delete Modify

User Property	Master Value	Local Value	Display
lastSavedAutoEx...	13:02:49 1996		off

CDF Parameter

Model name	Value	Display
Calculate Parameter	capacitance	off
Capacitance	3.505f F	off
Width & Length	2u M	off
Multiplier	1	off
Area capacitance (F/M^2)	0.001025	off
Fringe capacitance (F/M)	2.425e-10	off
Area	iPar("w")*iPar("l")	off
Perim	2*iPar("w")+2*iPar("l")	off

OK Cancel Apply Defaults Previous Next Help

Fig. 7 mimcap Ci

Figure 1 to 7 shows the test bench for source degeneration and the value of S11, voltage gain and noise factor.

In common gate case:

Fig. 8 figure for CG test bench when calculate S11.

MOS	Length 45nm Width 210um
Vbias	2.1V
Li	0.3525nH
Ci	100pF
Ld	1mH
Co	100pF

Table1 for the value of component

Fig. 9 figure of S11.

Fig. 10 figure for the result of gain

Fig. 11 figure of noise factor

Fig. 12 smith chart

Fig. 14 Smith Chart

Figure 8 to 14 shows the test bench for calculate S11, voltage gain and noise factor.

Edit Object Properties

Apply To:

Show: ☐ system ☒ user ☒ CDF

Property	Value	Display
Library Name	gpdK045	off
Cell Name	ind_a	value
View Name	symbol	off
Instance Name	L0	off

CDF Parameter	Value	Display
Inductance (H)	3.52515e-10	off
Inner Radius	28.0u M	off
Inductor Width	1u	off
Inductor Space	1.5u M	off
Model	ind_a	off
multiplier	1	off
Number Of Turns	1.5	off

Fig. 13 inductor Li

IV. DISCUSS

This project aimed to let us know how to design a LNA by knowing the characteristic of it. At first the professor told us to use non-ideal components to finish the design, which means the component cannot select the ideal value, so we just by fixed the inductor's value and then select the capacitor's value because the range of capacitor is larger than inductor. Then we also know that we should transform the central frequency to 10GHz and let the S11, noise factor have the optimize value at 10GHz.

At first we just want to calculate the noise factor, S11 and voltage gain in the same test bench, then we find that these three characteristic have trade off relationship because when we get a good S11 value we may not let the noise factor to become small at 10GHz which means we should use two test benches to get the S11 and noise factor.

V. CONCLUSION

In this project we know that we should know how to select the non-ideal component's value because we cannot use ideal components in real circuit, and we also know that there is trade off relationship between the characteristic of amplifier.

APPENDIX

The hand calculation that amplifier required, has already been written down on the A4 paper.

ACKNOWLEDGMENT

Thank you of the help of teacher.

REFERENCES

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