Design of a Novel CMOS Voltage Divider

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Abstract—Passive linear voltage dividers are an essential part of the voltage sensing and detecting circuits. In this paper, a novel voltage divider is designed in 180nm CMOS technology and is validated with LTSpice simulations. The proposed circuit features very low steady current consumption and as a result, very little power dissipation around 200-300pW.

Index Terms—CMOSFET circuits, CMOS voltage divider, Low power consumption, Voltage measurement

I. INTRODUCTION

FOR voltage sensing applications, voltage dividers are essential to scale down high voltage to a lower level for comparing it with a reference voltage. Voltage dividers make it easy for microcontrollers with analog to digital converters to measure the voltage. One of the most widely accepted voltage dividers consists of several identical resistors connected in series between the supply voltage (VDD) and ground. The voltage distributes evenly on the resistors (if the resistors are equally valued), and the desired output level can be obtained from the correct node.

In the case of two resistors connected in series from VDD to ground, the current flowing is equal to $VDD / (R_1 + R_2)$. The expression for the output voltage is given as,

$$V_{out} = \frac{R_2}{R_1 + R_2} V_{DD}$$

Where R_2 is the resistance connected between the output voltage and the ground.

The advantages of this traditional design are stability, accuracy, and robustness. However, there is a finite resistance between the supply rails, and therefore, a significant steady current keeps flowing throughout the operation. This steady-state current can be reduced by increasing the resistance value. But this, in turn, takes up extra area on the chip that might double the size of the whole system. Even if the resistance is increased substantially, there will still be some Nano amperes or microamperes of current flowing constantly.

One other problem is that higher voltages mean higher current flowing. If the purpose is to sense the battery voltage, this characteristic of the voltage divider is undesirable.

Voltage dividers can be implemented by NMOS and PMOS, where the width and length of the MOSFETs dictate the voltage division ratio. These MOS-based designs only occupy 0.01% of the area as compared to the resistors.

This paper introduces a novel approach to scale down high DC voltages by taking advantage of the body effect in MOSFETs.

II. THE PROPOSED VOLTAGE SCALING DESIGN

Fig. 1 shows the schematic of the proposed voltage scaling circuit. The design consists of a diode-connected PMOS and a diode-connected NMOS, both connected in series. The bulk terminal of the PMOS transistor M2 is connected to the input voltage that needs to be sensed. The source connects to a stable voltage, and the variation in the bulk-source voltage will affect the threshold voltage of the transistor, varying the drain current. The following approach is beneficial at high DC voltages as there is a very weak dependence of the bulk-source voltage on the drain current of M2. This weak dependence, moreover, makes this circuit capable of operating with low supply voltages.

Fig. 1. The proposed voltage scaling circuit

The PN junction formed by the source and bulk of the MOSFET is a diode and is normally reverse-biased to prevent leakage currents. In this case, we are using the bulk-source voltage to regulate the drain current of the PMOS.

The threshold voltage of a PMOS can be written as

$$V_{TH} = V_{T0p} + \gamma \left((2\phi_f + V_{BS})^{0.5} - (2\phi_f)^{0.5} \right)$$

where V_{T0p} is the threshold voltage when the bulk-source voltage is zero, ϕ_f is a physical parameter and γ is the body-effect parameter.

And the drain current equation for PMOS is given as follows (if the channel length modulation is neglected) [1].

$$I_{D2} = 0.5\mu_p C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{TH})^2$$

It can be observed from both these relationships that if the input voltage increases, or in other words, if the bulk-source voltage increases, drain current and the output voltage also increases. Fig. 2 shows the graphical representation of the relationship between the bulk-source voltage and the drain current

Fig. 2. Relationship between the input voltage and the PMOS drain current

The output voltage can be written as

$$V_{out} = I_{D2}(r_{o1} || r_{o2})$$

III. SIMULATION RESULTS

The design is simulated in LTSpice in the 180nm process. The circuit is operated with a 1V supply (VCC), and input voltage from 25V to 48V with an increment of 1V is provided. Fig. 3 shows the output voltage. The output voltage can be amplified by a gain of 10 or 100 for high resolution. The current consumption is shown in Fig. 4. The current flowing into the bulk of the PMOS from the input is shown in Fig. 5. The overall power consumed from the input voltage is in the vicinity of 200pW - 300pW.

Fig. 3. Scaled output voltage

Fig. 4. Drain current of the PMOS

Fig. 5. Current flowing into the bulk of the PMOS

The current consumption, however, increases as the supply voltage (V_{CC}) increases. To overcome this issue, the PMOS transistor can be used in OFF-state as demonstrated in Fig. 6. In which case, the subthreshold behavior of the MOS transistor has to be taken into account. Fig. 6 shows the output voltage of this circuit, and Fig. 7 shows the current consumption with supply voltage of 5V.

Fig. 6. Voltage scaling circuit with PMOS in OFF state

Fig. 7. Output voltage with turned-off MOSFET and 5V supply

Fig. 8. Current flowing into the bulk of the turned-off MOSFET

IV. CONCLUSION

A voltage scaling circuit has been designed and tested via simulation, which exploits the dependence of the drain current on the bulk-source voltage. This approach offers a very low steady current consumption, consumes the same area as conventional CMOS voltage dividers, can be operated with very low supply voltages, and dissipates very little power from the input.

V. REFERENCES

[1] B. Razavi, Design of Analog CMOS Integrated Circuits, New York:McGraw-Hill, 2000.