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Device-Circuit Co-design of Memristor-based on Niobium Oxide for Large-Scale Crossbar Memory

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Abstract—Memristor-based crossbar architecture emerges as a promising candidate for 3-D memory and neuromorphic computing; however, the sneak current through the unselected cells becomes a fundamental roadblock for their development as it results in misreading and high power consumption. In this regard, we investigate Pt/Ti/NbO₂/Nb₂O_{5-x}/Pt-based self-selective memristor, which combines inherent nonlinearity of NbO₂ switching layer and non-volatile operation of Nb₂O_{5-x} memory layer in a single device. The results show that Pt/Ti/NbO₂/Nb₂O_{5-x}/Pt memristor offers the sneak current of 310 nA, selectivity of around 174, and on/off current ratio of 4.79 compared to the sneak current of around 70 μ A, selectivity of about 4.02, and on/off current ratio of around 1.55 for Pt/Ti/Nb₂O_{5-x}/Pt-based memristor. Our self-selective memristor minimizes the sneak current, but a small on/off current ratio limits their readout margin and power efficiency for crossbar array size greater than 2¹². Further, we demonstrate that breaking down a large-scale crossbar array into smaller subarrays and separating them by transistor switches is a more efficient way of eliminating the sneak current. The memristor-transistor split crossbar architecture essentially provides the readout margin and power efficiency of subarray for large size crossbar array and allows high-density array integration over 1Transistor-1Memristor architecture.

Index Terms—Self-selective, memory computation, numerical modeling, niobium oxide (NbO₂), crossbar architecture

I. INTRODUCTION

With the increasing demand for high-density data storage and high-speed computation in the area of artificial intelligence, internet-of-things, and big data servers, there is an upsurge in the demand of high-storage non-volatile memory and in-memory computing devices [1]. Crossbar array architecture based on resistive random access memory (RRAM) cell is considered as a promising candidate for non-volatile memory due to their low operational power, superior switching speed, and excellent reliability [2], [3]. Despite memristor-based RRAM cell provides a new opportunity to implement energy-efficient and massively parallel system for processing a large amount of information, the sneak current through the unselected memory cells limits the crossbar array size as it reduces the readout margin [4]. Further, the sneak current immensely increases the power consumption of the array and worsens the reliability issues. To suppress the sneak current, the most studied solutions are the integration of switches, such as diode (D), transistor (T), and selector (S), with memristor (M) [4], [5]. In particular, 1T-1M configuration has been widely adopted and demonstrated as an energy-efficient crossbar architecture with TaO_x, Al₂O₃ and HfO₂ memristors [6]–

[8]. However, the integration of a separate switching transistor increases the circuit footprint from $4F^2$ to $20F^2$, where F is the minimum feature size of the process technology [9]. An efficient solution for eliminating the sneak current could be developing the self-selective memristor (SM) cell with built-in nonlinearity, which combines the memristive nonvolatile switching and the threshold-type selector property with high current in a single two-terminal device [10], [11]. Therefore, a novel device and circuit architecture with self-selective memristor are needed for achieving the ultralow sneak current, high speed, and more reliable switching operations.

NbO₂ attracts significant attention for threshold switching device due to the following advantages [12], [13]: (i) exhibits an insulator-to-metal transition (IMT) at high temperature, which could offer thermal stability at the device-operating temperature. (ii) highly non-linear current-voltage (I-V) characteristics, which could prevent the sneak path current through the neighboring cell, and (iii) exhibits bipolar switching characteristics. To avoid the reliability issues, the integration of Nb₂O_{5-x} and NbO₂ layer presents a viable choice for self-selective device development as it has been recently found to be stacked using self-assembled processing [14]. Interestingly, NbO₂/Nb₂O_{5-x}-based self-selective memristors have demonstrated excellent performance with high current density and high on/off current ratio [15], [16]. Even though several recent efforts have been devoted to the understanding of the underlying switching mechanism in NbO₂/Nb₂O_{5-x} based self-selective memristor [15], [17], crossbar-level performance analysis remains unexplored. Therefore, more efforts on crossbar-level performance analysis are required to expand their usage in memory and neuromorphic system design.

In this work, we examine the crossbar array performance of Pt/Ti/NbO₂/Nb₂O_{5-x}/Pt-based memory cell and propose a memristor-transistor split crossbar architecture for constructing a realistic large-scale crossbar array. The performance analysis is performed using multi-scale modeling that connects the three design levels, such as material, device, and circuit. To capture material properties and provide an accurate description of device physics, we have adopted a sophisticated numerical modeling for memristor modeling that involves the self-consistent solutions of drift-diffusion, current continuity, and the heat equation. Further, the current equations are modeled in a professional circuit simulator using the Verilog-AMS interface to conduct static and transient simulations of crossbar architecture. Firstly, we focus on investigating the sneak current in niobium-oxide based self-selective memristor and its effects on the crossbar performance. We subsequently design a scalable memristor-transistor split crossbar array to diminish

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the effect of sneak path current in traditional memristive crossbar arrays. Afterward, we explore the benefits of the split crossbar array over the crossbar array using 1-SM cell and 1T-1M cell.

II. MEMRISTOR GEOMETRY AND MODELING APPROACH

Fig. 1(a) shows that three-dimensional memristor device geometry is considered as a two-dimensional (2-D) cylindrical geometry in our simulation due to symmetry in the axial and radial directions. The threshold switching is realized from the 10 nm NbO₂ switching layer stacked on top of amorphous Nb₂O_{5-x} layer. The NbO₂ exhibits a highly non-linear switching characteristics, while Nb₂O_{5-x} serves as a memristive switching layer. The platinum (Pt) is used as top and bottom electrodes with a thickness of 25 nm and 30 nm, respectively. The Ti electrode of thickness $t_{Ti} = 5$ nm is considered in between NbO₂ layer and top electrode as it prevents oxygen out-diffusion during device operation. The overall cross-section area of the device is around 110×25 nm². Moreover, Pt/Ti/NbO₂/Pt threshold switching (TS) device and Pt/Ti/Nb₂O_{5-x}/Pt memory switching (MS) device are simulated with nearly the same threshold and memory layer thickness, respectively, as considered for the self-selective device.

Fig. 1(b) summarizes the developed multi-scale modeling approach. Firstly, the material attributes of NbO₂ and Nb₂O_{5-x} are acquired from reported experimental data [15], [17]–[19]. Subsequently, these material attributes are used to develop a fully coupled multi-physics simulator for understanding the switching properties of niobium-oxide devices. A multi-physics simulator is developed in commercial COMSOL simulation tool by self-consistently solving differential equations involving current continuity equation, heat conduction equation, and oxygen vacancy (n_{ox}) drift-diffusion equation. Once the current is obtained from multi-physics simulation, a lookup table-based approach is used for modeling current equations in the industry-standard Cadence circuit simulator. The cadence simulation tool is then used to examine the static and dynamic performance metrics of the crossbar array.

A. Modeling of Switching Properties of NbO₂ layer

In general, the threshold switching effect in NbO₂ is attributed to the IMT that occurs at around 1081 K temperature [17], [20]. However, the thermal conductance-based model (σ as a function of T) exhibits major conflicts in comparison to the experimental findings as the internal device temperature is found to be well below the IMT transition temperature during switching [15]. Thus, several recent works have described the switching mechanism in NbO₂ using thermal activation due to joule heating and electric field enhanced conduction mechanisms [12]–[14]. The switching effect in NbO₂ could be triggered when the activation energy is lowered due to the applied electric field. This is explained well by the Poole-Frenkel conduction mechanism. The electric-field assisted

electrical conductivity can be modeled using the Poole-Frenkel effect (PFE) equation as

$$\sigma_{Th} = \sigma_0 \exp \left(-\frac{\Delta W_A - \beta \sqrt{E}}{k_B T} \right) \quad (1)$$

where σ_{Th} is the electrical conductivity of the NbO₂ threshold layer, σ_0 is conductivity pre-factor (9.99×10^6 S/m for NbO₂), ΔW_A (≈ 0.68 eV) is the activation energy of carriers, E is the electric field, k_B is the Boltzmann constant, and T is the temperature across the device. A R_{LRS} of 3.7 k Ω is considered for modeling the pure threshold switching in the device [15]. It is found from Eq. 1 and (5) that the physical origin of the threshold switching effect is explained using the lowering of the activation energy for n_{ox} due to the electric field and joule heating.

Fig. 2 shows the I-V characteristics of Pt/Ti/NbO₂/Pt based threshold switching device using our simulation model based on PFE and reported experiment data [14] at the same device geometry. It is found that our simulation results are in good agreement with reported experiment data for NbO₂ threshold switching device. It proves that the thermal and electric field enhanced conduction mechanisms accurately explain the phenomenon of switching in NbO₂.

B. Multiphysics Modeling Approach

To explain the memristor switching behavior, we have considered the conductive filament (CF) with high n_{ox} and dynamic migration of n_{ox} in Nb₂O_{5-x} memory layer. Fig. 1(a) shows that we consider a continuous CF of size 6 nm in the inner radial region. The conductive filamentary assumption is in good agreement with the experimental studies [21]. The migration of n_{ox} in filamentary and non-filamentary regions is considered to be governed by the hopping process across the barrier, diffusion induced by density gradient, and drift driven by the electric field. Further, n_{ox} is assumed to be activated thermally by solving the Fourier equation for Joule heating, which incorporates the self-heating effect. Thus, migration of n_{ox} is modeled by three partial differential equations including current continuity equation, heat conduction equation, and oxygen vacancy drift-diffusion equations, as shown in Fig. 1(b).

The continuity equation, which represents the time-dependent evolution of n_{ox} , is given as.

$$\frac{\partial n_{ox}}{\partial t} = \nabla (D \nabla n_{ox} - \mu n_{ox} \nabla V + D S n_{ox} \nabla T) \quad (2)$$

The continuity equation has three terms in which the first term describes the diffusion of n_{ox} ; the second term gives the drift motion of n_{ox} ; and the last term accounts for the heat transport due to the movement of molecules along a temperature gradient. The S is the Soret diffusion coefficient, and V is the electrical potential across the device. The diffusion coefficient (D) is used to account for the temperature dependency of the n_{ox} diffusion that is calculated as

$$D = D_0 \exp \left(-\frac{E_a}{k_B T} \right) \quad (3)$$

Figure 1. Simulated geometry and modeling methodology: (a) Pt/Ti/NbO₂/Nb₂O_{5-x}/Pt-based self-selective memristor geometry in 2-D axisymmetric, and (b) multi-scale modeling methodology: the left side shows the main transport equations and the right side demonstrates material-device-circuit analysis approach.

Figure 2. Simulated and experimental [14] I-V characteristics of Pt/Ti/NbO₂/Pt based threshold switching device. The I-V characteristics of the experimental device is measured with 70 μA compliance current (I_{CC}), which is frequently applied to control the resistance of low resistance state and to avoid permanent breakdown of the memristor.

Figure 3. Material attributes of Nb₂O₅: (a) pre-exponential factor of electrical conductivity σ_0 , (b) activation energy (E_{AC}), and (c) thermal conductivity (k_{TH}) as a function of n_{ox} . The maximum and minimum values of E_{AC} are assumed around 53.7 W/m-K and 0.12 W/m-K, respectively, which are in good agreement with experimental data [18], [19]. Further, σ_0 and k_{TH} are considered from previous reported work on Nb₂O_{5-x} [18].

where D_0 is the pre-exponential factor, E_a is the energy barrier for n_{ox} diffusion. The mobility (μ) of n_{ox} can be related to the diffusivity by the Einstein relation as $\mu = \frac{qD}{k_B T}$, where q is the electron charge. Equation 2 is solved self-consistently with the current continuity equation for incorporating the electrical conduction. The current continuity equation is given as

$$\nabla J = \nabla \sigma \nabla V = 0 \quad (4)$$

where J is the current density, and σ is the electrical conductivity. The electrical conductivity of the Nb₂O_{5-x} layer is described by the Arrhenius equation as $\sigma = \sigma_0 \exp\left(-\frac{E_{AC}}{k_B T}\right)$. The E_{AC} is the activation energy for n_{ox} conduction. The σ_0 and E_{AC} are dependent on oxygen vacancy and assumed to increase linearly, as shown in Fig. 3.

For accounting heat conduction in the device, the dynamic Fourier equation for Joule heating is self-consistently solved with Eq. 2 and Eq 4. The dynamic Fourier equation for Joule

heating is given as

$$\rho_m C_p \frac{\partial T}{\partial t} - \nabla \kappa \nabla T = \frac{J^2}{\sigma} \quad (5)$$

where ρ_m is the density of mass. In memristive Nb₂O₅, the κ is assumed to be dependent on n_{ox} , as shown in Fig. 3(c). On the other hand, the thermal conductivity of threshold layer (κ_{Th}) is contributed due to phonons (κ_{ph}) and free electrons (σ_{Th}) [15]. The κ_{Th} is computed as

$$\kappa_{Th} = \kappa_{ph} + LT \sigma_{Th} \quad (6)$$

where L is the Lorenz number that can be obtained from the Wiedemann-Franz law [22]. It is assumed that the device is thermally insulated expect that the outermost thermal boundaries of the top and bottom electrodes are taken as ideal heat sinks, and the Dirichlet boundary condition is applied with a constant value for the ambient temperature. The continuity, current continuity, and Joule heating equations are numerically solved in the COMSOL simulator using finite element method to investigate the static and dynamic behaviour of memristor. The Newton-Raphson approach is adopted inside the self-consistent device solver for computationally efficient solutions of three non-linear PDE equations.

C. Circuit Simulation

A lookup table-based approach is followed for implementing the terminal currents of the device model in a professional Cadence circuit simulator using the Verilog-AMS interface. The write operation in crossbar array is performed using $V/2$ ($V = V_{write} = 2.5$ V) biasing scheme as it exhibits a higher power efficiency over $V/3$ biasing scheme [23]. For the reading operation, the voltage bias of $V_{read} = V_{th}$ is applied on selected cell, while $V_{read}/2$ is appeared on partially selected cells and zero voltage is appeared on unselected cells. Further, in crossbar simulation, we have assumed the wire resistance in the range of 0.1Ω to 10Ω (10Ω is considerably higher than the ITRS 2013 interconnect technology projection) [10], [24], [25].

III. RESULTS AND DISCUSSION

Fig. 4(a) shows the I-V characteristics of Pt/Ti/Nb₂O₅/Pt memristor device. It is observed that memristor exhibits bipolar switching behavior with SET and RESET transitions for positive and negative voltages, respectively. The SET transition, which is a high resistance state (HRS) to low resistance state (LRS) transition, appears when negatively charged n_{ox} migrate towards the top electrode (TE). This results in the formation of conductive filament (CF). On the other hand, RESET transition, i.e., breaking of CF, is observed when n_{ox} migrate towards the bottom electrode (BE). The positive SET voltage indicates that memristor acts as an n-type intrinsic semiconductor, which is in good agreement with the experimental studies on Nb₂O₅-based memristor [26] [27]. It is found that the memristor persists in the LRS state even though the applied voltage reduces to zero, which shows the non-volatile memory property of the device. The SET and RESET voltages for the device are found to be around $V_{set} = 1.34$ V and $V_{reset} = -1.3$ V, respectively. The maximum switching currents for SET and RESET transitions are around $477 \mu A$ and $284 \mu A$, respectively. The memristor has a sneak current of around $72 \mu A$, a selectivity (S) of around 4.02 ($S = (I_{on})_{V_{read}} / (I_{off})_{V_{read}/2}$), and an on-off current ratio of around 1.55 for the $V/2$ biasing scheme [17]. Thus, the CF-based memristor has a lower selectivity or nonlinearity, and integration of the switching layer is much needed for a realistic crossbar array realization.

Figure 4. Switching characteristics for the voltage sweeps: (a) I-V characteristics of Pt/Ti/Nb₂O₅/Pt based memristor /memory switching device (MS), and (b) I-V characteristics of Pt/Ti/NbO₂/Nb₂O_{5-x}/Pt based self-selective memristor (MS+TS).

Fig. 4(b) shows the I-V characteristics of Pt/Ti/NbO₂/Nb₂O_{5-x}/Pt-based self-selective memristor. It is observed that as applied voltage increases, the current abruptly increases at $V_{th} = 1.54$ V for the SET side. When the applied voltage decreases below $V_{hold} = 1.13$ V, the current suddenly falls back to a low value. The self-selective memristor shows the same trend as observed for the TS device. The device exhibits identical SET and RESET characteristics with identical values for V_{th} and V_{hold} . The integration of NbO₂ switching layer with memristor offers a much smaller OFF-state current of around $0.31 \mu A$ compared to $84 \mu A$ for Pt/Ti/Nb₂O_{5-x}/Pt-based memristor. However, the drive current of the self-selective device is found to be around $1.57 \mu A$, which is considerably lower than that of $102 \mu A$ for threshold device. It is because the memristor layer resistance is limiting the drive current [28]. It is found that the self-selective device has a selectivity of 170, an on-off resistance of 4.79, and a sneak current of 310 nA. With this understanding, it becomes important to examine if a realistic crossbar array can be developed from the achieved nonlinearity in the self-selective memristor.

Figure 5. Crossbar layout and performance metrics: (a) crossbar array layout of self-selector memristor, (b) Readout margin as a function of crossbar array size for three different wire resistances simulated using Verilog-A model, and (c) Simulated power efficiency as a function of crossbar array size for three interconnect resistances.

A. Self-Selective Memristor Crossbar Array Operations

Fig. 5(a) shows the crossbar array with the Pt/Ti/NbO₂/Nb₂O_{5-x}/Pt-based self-selective memory cell. The writing operation in the crossbar array is performed using the V/2 biasing scheme. A pulse of $V_{read} = V_{th}$ is applied to read the memory state of a selected cell. Fig. 5(a) illustrates the reading operation in crossbar array. A net voltage of V_{read} appears on the selected cell, which is marked in blue color, while the partially selected cells in the same word line and bit line experience a voltage of $V_{read}/2$, which is marked in red color. The remaining unselected cells have a net-zero applied voltage. The partially biased cell with $V_{read}/2$ voltage is mainly responsible for the sneak-path current.

Fig. 5(b) shows the readout margin as a function of crossbar array size for three different inter-cell wire resistances. It is observed that the readout margin of crossbar array based on self-selective memristor significantly decreases with the increasing array size. At one kB array size (2^{10} bit capacity), the readout margin for self-selective memristor cell is around 14% for 10Ω wire resistance, which is near to the minimum (10%) defined limiting value [29]. The simulation results reveal that inter-cell wire resistance results in marginal degradation in readout margin with around $0.15\times$ smaller for a 10-fold increment. The degradation in readout margin with array size is because of the high sneak current and low on-off current ratio.

The impact of sneak current on power can be understood by comparing the write power in the selected and unselected cells. Fig. 5(c) shows the power efficiency (percentage power consumed in selected device out of total power consumption) as a function of array size for three different inter-cell wire resistances. It is observed that the power efficiency linearly decreases as array size increases. At four kB array size (2^{12} bit capacity), the power efficiency is around 27% for 0.1Ω wire resistance. Further, the power efficiency marginally decreases with the increasing wire resistance in the range of 0.1Ω to 10Ω. The readout margin and power efficiency suggest that achieving the crossbar array size larger than 64×64 is challenging with Pt/Ti/NbO₂/Nb₂O_{5-x}/Pt self-selective memory cell. To achieve a larger crossbar array size, we can further optimize the device for higher nonlinearity and on-off

resistance ratio; however, this could lead to a reduced drive current and thereby, enhance the switching issues. Therefore, to solve the issue of sneak current, we can focus on the optimization of the crossbar array architecture.

B. Split Crossbar Array Operation

Fig. 6 shows memristor-transistor split crossbar array architecture, which is constructed by breaking down a large-scale array into smaller array blocks. In this design, transistor switches in rows and columns isolate the small crossbar array units, called subarrays. It is observed from Fig. 6 that 16×16 crossbar array can be implemented by connecting 4 blocks of 4×4 subarrays and 32 transistor switches, while 1T-1M architecture requires 256 transistor switches, which could cost a significant chip area. The transistor switches are used to limit the sneak current within the subarray blocks. The read and write operations in the split crossbar array are performed in the same way as it was done for the simple crossbar array as in Fig. 5(a). The transistors in split crossbar are collectively or individually switched ON to isolate a particular subarray block.

Fig. 6(b) and (c) show the readout margin and power efficiency for the 64×64 split crossbar array implemented using 16×16 subarray, 32×32 subarray, and 64×64 subarray. The transistors in our design are considered to be in 180 nm technology node. The readout margins of split crossbar array is around 32%, 14%, 10% with 16×16 subarray, 32×32 subarray, and 64×64 subarray, respectively. Similarly, the power efficiencies is found to be around 33.6%, 27%, 10%. It is observed that a significantly smaller leakage current of 180 nm transistor has nearly suppressed the sneak current. The readout margin and power efficiency are better when the crossbar array is implemented using smaller subarrays because the transistor switches limits the sneak current-path within subarrays. It is observed from comparing Fig. 6(b) and 5(b) that the readout margin of split crossbar array is essentially equal to the readout margin of subarray. Thus, the selection of subarray size is crucial for the split crossbar, and the subarray block could govern the readout margin and power efficiency

Figure 6. Split memristor-transistor crossbar array architecture layout and performance metrics. (a) Split memristor-transistor crossbar array architecture with self-selector memristor memroy cell and MOSFET. (b) Readout margin and (c) power efficiency of 64×64 split crossbar array as a function of crossbar subarray size for three different wire resistances. (d) Readout margin and (e) power efficiency of split crossbar architecture, which is implemented using 16×16 subarray blocks, as a function of array size.

Table I
PERFORMANCE COMPARISON OF THE 64×64 MEMRISTIVE CROSSBAR
ARRAYS USING NIOBIUM OXIDE BASED MEMRISTOR.

Parameters	1-SM	1T-1M	Split Crossbar		
			4×4 sub- array	16×16 subarray	32×32 subarray
Area	$16,384 F^2$	$81,920 F^2$	$49,152 F^2$	$24,576 F^2$	$20,480 F^2$
Sneak Current	$1.05 \mu A$	$10.6 pA$	$88.4 nA$	$0.77 \mu A$	$0.95 \mu A$
Readout Margin	8.25	95.3	84.52	29.20	11.51
Power Efficiency	26.6	88.8	62.42	33.55	27.59

$F = 4\lambda$ is the minimum half-pitch.

of the array. However, the implementation of a crossbar array using smaller subarrays suffers a higher area penalty.

We have used 16×16 unit blocks to build the crossbar arrays of higher capacities. Fig. 6(d) and (e) show readout margin and power efficiency of split crossbar architecture implemented using 16×16 subarray blocks as a function of array size. The readout margin of the split crossbar array is not degraded considerably for array size greater than 16×16 . In a split crossbar array, the readout margin at any array size remains around 30%, equal to the readout margin of 16×16 subarray block. There is also an improvement in the power efficiency at larger array sizes, consistent with the containment of the sneak current within the smaller unit blocks. Therefore, the

split crossbar array allows large-scale crossbar array implementation by effectively eliminating the sneak current.

Table I benchmarks the performance of 64×64 crossbar array using self-selective memory cell, 1T-1M cell, and self-selective cell (1-SM) with split crossbar array using 4×4 subarray, 16×16 subarray and 32×32 subarray. The values for the 1T-1M crossbar array are calculated assuming 180 nm technology. It is found that split crossbar array using 4×4 subarray, 16×16 subarray, and 32×32 subarray decreases the area requirement by factors of 1.7, 3.3, 4, respectively when compared to the 64×64 crossbar array using 1T-1M cell. The split crossbar array implemented using 16×16 subarrays requires 512 transistor switches as compared to 4096 transistors for 64×64 crossbar array using 1T-1M cell. It is also observed that the advantage of split crossbar is a lower sneak current over a simple crossbar array. The results show that the readout margin of more than 20% is achieved for the crossbars consisting of 4, 16, 32 subarrays, which is better than the readout margin for the crossbar array implemented only using self-selective cells. As there is a direct correlation between sneak current and the readout margin, a decrease in the leakage results in an enhancement of readout margin for split crossbar array. Our proposed split crossbar array also offers a better power efficiency over a simple crossbar array. Therefore, a split crossbar architecture can be a more suitable candidate for constructing large-scale crossbar architecture with improved area overhead compared to a 1T-1M crossbar array, improved readout margin, and power efficiency compared to a 1M

Figure 7. Switching time for Pt/Ti/NbO₂/Nb₂O_{5-x}/Pt based self-selective memristor: current and voltage as a function of time for (a) SET transition, and (b) RESET transition.

crossbar array.

C. Writing Time for Self-Selective Memristor

Fig. 7 shows the SET and RESET transient response of Pt/Ti/NbO₂/Nb₂O_{5-x}/Pt based self-selective memristor for investigating the switching time modification from threshold layer integration. It is observed that, above V_{TH} , the self-selective device requires around 26 ns and 40 ns for SET and RESET transitions, respectively. The device responds instantaneously with the applied stimuli which is also observed in other experiments [30]. A significantly lower rise time shows that the selector quickly switches from insulating to the metallic phase. Thus, the integration of the NbO₂ selector with memristor layer does not significantly affect the operating speed of the memory.

IV. CONCLUSION

Using a multi-scale modeling approach, we have investigated the performance of niobium oxide-based self-selective memristor for crossbar array memory by analyzing the sneak current, readout margin, and power efficiency. We have found that integrating the NbO₂ selector layer with memristor enhanced nonlinearity and on-off current ratio and reduced the sneak current, but the device cannot meet the requirement for practical large-scale crossbar array implementation. The memristor-transistor split crossbar array, implemented using smaller subarrays and isolating the subarrays using transistors, restricts the sneak current path and allows subarray readout margin and power efficiency in large-scale crossbar array architecture. The split crossbar architecture provides an effective way for improving the reading accuracy and power efficiency for large-scale memory realization. Moreover, it reduces the chip area requirement over 1T-1M cells without affecting the crossbar array functionalities. Our split crossbar architecture with the self-selective memristor can enable the development of memory and logic-in-memory architectures for single step and parallel computation without affecting the speed of the memristor. Future studies should focus on the impact of memristor and transistor variability on the crossbar array performance.

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