Dynamic Offset Compensated Operational Amplifiers

This paper was downloaded from TechRxiv (<https://www.techrxiv.org>).

LICENSE

CC BY 4.0

SUBMISSION DATE / POSTED DATE

14-10-2021 / 29-10-2021

CITATION

Assim, Ara Abdulsatar Assim; Balashov, Evgenii (2021): Dynamic Offset Compensated Operational Amplifiers. TechRxiv. Preprint. <https://doi.org/10.36227/techrxiv.16810225.v1>

DOI

[10.36227/techrxiv.16810225.v1](https://doi.org/10.36227/techrxiv.16810225.v1)

Dynamic Offset Compensated Operational Amplifiers

Ara Abdulsatar Assim^{1,2}

Evgenii Balashov¹

¹ Peter the Great St. Petersburg Polytechnic University, St. Petersburg 195251, Russia

² University of Salahaddin, Erbil 44001, Iraq

Index-terms: Dynamic Offset Cancellation, Operational Amplifier, Auto-Zeroing, Chopping, CMOS.

Abstract

The given work is devoted to designing and implementing different dynamic offset cancellation techniques for 50 nm technology CMOS operational amplifiers. The goal is to minimize or get rid of the effects of the offset voltage. Offset voltage exists in all differential amplifiers due to the fact that no pair of transistors can be fabricated with the same size, there is always a slight difference in their dimensions (length or width), this gives rise to an undesirable effect called offset, the value of offset voltage for cheap commercial amplifiers are in the range of 1 to 10 mV, despite the fact that this isn't a significant value, due to the high gain of such amplifiers, this voltage is amplified by tens or hundreds of times, this results in clipping of the output signal and this further limits the amplifier's maximum allowable input voltage within the given dynamic range, hence its of great importance to take this small voltage into consideration, low-offset amplifiers find applications in mixers, analog to digital converters, instrumentation devices, etc. In this work, by using two different techniques for removing offset voltage (chopping and auto-zeroing), five low offset operational amplifiers were designed. The implemented methods reduced the flicker noise by more than 457 times (from 9.4 nV/ $\sqrt{\text{Hz}}$ to 20 pV/ $\sqrt{\text{Hz}}$) at 1 Hz. All the simulations were done using Cadence Virtuoso.

1. Offset cancellation techniques

Reducing offset voltage is the goal of this research, in this work different possible solutions are being considered to reduce its value to as minimum as possible. Low-offset operational amplifiers are widely used for different applications such as medical tests, industrial sensors, and measurement systems, in medicine they are used for amplifying signals coming from medical electrodes (wearable sensors) for performing EEG and ECG tests (fig. 1.1), in chemical industries they can be along with chemical sensors, hall-effect sensors, pressure sensors, and for sensing small currents in measurement systems [4, 5]. To minimize offset voltage, three methods are used, these are: trimming,

auto-zeroing, and chopping [5, 19-24]. at zero and low frequencies, offset, flicker noise and drift are the supreme fallacy sources in operational amplifiers. This is mainly applicable for op-amps designed with CMOS transistors.

Fig. 1.1. Using low offset op-amp with medical electrodes

The succeeding topics are concerned with reducing flicker noise and lower offset, before explaining these techniques in detail, it is necessary to have a fundamental understanding of these issues [18-24]. Offset voltage occurs due to random unpredictabilities during manufacturing the transistors. MOS transistors suffer from threshold voltage inconsistency since the threshold voltage is dependent on transistor's doping level and it is different for each transistor. Another common issue is mismatch between the transistors' lengths and widths. While flicker noise exists in lower frequencies, it is also known as (flicker or pink noise), this type of noise has a power spectral density of $1/f$, the point at which this noise reduces to thermal noise is referred to as corner frequency. It is generally caused by the imperfections in the joint between the gate's silicon dioxide and the semiconductor substrate [5, 18]. Flicker noise can be expressed as:

$$V_n = \sqrt{\frac{K}{WLC_{ox}f}} \quad (1.1)$$

where – K is a technology dependent constant; W – is the transistor's width; L is the transistor's length; f – is the frequency; C_{ox} is the gate-oxide capacitance.

Trimming method is implemented during fabrication of the transistors to reduce transistor mismatch, it may also be reduced if larger size transistors are used (as in fig. 1.2) but this is not an effective solution because larger transistors need more area [4], which will lead to a higher cost, thus Polysilicon-resistor films are commonly used in typical CMOS processes because they are widely available and possess a high sheet resistance [17, 18]. The laser-trimming apparatus is built from neodymium-doped yttrium-aluminum-garnet laser. The energy of the laser is soaked up by the pol-

ysilicon film, this leads to localized crystallization of the material, hence that allows a very accurate reduction of the resistivity of the interest zone [17]. It is possible to obtain very low offset voltages using trimming, but this method does not reduce the flicker noise, hence other techniques (chopping and auto-zeroing) are needed to prevent this problem, they also compensate offset changes gradually as the amplifier parameters change due to again and temperature changes.

Fig. 1.2. Offset voltage vs. channel length

Chopping is one of the major techniques used for offset elimination [2, 6-9, 18-24], it is favorable in applications where a continuous-time signal is needed, in contrast to auto-zeroing technique, chopper amplifier (fig. 1.3) does not cause noise-folding. This method is based on modulation in frequency domain. The principle of operation is that the voltage V_{in} goes through the chopper that is driven by a clock at frequency f_{ch} , hence it will be transformed to a pulse voltage [9, 18-20]. Later, the modulated signal will be amplified along with the input offset. The second chopper acts as a demodulator, it demodulates the input signal to a DC voltage, and at the concurrently modulates the offset to the odd harmonics of clock frequency that will be removed by a low-pass filter [11, 18-23]. This results in a signal with no offset and flicker noise, these two components now exist at higher frequency (which is equal to chopping frequency), fig. 1.4 and fig. 1.5 show these steps graphically in time and frequency domain, respectively.

Fig. 1.3. Chopper amplifier architecture

Fig. 1.4. Demonstrating chopping concept in time domain

Fig. 1.5. Demonstrating chopping concept in frequency domain

A chopper consists of four transistors, it is driven by two non-overlapping clock signals as shown in fig. 1.6:

Fig. 1.6. Chopper circuit

In the power spectrum density (PSD), both the offset voltage and the flicker noise are moved away to the chopper pulse frequency, as illustrated in fig. 1.7:

Fig. 1.7. PSD of an op-amp with and without chopping

Despite chopper amplifier's well performance in removing offset and flicker noise, charge injection gives rise to chopper ripple [5], various methods exist to eliminate it (refer to fig. 1.8). One way is

to use dummy switches that feed charge to the transistor switch, this in return gets rid of the existing charge. nonetheless, charge cannot be distributed equally between source and drain terminals, for that reason, this method is not very helpful. Another solution is using two transistors connected in parallel, this solution is handy with smaller input signals only, the last and most effective method is to use a fully differential circuit, this reduces the offset voltage by a factor of ten [5, 18].

Fig. 1.8. (a) using parallel transistors, (b) using a fully-differential circuit

Apart from chopping, another major technique exists, it is called auto-zeroing, it is widely used to reduce offset voltage, this method is based on a sampling (discrete-time). It samples the voltage offset of the amplifier in the first clock pulse, and then subtracts it from the input signal in the second clock pulse [8, 12-14, 18]. Three main topologies exist for auto-zeroing, which are: output offset storage, input offset storage and closed-loop offset cancellation with the help of a supplementary operational amplifier [18]. All the mentioned circuits use two non-overlapping clock signals (CK and $\overline{CK}$) that are out of phase by 180 degrees, in other words when CK is logic one, $\overline{CK}$ should be logic zero and vice-versa, if both are on at the same time even for a very short moment, both of the inputs of amplifier inputs will be shorted, that will lead to undesired effects. The easiest method to realize an auto-zeroing amplifier is to put a capacitor at the amplifier's output, as illustrated in fig. 1.9, C1 capacitor stores the offset in one clock phase and compensates it in the next phase. At the first phase the amplifier works in its normal amplification mode, in other words F1, S1 and S4 switches are on while S2 and S3 are off. In the next phase, the amplifier is working in compensation mode, switches S1, F2 and S4 are off while S2 and S3 are on. This method is sometimes referred to as open loop offset cancellation.

Fig. 1.9. Auto-zeroing scheme with output offset storage

There is a different auto-zeroing scheme that can be realized with input offset storage. Sometimes it is called closed loop offset cancellation. As in fig. 1.10, in the first half of each clock cycle S_4 , F_2 , and S_1 are open, but S_2 and S_3 are closed. in the second half, S_4 , F_2 , and S_1 are closed while S_2 and S_3 are open.

Fig. 1.10. Auto-zeroing scheme with input offset storage

As in chopper amplifiers, auto-zeroing compensated amplifiers suffer from charge injection, therefore an architecture with a supplementary amplifier has been designed to be used to reduce sensitivity to charge injection as shown in fig. 1.11. The amplifier operates in the following manner: during the first phase when F_1 is closed, the amplifier G_1 amplifies the input signal, in the succeeding phase, F_1 is open and F_2 causes the inputs of G_1 to be connected to each other, this results in an output current (I_1 due to input offset), the resulting current on I_1 creates a voltage on C_1 capacitor, the given capacitor supplies the supplementary amplifier G_2 , through that, offset compensation takes place.

Fig. 1.11. Auto-zeroing scheme with supplementary amplifier

As mentioned earlier, auto-zeroing compensated amplifiers are inappropriate to be used in continuous-time applications, because of that reason, a different architecture has been designed for that purpose, it is called ping-pong. Ping-pong amplifiers use two identical auto-zero amplifiers that are fed with two clock signals (180 degrees apart). The two amplifiers work parallelly (as depicted in fig. 1.12).

When the clock signal F1 is high and F2 is low, the amplifier G1 works in amplification mode while G3 is in compensating mode, during the next clock cycle (F1 is low and F2 is high), G3 amplifies the input signal while G1 compensates for offset, this will lead to a continuous signal existence at the output, thus convenient for continuous-signal applications, additionally, this drastically reduces the flicker noise [12]. The only disadvantage of that method is occurrence of voltage spikes due to switching at the output (V_{b1} and V_{b2}), it can be reduced by using active integrators instead of the capacitors [18]. An additional design exists (as shown in fig. 1.13) that solidly lessens chopper ripples, a combination of both auto-zeroing and chopping is used. That technique works because auto-zeroing reduces the ripples and the noise folding issue caused by auto-zeroing is solved by modulating to a larger frequency. A downside of that technique is reduction of signal to noise power because auto-zeroing's output is discrete.

2. Design of The Operational Amplifiers

The very first thing before attempting to reduce the offset is indeed implementing the operational amplifier, two operational amplifiers have to be designed (a typical single-output operational amplifier and a fully-differential operational amplifier), the single-output operational amplifier is used in auto-zeroing configurations, while the fully-differential operational amplifier is needed for the schemes that involve chopping, certain configurations may use two or more operational amplifiers,

in such case, the other operational amplifiers are referred to as, auxiliary or supplementary op-amps, they serve the main operational amplifier. In this part, the schematic diagram of both of the operational amplifiers, their transient analysis results, magnitude and phase responses are provided.

2.1. Schematic of a single-output operational amplifier

A standard three-stage operational amplifier topology is chosen here, the first stage is differential amplifier, the next stage is gain-stage (common-source) followed by the last stage which is a buffer, buffer is used when the amplifier is used to drive large resistive or capacitive loads which is required in practice (as depicted in fig. 2.1). Table 2.1 shows the transistor widths/lengths used in the op-amp and the biasing circuits. The design uses 50 nm CMOS technology, and the width of both transistors are quite large as in all analog circuits, while for the biasing circuit in fig. 2.1, two technologies are used which are 100 nm and 5u, different widths are used for 100 nm transistors.

Table 2.1 Sizes of the used transistors

Transistor-type	W/L
P-MOS	1u / 50n
N-MOS	0.5u / 50n

Fig. 2.1. A single-ended op-amp circuit

Like all op-amps, the given single-ended op-amp has two differential inputs, they are labeled as V_n and V_p , there is only one output which is V_{out} , the biasing circuit is shown as a symbol in fig. 2.1 and its circuit is provided in fig. 2.2. The biasing circuit produces a stable DC voltage of 353 mV that is fed to the amplifier through V_{bias} wire.

Fig. 2.2. The biasing circuit

For the sake of convenience and simplicity, the previous op-amp is now turned into a symbol, called (OP AMP) as depicted in fig. 2.3, at this point, the op-amp must be tested to ensure it operates properly, AC (magnitude and phase responses) and transient analyses are performed, the offset here is not considered ($V_{OS} = 0$). The amplifier is driven by two differential input sources with an amplitude of 250 mV, having a DC component of 500 mV and the frequency is 1 kHz, the differential inputs are generated by using two voltage-dependent voltage sources, one with a gain of 1 and the other with a gain of -1.

Fig. 2.3. Test bench scheme of the single-ended op-amp

The transient analysis result is presented in fig. 2.4 below, the purple signal is the differential input, and the red signal is the resulting output, the amplification is visible, if desired, gain can be increased by modifying the feedback and the input resistors.

Fig. 2.4. The differential input signal (purple) and the obtained output (red) for the single-ended op-amp circuit in figure 2.3.

It is also useful to know how the proposed operational amplifier behaves in frequency domain, the magnitude and phase responses have been measured (fig. 2.5 and fig. 2.6), bandwidth can be obtained from the magnitude response, typically the frequency at which the gain is 0 dB is the highest operating frequency, the given amplifier has a bandwidth of 47 MHz and a DC gain of 69.78 dB.

Fig. 2.5. Magnitude response of the single-ended op-amp

Additionally, the phase response of the given op-amp is provided in fig. 2.6:

Fig. 2.6. Phase response of the single-ended op-amp

2.2. Schematic of a fully-differential operational amplifier

As mentioned earlier, for certain offset cancellation techniques (such as chopping), a fully differential amplifier is used because more than one feedback path is needed, the schematic of this type of op-amp is provided in the following figures below (fig. 2.7, fig. 2.8 and fig. 2.9), due to its large size, the amplifier is broken into three parts (input stage, output stage and the feedback loop).

Fig. 2.7. Differential-input stage of the fully differential op-amp

The differential inputs are V_{inP} and V_{inN} , VCM is common-mode voltage, which is 500 mV in this case, the outputs of the first stage are given to the inputs of the later stages, they are labeled as (vodn and vodp).

Fig. 2.8. Output stage of the fully differential op-amp

The output stage is given in fig. 2.8., the differential outputs are VoutP and VoutN, in addition to that, negative feedback loop (fig. 2.9) is needed to ensure stability of the system and the bias circuit is the same as for the single-ended op-amp, thus it is not shown here.

Fig. 2.9. Feedback loop of the fully differential op-amp

Now the fully differential op-amp circuit may be tested (fig. 2.10) to make sure it works correctly before proceeding to using it in offset cancellation configurations, for convenience, as for the previous op-amp, the large schematic is represented as a symbol, called (Fully_Differential), the feedback resistors are chosen to have a gain value of 5 (can be easily calculated: $100 \text{ k}\Omega / 20 \text{ k}\Omega = 5$), the loads are two capacitors having a value of 250 fF.

Fig. 2.10. Test bench of the fully differential op-amp

The transient analysis result is provided in fig. 2.11, the red signal is the input (has a peak-to-peak value of 196 mV), while the blue signal is the output signal (with a peak-to-peak value of 966 mV). It may be concluded that the amplifier amplifies the signal correctly because $966/196 = 4.9$, which is very close to 5 (the ideally calculated gain value).

Fig. 2.11. Differential input (red) and output (blue) signals for the fully-differential op-amp

Likewise, magnitude and phase responses of the fully-differential amplifier has been measured and provided in fig. 2.12 and fig. 2.13, respectively.

Fig. 2.12. Magnitude response of the fully-differential op-amp

It can be seen that the fully-differential amplifier has a wider bandwidth, the bandwidth is 493 MHz, that is much larger in comparison with the previous op-amp but at the cost of its gain (47 dB) and its design complexity.

Fig. 2.13. Phase response of the fully-differential op-amp

At this stage, the two required operational amplifier schemes are realized, they are ready to be used in offset cancellation schemes, offset is added deliberately (modeled as a voltage source) and then offset reduction techniques are provided, the effect of adding offset voltage is demonstrated by using the test bench circuit illustrated in fig. 2.14.

Fig. 2.14. Modeling offset voltage

Fig. 2.14 above consists of two differential inputs (V_{plus} and V_{minus}), The capacitor with value of 250 fF acts as a load, offset is added to the positive input (as a DC voltage source of ± 50 mV), the effect of this small voltage is depicted in the following two figures (fig. 2.15 and fig. 2.16). Adding a positive offset voltage with a value of +50 mV causes clipping at the upper-peak (top) of the signal (blue signal in fig. 2.15).

Fig. 2.15. The effect of adding positive voltage offset

While adding a negative offset voltage with a value of -50 mV clips the lower-peak (bottom) of the signal (blue signal in fig. 2.16).

Fig. 2.16. The effect of adding negative voltage offset

3. Design of Op-Amps with Dynamic Offset Cancellation

Offset voltage is a dominant error source for operational amplifiers especially at low frequencies, as mentioned earlier, it occurs due to mismatch in transistor sizes, offset is a very vital parameter for operational amplifiers that is used in various applications for instance, calibrating signals, sensitive sensor interfaces, high accuracy instrumentation devices and many more. There are three major techniques that are commonly used to remove/reduce offset voltage, these are trimming, auto-zeroing, and chopping. Trimming is usually done during fabrication to eliminate offset by making sure the sizes of transistors match, it does not belong to the category of dynamic offset cancellation techniques, for that reason, this technique is mentioned only theoretically, and it is not realized in this work. Auto-zeroing's principle of operation is based on sampling, the offset voltage is captured in a phase (the value is kept on a capacitor with an opposite polarity) and then subtracted in next clock phases, while chopping operates based on continuous-time modulation, both the input signal

and offset voltage are modulated to a carrier signal with a much higher frequency than the input signal. Because the offset undergoes modulation, a ripple is observed at the amplifier's output. Both mentioned techniques are dynamic techniques that continuously reduce offset, they also reduce low frequency noise and offset drift as a function of temperature or time, in this part, the auto-zeroing and chopping methods are implemented practically with different architectures, these include ping-pong amplifier, auto-zeroing with supplementary amplifier and a combination of both chopping and auto-zeroing. their results are compared, and their PSS (periodic steady state) noise differences are summarized in a table, due to the existence of clock signals, normal input and output referred noises cannot be used for this category of circuits, hence, PSS noise is used for that purpose.

3.1. Auto-zeroing

A fundamental auto-zeroing amplifier is provided in fig. 3.1, the proposed amplifier operates in the following manner, when the input clock C1 is on (C2 is off), both of the Vn and Vp are shorted, the feedback loop is closed and the offset that appears at the output is fed back into the input, thus the capacitor (C0 - 5 nF) is charged to the offset voltage value, on the other cycle when C2 is on (C1 is off), the amplifier works as usual, meaning that the inputs are fed, at the same time the capacitor charge compensates the offset voltage because they are opposite in sign, this will result in zero offset voltage at the input.

Fig. 3.1. Auto-zeroing scheme

The clock signals mentioned earlier are shown in fig. 3.2, both signals have a duty-cycle of 50% and a frequency of 20 kHz, it is assumed they are ideal clock signals, non-idealities in the clock pulses such as clock-skew cause residual offsets.

Fig. 3.2. C1 and C2 clock signals used in the auto-zeroing circuits

Transient analysis may be run to observe the input and output signals, fig. 3.3 depicts the differential input signals (amplitude is 50 mV and DC component is 500 mV), possessing a frequency of 1 kHz.

Fig. 3.3. Differential input signals used in auto-zeroing amplifier

The output signal of the auto-zeroing amplifier (black signal) along with the differential inputs are provided in fig. 3.4, it can be observed that the signal is a sampled version of the amplified inputs, therefore it is not continuous but that is not an issue for this architecture, since it is not used for continuous-time applications. The visible spikes in the output signal can be eliminated using a low-pass filter (LPF).

Fig. 3.4. Output and input signals of the auto-zeroing amplifier in time-domain

A discontinuity exists at the beginning of the output signal, that is due to the capacitor C_0 , it takes some time to charge and start compensating (this duration is less than 350 μs) as shown in fig. 3.5, then the capacitor carries a value of -10 mV, because the fed offset is 10 mV.

Fig. 3.5. Capacitor C_0 charging to the desired voltage

Later on, the PSS analysis is executed to check that the auto-zeroing amplifier works properly, the PSS analysis can be done in both time domain and in frequency domain for noise calculation, time-domain PSS is provided in fig. 3.6, it is a replica of the output signal in transient analysis and that is a good indicator, from that we may conclude that the amplifier works correctly, in addition to that, it gives a clearer view of the output signal (because only two periods are shown here).

Fig. 3.6. PSS time-domain output signal

Moreover, a comparison of the output signal (blue signal) and the signal appearing on the capacitor C0 (red signal) is done to clearly see how offset voltage of 10 mV is removed (fig. 3.7).

Fig. 3.7. Comparison of output signal with the signal appearing on the capacitor C0

As mentioned previously, PSS analysis can be used to observe noise versus frequency, the result of such analysis is provided in fig. 3.8:

Fig. 3.8. PSS noise comparison for the AZ amplifier with (red signal) and without compensation (blue signal)

Running transient analysis simulation provides such signals (fig. 3.10), the output signal (black) looks quite similar to the output signal of the first auto-zeroing scheme but the difference in that case is, the compensation takes place almost immediately, that is because the capacitor here (fig. 3.11) charges much quicker than the previous case, despite increasing the circuit's complexity, using a supplementary amplifier is superior to using only one amplifier due to its better performance.

Fig. 3.10. Auto-zeroing with a supplementary amplifier's transient input and output signals

The voltage appearing on the capacitor in the given case comes with ripples (fig. 3.11), it is a DC voltage in the range of -10.0195 mV to -10.0145 mV, the variation is in range of 5 μ V, despite the fact, this is not a considerable amount, its noticeable and caused by charge injection.

Fig. 3.11. Voltage appearing on C0 capacitor in fig. 2.25

Habitually, the PSS noise analysis is done to see the noise level before and after compensation, the result is presented in fig. 3.12, the noise is reduced from 37.506 μ V/ $\sqrt{\text{Hz}}$ to 4.940 μ V/ $\sqrt{\text{Hz}}$, that is 158% better than the first AZ amplifier.

Fig. 3.12. PSS noise comparison for the AZ amplifier with a supplementary amplifier before compensation (blue signal) and after compensation (red signal)

3.3. Continuous-time auto-zeroing

The previous two auto-zeroing amplifiers were meant to be used in non-continuous applications, they are good in certain applications but should not be used when continuous-time signals are needed, as in voice amplifiers or analog-to-digital converters. A configuration exists that is commonly known as continuous-time auto-zeroing amplifier (CTAZ or ping-pong amplifier), it is a broad term that can be used for any amplifier that implements two identical sub-amplifiers with opposite clock pulses to achieve a continuous signal at the output. A realization of such amplifier is given in fig. 3.13. It's working principle can be summarized in two stages, the first stage when C2 is high (C1 is low), the upper amplifier receives the signal from the differential inputs, amplifies it and feeds it to the output (Vout), at this stage, the lower amplifier's inputs are shorted and it's in compensation mode, in the next stage, when C2 turns into low (C1 is high), the lower amplifier amplifies the signal while the upper amplifier compensates for offset and the output voltage is taken from the lower amplifier, this results in a continuous signal at all times at the output.

Fig. 3.13. Continuous-time auto-zeroing amplifier

The differential inputs and the output signal of the CTAZ amplifier in fig. 3.13 are presented in fig. 3.14, the black signal refers to the output, it is a continuous signal with a DC component of 500 mV, this shows that the offset of 10 mV at the input is removed, a proof that the amplifier is working flawlessly. The visible voltage spikes that can be easily resolved with a low-pass filter. The beginning of the output signal is distorted since the amplifier takes some time to start compensating.

Fig. 3.14. CTAZ's input and output signals

The PSS noise (refer to fig. 3.15) shows an incredible noise performance, the noise is lessened from $28.6967 \text{ uV}/\sqrt{\text{Hz}}$ to $62.8146 \text{ nV}/\sqrt{\text{Hz}}$.

Fig. 3.15. PSS noise comparison for the CTAZ amplifier before compensation (blue signal) and after compensation (red signal)

To remove the voltage spikes and other random high frequency components that are caused by switching operations, a Butterworth LPF is connected to the output of the CTAZ amplifier as illustrated in fig. 3.16, the filter's order is 7 with an input and output impedances equal to the CTAZ's feedback resistor value (100 k Ω). The corner frequency is equal to 8 kHz because the clock frequency is 20 kHz and the input signal is 1 kHz, the corner frequency should be higher than the input signal and less than the clock signal, so 8 kHz is a suitable value, picking a different value in the range of 2 kHz to 10 kHz does not result in a major difference.

Fig. 3.16. Adding a LPF to the CTAZ amplifier's output

The filter's output is shown in fig. 3.17 (black signal), the beginning of the signal is expectedly deformed because offset cancellation has not taken place yet, and the signal is not in phase with the inputs because a filter causes a time delay, in practice that does not cause any trouble, it can be fixed if desired with a phase-locked loop (PLL).

Fig. 3.17. CTMZ amplifier's filtered output

The discrete Fourier transform (DFT) of the output signal is taken in fig. 3.18 to observe the differences in frequency components of the output signal before and after offset compensation. The compensated signal which is colored in red has much less power along the entire frequency spectrum, that is particularly crucial in lower frequencies, the non-compensated signal has a power of -6.04 dB at 0 Hz, while the compensated signal lowered this value to -21.16 dB.

Fig. 3.18. DFT of the output signal with (red) and without compensation (blue)

3.4. Chopping

In contrast to auto-zeroing, chopping amplifier does not need any capacitor, it compensates offset voltage using modulation rather than charge compensation, a basic chopper amplifier is presented in fig. 3.19. It consists of two choppers, a fully differential operational amplifier, and a Butterworth low-pass filter. An offset of 10 mV is added as a DC voltage source.

Fig. 3.19. Chopper amplifier circuit

The block (Fully_Differential) amplifier is the same fully differential operational amplifier provided in section 2 (fig. 2.7. to fig. 2.9.), the chopper consists of four NMOS transistors, its configuration is as depicted in fig. 3.20:

Fig. 3.20. Chopper schematic

The chopper is driven by two clock frequencies of 20 kHz (C1 and C2 are out of phase by 180 degrees) they alternate between 1 V and -1 V as in fig. 3.21, as a rule, the clock frequency should be much higher than the frequency of the input signal. During one cycle “in1” is connected to “out1” and “in2” is connected to “out2”, during the other cycle, “in1” will be connected to “out2” and “in2” will be connected to “out1”.

Fig. 3.21. Clock signals used in chopper amplifier

The chopper amplifier is fed with two differential sinusoidal signals, with an amplitude of 100 mV, frequency of 1 kHz and a DC component of 500 mV as illustrated in fig. 3.22:

Fig. 3.22. Differential input signals fed to the chopper amplifier

The time-domain (transient analysis) results for the chopper amplifier circuit in fig. 3.19 without compensation is given in fig. 3.23, to turn off compensation, the C1 and C2 clocks may simply be replaced with a DC voltage source of 1 V and 0 V respectively, the effect of offset voltage (10 mV) is visible, the differential outputs' DC component is not 500 mV as supposed to be, the signals are displaced, the peak difference is now 10.6 mV (that is nearly equal to the imposed input offset voltage).

Fig. 3.23. Chopper amplifier's outputs without compensation

After observing the chopper amplifier's output before compensation, the offset compensation may be started by replacing C1 & C2 DC sources with clock signals, the first chopper acts as a modulator, it modulates the inputs to a larger frequency (in this case, its 20 kHz), the fully differential op-amp as usual amplifies the modulated signal and feeds it to the second chopper that acts as a demodulator, the output signals at this point (as shown in fig. 3.24) appear as a sampled signal due to switching, but in fact, it's a continuous signal.

Fig. 3.24. Chopper amplifier's output after offset compensation (before filtering)

By simply passing the outputs to a LPF, a continuous offset free signal can be obtained as in fig. 3.25:

Fig. 3.25. Chopper amplifier's output after offset compensation and filtering

The PSS noise analysis is not limited to be used in auto-zeroing amplifiers only, it can be used in chopper amplifiers as well, fig. 3.26 shows to what extent a chopper amplifier reduces noise, before compensation the noise was $84.764 \text{ uV}/\sqrt{\text{Hz}}$, while after compensation, this value went down to $1.127 \text{ uV}/\sqrt{\text{Hz}}$, in other words, after compensating for offset, the amplifier is 75 times less noisy.

Fig. 3.26. PSS noise comparison for the chopper amplifier before compensation (blue signal) and after compensation (red signal)

The DFT samples taken illustrated in fig. 3.27 further validates the point, output signal's power at 0 Hz is reduced from -37.29 dB to -45.23 dB.

Fig. 3.27. DFT samples of the chopper amplifier's output with compensation (red) and without compensation (blue)

3.5. A combination of chopping and auto-zeroing

A combination of both chopping and auto-zeroing can be used to achieve better noise performance, that is a more sophisticated configuration despite its complexity because auto-zeroing part gets rid of the voltage ripples caused by chopping, while chopping gets rid of the noise folding problem that is caused by auto-zeroing. An example of such system is provided in fig. 3.28.

Fig. 3.28. Schematic of an amplifier using both chopping and auto-zeroing

The circuit consists of two choppers, placed in the input and the output, and two auto-zeroing amplifiers (upper and lower) are used to achieve a continuous-time signal at the second chopper's input, its operation can be explained simply by the two-phase nonoverlapping clock signals (C1 and

C2). When C1 is one and C2 is zero, the upper auto-zeroing amplifier works in amplification mode while the lower auto-zeroing amplifier compensates the input offset of 10 mV, the feedback loop op-amp senses the voltage difference at the output of the main amplifier then the capacitors are charged to this value, later they are amplified and subtracted from main amplifier's output. In the next clock period (when C1 is zero and C2 is one), the system works in a similar manner, but this time the lower amplifier operates in amplification mode and the upper amplifier compensates the offset. This results in a continuous signal as provided in fig. 3.29, though visually it looks like a discrete signal due to sampling and modulation.

Fig. 3.29. Output voltage of an amplifier with chopping and auto-zeroing compensation

The voltage spikes and intermodulation products that are visible in fig. 3.29 can be taken out easily with a low-pass filter. The LPF's output is provided in fig. 3.30, it is a signal with removed offset voltage (the signal's DC component is 500 mV, that is the desired value, equal to the common-mode voltage). The circuit takes around of 765.1 us to initiate compensation of offset voltage.

Fig. 3.30. Filtered output voltage of an amplifier with chopping and auto-zeroing

Additionally, the used low-pass filter adds to that existing delay, as depicted in fig. 3.31, there is a time delay of 285.7 us, that is equivalent to a phase difference of 102.87 degrees between the filtered signal (black) and the unfiltered signal (red).

Fig. 3.31. Comparison of output signals of an amplifier using both chopping and auto-zeroing with (black) and without (red) low-pass filtering

The flicker noise reduction can be observed from the PSS noise analysis as portrayed in fig. 3.32, flicker noise is 405.811 $\mu\text{V}/\sqrt{\text{Hz}}$ without using any type of compensation, this value is reduced to 381.234 $\mu\text{V}/\sqrt{\text{Hz}}$ by using auto-zeroing only (choppers are turned off), however by enabling both choppers and auto-zeroing, the flicker noise is greatly reduced to 29.810 $\mu\text{V}/\sqrt{\text{Hz}}$ from 405.811 $\mu\text{V}/\sqrt{\text{Hz}}$, in other words, flicker noise is reduced approximately by 1361%.

Fig. 3.32. PSS noise comparison for the amplifier with auto-zeroing & chopping

Interestingly, the flicker noise reduction rate for an amplifier using both auto-zeroing & chopping is less than the CTAZ amplifier, that is because implementing an amplifier with a combination of both

auto-zeroing and chopping needs at least four times more transistors, and that naturally leads to an increase in the flicker noise.

3.6. Offset voltage reduction performance

In this section, the previously proposed operational amplifiers with dynamic offset voltage cancellation techniques are compared in terms of their offset voltage reduction performance (i.e., to what extent the offset voltage is reduced). The analysis can be done by measuring the output signal's maximum and minimum values, then their average value is taken which corresponds to the offset voltage level after compensation. Fig. 3.33 illustrates the auto-zeroing amplifier's output signal, the average of the peaks is equal to 500.041 mV, since the input signal's offset value (DC component) was 500 mV and the added offset was 10 mV, a difference of 0.041 mV exists, because the amplifier is unable to reduce it beyond that value (ideally to zero). In short, an offset voltage of 10 mV at the input was reduced to 0.041 mV at the output.

Fig. 3.33. Auto-zeroing amplifier's offset and peak voltages

Likewise, the measurements are done for an auto-zeroing amplifier with a supplementary amplifier, its offset reduction performance is better, because the new offset voltage value after compensation is 499.989 mV as depicted in fig. 3.34, this is 0.011 mV less than 500 mV (the desired offset value), comparing it with the previous auto-zeroing amplifier (fig.3.33), this amplifier reduces offset by 3.7 times more than the previous auto-zeroing amplifier.

Fig. 3.34. Auto-zeroing with a supplementary amplifier's offset and peak voltages

Furthermore, the output signal of a continuous-time auto-zeroing amplifier with its peaks and average is provided in fig. 3.35, this type of amplifier produces an offset of 499.954 mV, almost close to the ideal value of 500 mV, CTAZ amplifier performs better than the previously mentioned auto-zeroing amplifiers (fig. 3.33 & fig. 3.34).

Fig. 3.35. Continuous-time auto-zeroing amplifier's offset and peak voltages

Moreover, the same routine can be executed for the chopper amplifiers, the output signal of the chopper amplifier is given in fig. 3.36, the compensated output's offset value is 10.41 μ V, as expected, this value is much less than the offset voltages in all the auto-zeroing amplifiers, it can be noted that the offset does not contain the 500 mV component, because the output signal is taken from the chopper's differential outputs, in other words, the chopper's output signals are subtracted from each other ($V_{ch1} - V_{ch2}$), each of them possesses an offset voltage of 500 mV, thus it is removed.

Fig. 3.36. Chopper amplifier's offset and peak voltages

Lastly, fig. 3.37 presents the output signal of an operational amplifier that implements both techniques (chopping and auto-zeroing), the compensated signal's offset voltage is 0.01535 mV larger than the required offset voltage of 500 mV .

Fig. 3.37. Offset and peak voltages of an op-amp with both chopping and auto-zeroing

Its performance may be assessed as worse than continuous-time auto-zeroing amplifier but better than chopping and the other mentioned auto-zeroing amplifiers (in sections 3.1 and 3.2).

3.7. Input-referred voltage noise power spectral density comparison

All the PSS noise analyses done previously in sections (3.1 to 3.5) were done to measure output-referred noise power spectral density, but in order to have a more thorough understanding of the amplifiers' actual noise performance, input-referred noise PSD must be considered, as in data sheets. Input-referred noise PSD values are achieved by simply dividing the output-referred noise

PSD results by the gain (obtained from the amplifier's magnitude response). In this work, the single-ended amplifier has a gain of 69.78 dB, and the fully-differential amplifier has a gain of 47 dB, this converts to voltage gains equal to 3054.9 and 223.8, respectively. Fig. 3.38 provides the input-referred noise PSD measurement for the auto-zeroing amplifier in section 3.1, the flicker noise is reduced from 9.29 nV/ $\sqrt{\text{Hz}}$ to 2.53 nV/ $\sqrt{\text{Hz}}$, the flicker noise value is quite low, and it is comparable to commercial state of the art operational amplifiers.

Fig. 3.38. PSS input-referred noise PSD comparison for the basic auto-zeroing amplifier with (red signal) and without compensation (blue signal)

It is worth to mention that the ratio between the flicker noises before and after compensation is equal for input-referred noise PSD and output-referred PSD. The input-referred noise PSD for the op-amp (auto-zeroing with supplementary amplifier) in section 3.2 is given in fig. 3.39, the flicker noise is brought down from 12.153 nV/ $\sqrt{\text{Hz}}$ to 1.616 nV/ $\sqrt{\text{Hz}}$.

Fig. 3.39. PSS input-referred noise PSD comparison for the AZ amplifier with an auxiliary amplifier with (red signal) and without compensation (blue signal)

The continuous-time auto-zeroing amplifier has the lowest flicker noise among all the proposed amplifiers, the flicker noise is lessened from $9.396 \text{ nV}/\sqrt{\text{Hz}}$ to $20.56 \text{ pV}/\sqrt{\text{Hz}}$, in other words by 45684.5%, that is depicted in fig. 3.40.

Fig. 3.40. PSS input-referred noise PSD comparison for the CTAZ amplifier with (red signal) and without compensation (blue signal)

Moreover, input-referred noise PSD for the chopper amplifier is given in fig. 3.41, flicker noise is brought down from $337.176 \text{ nV}/\sqrt{\text{Hz}}$ to $4.49 \text{ nV}/\sqrt{\text{Hz}}$, this value is quite low, considering the fact that the amplifier has a very high bandwidth (493 MHz), and the compensation part of the schematic has a pretty simple and low cost configuration, it consists of only two choppers (8 transistors).

Fig. 3.41. PSS input-referred noise PSD comparison for the chopper amplifier with (red signal) and without compensation (blue signal)

Lastly, the same analysis is done for the most complicated scheme in section 3.5 (op-amp implementing both chopping and auto-zeroing techniques), fig. 3.42 shows that the flicker noise is 747

$\text{pV}/\sqrt{\text{Hz}}$ with no compensation, this is lowered to $54.87 \text{ pV}/\sqrt{\text{Hz}}$. In comparison with the previously mentioned four configurations, this comes in second place, because the flicker noise after compensation is still more than the flicker noise of the continuous-time auto-zeroing amplifier, nevertheless, that still makes this circuit useful due to its high bandwidth, low voltage ripples at the output and immunity to noise-folding problem.

Fig. 3.42. PSS input-referred noise PSD comparison for the amplifier with auto-zeroing & chopping

3.8. Thermal performance

Like all electronic circuits, the biasing circuit used in this work is affected by changes in temperature, fig. 3.43 depicts biasing current as a function of temperature. The biasing circuit can operate normally in the temperature range of -40°C to 85°C . The biasing current increases with an increase in temperature, higher temperatures lead to a decrease in the transistor threshold voltage and reduction in carrier mobility, this effect increases the drain current.

Fig. 3.43. Bias current versus temperature

Similarly, the bias voltage is also not immune to variations in temperature, fig. 3.44 shows bias voltage versus temperature, the voltage reduces at a rate of 0.597 mV/C, nevertheless, these changes do not cause op-amps to malfunction, heat sinks are used, and negative feedback keeps the amplifiers stable.

Fig. 3.44. Bias voltage versus temperature

Summary

All the proposed dynamic offset op-amps were simulated using PSS and transient analyses, the obtained results which include output-referred noise power spectrum density and offset voltage reduction performance of all the proposed dynamically compensated operational amplifiers are summarized in table 3.1, table 3.2, respectively.

Table 3.1 Output-referred noise PSD

Configuration	Output-referred noise PSD before compensation (uV/ $\sqrt{\text{Hz}}$)	Output-referred noise PSD after compensation (uV/ $\sqrt{\text{Hz}}$)	Reduction percentage (%)
Auto-zeroing (AZ)	28.696	7.821	366.89
AZ with supplementary amplifier	37.506	4.94	759.08
Continuous-time auto-zeroing	28.696	0.0628146	45684.76
Chopping	84.764	1.127	7514.98
Chopping & auto-zeroing	405.811	29.810	1361.29

Table 3.2 Input-referred offset voltage reduction rates

Configuration	Input offset voltage (uV)	Input-referred offset voltage after compensation (uV)	Reduction rate
Auto-zeroing (AZ)	10000	20.575	486.026
AZ with supplementary amplifier	10000	5.5	1818.181
Continuous-time auto-zeroing	10000	23	434.782
Chopping	10000	5.21	1919.385
Chopping & auto-zeroing	10000	7.675	1302.931

The input-referred noise PSD cannot be measured directly, it can be determined from the output-referred noise PSD, using the following formula:

$$S_{in} = \frac{S_{out}}{Module\ gain^2} \quad (3.1)$$

where S_{in} and S_{out} are the average power spectral density of noise voltage of the input and output respectively, $V^2/(\text{Hz})$; *Module gain* is the voltage gain of the op-amp, it is provided in table 3.3:

Table 3.3 Input-referred noise PSD

Configuration	Input-referred noise PSD before compensation (nV/ $\sqrt{\text{Hz}}$)	Input-referred noise PSD before compensation (nV/ $\sqrt{\text{Hz}}$)
Auto-zeroing (AZ)	9.299	2.534
AZ with supplementary amplifier	12.153	1.616
Continuous-time auto-zeroing	9.396	0.020568
Chopping	337.176	4.493
Chopping & auto-zeroing	0.747	0.054874

The thermal performance was considered in section 3.8, the op-amps function properly in the temperature range of -40 °C to 85 °C.

The power supply rejection ratio and the common-mode rejection ratio are provided in table 3.4, PSRR and CMRR can be obtained from these formulas:

$$PSRR = \frac{\Delta V_{DD}}{\Delta V_{OS}} \quad (3.2)$$

$$CMRR = \frac{\Delta V_{CM}}{\Delta V_{OS}} \quad (3.3)$$

where V_{CM} is the common-mode voltage; V_{OS} – is the offset voltage and V_{DD} – is the drain supply voltage.

Table 3.4 PSRR and CMRR for the proposed op-amps

Configuration	PSRR (dB)	CMRR (dB)
Auto-zeroing (AZ)	104.103	98.08
AZ with supplementary amplifier	115.563	109.54
Continuous-time auto-zeroing	103.135	97.115
Chopping	116.033	110.012
Chopping & auto-zeroing	112.668	106.648

Conclusion

In this work, a comparative analysis of CMOS operational amplifiers with dynamic offset cancellation was done. The results of this analysis showed that the dynamic offset cancellation techniques are an effective way to reduce the input offset voltage and its consequences such as flicker noise in operational amplifiers.

Two operational amplifiers were designed (single-output and fully-differential) in 50 nm CMOS technology, with a gain-bandwidth product (GBWP) of 47 MHz and 493 MHz, and an open-loop gain of 69.78 dB and 47 dB respectively, both of them have an operating voltage range of 1 V. The first configuration (basic auto-zeroing) reduced the offset voltage by only 486 times, while the best configuration which is chopping, reduced the offset voltage by approximately 1919 times.

The results of the input-referred noise power spectral density analysis of the proposed operational amplifiers show a flicker noise ranging from 20.57 pV/ $\sqrt{\text{Hz}}$ in the continuous-time auto-zeroing circuit to 4.5 nV/ $\sqrt{\text{Hz}}$ in basic auto-zeroing circuit at 1 Hz, that is a great reduction of flicker noise in comparison with the previously implemented designs. Chopping technique is better than autozeroing due to the fact, that it is a continuous-time modulation technique that does not produce noise folding and it is more power efficient. The chopper amplifier in this work reduced flicker noise by 75 times (from 337.1 nV/ $\sqrt{\text{Hz}}$ to 4.5 nV/ $\sqrt{\text{Hz}}$), using only 8 transistors for modulation and demodulation. But chopping has its cons, chopping induces ripples at the output. An advantage of auto-zeroing is that it does not induce ripple and its discrete property is well cooperative with switched-capacitor circuits. In brief, chopper amplifier and continuous-time auto-zeroing amplifier are reducing the flicker noise and input offset voltage more strongly, nonetheless, picking an operational amplifier for a specific application does not depend only on its flicker noise and offset voltage reduction capability. For instance, in continuous-time applications such as in analog-to-digital converters, continuous-time auto-zeroing must be used, while for amplifying a trigger signal from a sensor, a basic auto-zeroing amplifier can be used despite its humble qualities when compared to other more sophisticated amplifiers.

Acknowledgements

I would like to express my deep gratitude to my supervisor, Associate Professor (Balashov E. V.) in Peter the Great Saint Petersburg Polytechnic University for his guidance and help during the writing of this work. Additionally, my deepest appreciation goes to my parents for their endless love, encouragement, and support. I also thank my dearest friend (Nikolai Kirichenko) for helping me during my stay in Russia.

References

- [1] Baker. R. J. CMOS: Circuit Design, Layout, And Simulation. 3rd edition. IEEE PRESS, 2010. — P. 773-908.
- [2] Bortun. N., Stan. M. N., Brezeanu. G. High precision bidirectional chopper amplifier with extended common mode input voltage range // International Semiconductor Conference (CAS). — 2015. — P. 297-300.
- [3] Carusone. T. C., Johns. D. A., Martin. K. W. Analog Integrated Circuit Design. 2nd edition. Wiley, 2011. — P. 36, 242-293.
- [4] Duwe. M., Chen. T. Offset correction of low power, high precision op amp using digital assist for bio-medical applications // IEEE International Symposium on Circuits and Systems (ISCAS). — 2012. — P. 850-853.
- [5] Huijsing. J. Operational amplifiers theory and design. 2nd edition. Delft, Netherlands. Springer Science+Business Media B.V., 2011. — P. 351-412.
- [6] Ivanov. V., Shaik. M. A 10MHz-bandwidth 4 μ s-large-signal-settling 6.5nV/ $\sqrt{\text{Hz}}$ -noise 2 μ V-offset chopper operational amplifier // IEEE International Solid-State Circuits Conference (ISSCC). — 2016. — P. 88-89.
- [7] Kuang. X., Wang. T., Fan. F., The design of low noise chopper operational amplifier with inverter // IEEE 16th International Conference on Communication Technology (ICCT). — 2015. — P. 568-571.
- [8] Kusuda. Y. A 60 V Auto-Zero and Chopper Operational Amplifier With 800 KHz Interleaved Clocks and Input Bias Current Trimming // IEEE Journal of Solid-State Circuits. — 2015. — 50. N 12. — P. 2804-2813.
- [9] Mai. T., Schmid. K., Rober. J., Hagelauer. A., Weigel. R. A fully differential Operational Amplifier using a new Chopping Technique and Low-Voltage Input Devices // 24th IEEE International Conference on Electronics, Circuits and Systems. — 2017. — P. 74-77.
- [10] Paul. A. MOSFET // MATERIALPEDIA. — [Bangladesh, 2019]. — URL: <https://materialpedia.materialscience.net/2019/03/18/mosfet> — (Date of access: 31.01.2021).
- [11] Pipino. A., Pezzotta. A., Resta. F., De Matteis. M., Baschiroto. A. A rail-to-rail-input chopper instrumentation amplifier in 28nm CMOS // IEEE International Conference on Electronics, Circuits, and Systems (ICECS). — 2015. — P. 73-76.
- [12] Prokop. R. Dynamic input offset auto-compensation of continuously working Opamp // 36th International Conference on Telecommunications and Signal Processing (TSP). — 2013. — P. 440-443.
- [13] Prokop. R., Novak. P., Musil. V. Bulk Driven Offset Compensation for Continuous Time Opamp Operation // Proceedings of the Fifteenth International Scientific and Applied Science Conference. — 2006. — P. 26-29.
- [14] Raghuveer. V., Balasubramanian. K., Sudhakar. S. A 2 μ V low offset, 130 dB high gain continuous auto zero operational amplifier // International Conference on Communication and Signal Processing (ICCSP). — 2017.
- [15] Razavi. B. Fundamentals of Microelectronics. 2nd edition. Wiley, 2013. — P. 354-388.
- [16] Shukla. G., Srivastava. N., Shadab. A. DC offset voltage reduction in cascaded instrumentation amplifier // 2013 Students Conference on Engineering and Systems (SCES). — 2013. — P. 1-5.

- [17] Singh. R., Audet. Y., Gagnon. Y., Savaria. Y., Boulais. É., Meunier. M. A Laser-Trimmed Rail-to-Rail Precision CMOS Operational Amplifier // IEEE Transactions on Circuits and Systems II: Express Briefs. — 2011. — 58. N 2. — P. 75–79.
- [18] Wu. R., Huijsin. J. H., Makinwa. K. A. A. Precision Instrumentation Amplifiers and Read-Out Integrated Circuits. New York. Springer, 2013. — P. 21-48.
- [19] Xu. J., Nguyen. A. T., Luu. D. K., Drealan. M., Yang. Z. Noise Optimization Techniques for Switched-Capacitor Based Neural Interfaces // IEEE Transactions on Biomedical Circuits and Systems. — 2020. — 14. N 5. — P. 1024-1035.
- [20] Yang. X., Yang. J., Lin. L., Ling. C. Low-power low-noise CMOS chopper amplifier // 2010 International Conference on Anti-Counterfeiting, Security and Identification. — 2010. — P. 83–84.
- [21] Yeh. C., Huang. J., Wu. P., Tsai H., Juang. Y. A low power and low noise CMOS chopper amplifier for use in capacitive type accelerometer // 2016 IEEE Asia Pacific Conference on Circuits and Systems (APC-CAS). — 2016. — P. 642-645.
- [22] Yong. X., Fei. Z., Zheng. S., Yuanliang. W. Design of novel chopper stabilized rail-to-rail operational amplifier // 2015 IEEE 11th International Conference on ASIC (ASICON). — 2015. — P. 1-4.
- [23] Zhong. X., Bermak. A., Tsui. C. A low-offset dynamic comparator with area-efficient and low-power offset cancellation // 2017 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC). — 2017. — P. 1-6.
- [24] Zhou. Y., Zhao. M., Dong. Y., Wu. X., Tang. L. A Low-Power Low-Noise Biomedical Instrumentation Amplifier Using Novel Ripple-Reduction Technique // 2018 IEEE Biomedical Circuits and Systems Conference (BioCAS). — 2018. — P. 1-4.