Fast Hierarchical Optimization Method for High Speed Channel Design Using Channel Operating Margin (COM)

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Abstract

This paper proposes a design flow for channel design by a fast hierarchical optimization method based on Channel Operating Margin (COM). Unlike the common design of experiment (DOE), the method performs the design by a hierarchical flow in the level of electrical characteristic while not the usual horizontal structure of physical parameters. It significantly reduces the number of huge samples used in DOE, and thus is able to offer a fast estimation approach for channel in the early design period. In each stage of the vertical flow, the electrical properties of component are extracted by 2.5D or 3D full wave simulator, and thus ensure the accuracy of the channel design. Design strategy for the most crucial discontinuity, Via, to achieve an impedance matching is addressed. Package effect on the COM is also discussed as a reference for adjusting the 3dB criterion of COM in the future.

Introduction

The state of the art of semiconductor technology pursues continuous improvement on the performance including the higher data rate, larger density, and more complicated interconnect in high speed channel. Design of high speed channel is very challenging in multi-giga data rate products since the parasitic effects, which could be neglected before, start to play non-negligible roles in deteriorating signal quality launched in PCB interconnects [1]. A bunch of criteria, such as insertion loss, return loss, insertion loss deviation, insertion loss to crosstalk ratio, etc., to determine the quality of channel have been widely used for data rate below 25Gbps. Turing into an era with higher data rate above 25Gbps, those separate masks are not able to be all satisfied at the same time. Therefore, a budgeting method among all masks with a simple criterion is demanded to be proposed to offer a solution.

Channel Operating Margin (COM) method has been introduced for providing a figure of merit (FOM) as a channel performance evaluation flow [2], and defined by IEEE Std 802.3bjTM-2014 as normative means to judge the performance of a passive high speed electrical channel [3]. With data rate over 25Gbps, traditional 2 levels Non-Return to Zero (NRZ) modulation cannot handle the large loss in the Nyquist frequency. Now the industry is turning its attention to next-generation transceivers using 4-level pulse amplitude modulation (PAM4) to support up to 56 Gbps or 112G bps per lane, and COM analysis for 56Gbps PAM chip to chip and backplane interfaces were demonstrated [4]. We can conclude that existing protocols are embracing COM, and COM will clearly evolve to support future protocols.

The COM definitely offers a way to guide the design of interconnection, and it would be used to locate the best performance of the channel, which includes transmitter, receiver, multilayer PCB, cable and connectors. The conventional optimization in a channel design depends on the sweeping of possible physical parameters in each component, and to select the combination of all parameters for the best performance under condition of specific criteria. It might be based on One Factor at a Time (OFAT) approach or the way like the fractional factorial Design of Experiment (DOE) method as introduced in [5]. They also brought in an Artificial Neural Network (ANN) there to increase the accuracy of the design. The OFAT has drawbacks that only a narrow factor space is considered and the interaction between factors is neglected. DOE liked sweeping approach costs substantial amount of computational time and iterations for the numerous combinations of the physical parameters in channel. Time to market and competitive differentiation pressures for chip and board designer probably would not allow it to be accepted. The implementation of ANN accelerates the speed of the iteration while it requires large enough input data for training to ensure the accuracy. Thus it is not suitable in the early stage of channel design.

This paper proposes a fast hierarchical optimization method for high speed channel design using COM. The COM was mostly used to determine the quality in the compliance simulation or test stage after the channel design, and there is no existing design guide for channel based on COM. The significant contribution of this paper is that

we firstly propose a fast and accurate design flow for high speed channel design based on the merit of COM. Unlike the common optimization approaches, the method performs the design based on COM by a progressive structure from the level of electrical characteristic to level of physical parameters while not like the conventional way which only stays in physical parameters level. It significantly reduces the number of huge samples used in DOE since one factor in electrical level contains information of various factors in physical level. Thus it is able to offer a fast estimation approach for channel in the early design period. Moreover, in each stage of the vertical flow, the characteristic extraction of each component is performed by the full-wave 3D simulator while not the common 2D simulator for channel DOE, and absolutely can ensure the accuracy. In this paper, design of channel for data rate over 25Gbps would be demonstrated in detail with addressing on impedance matching strategy for the most crucial discontinuity, Via.

1. An Overview of Channel Operating Margin

For those who are unfamiliar with the definition of COM, this section would provide an overview of the method for helping them understand the implementation of COM and corresponding results in our proposed fast optimization algorithm in the later section of this paper.

COM is defined by by IEEE Std 802.3bjTM-2014 as a figure of merit to determine if the quality of channel satisfy the requirement by the compliant transceiver. It describes a ratio of available signal amplitude to statistical noise amplitude as in

$$\text{COM} = 20 * \log_{10} \left(\frac{A_s}{A_n} \right) \quad (1)$$

Fig. 1. Flow chart for a Channel Operating Margin calculation [3].

The flow chart to calculate the COM in detail is introduced in [3] and depicted in Fig. 1. Calculation of COM starts with the characteristics of channel; here S-parameter is defined to represent it. Detail steps for the computation are described as the following steps and in Fig. 2:

1. Transfer function extraction for channel (S-parameter Tx to Rx);
2. Conversion from frequency domain to time domain for Single bit response;
3. Determine equalization configuration to make maximum FOM and obtain the amplitude of available signal;
4. Define channel interference, jitter and other noise to get amplitude of statistical noise;
5. To achieve COM based on (1).

Fig. 2. The computation process for channel operating margin.

2. Conventional Optimization Methods by COM

COM offers a convenient approach to guide the channel design and also provides criteria as FOM to judge the quality of channel. In contrast to the traditional masks as eye height and eye width, COM has an obvious merit as the time reduction on simulation time.

Various optimization methods have been proposed for high-speed SerDes channel design using COM metric. Recently, a comparison of the pros and cons for Design of Experiments (DOE), Response Surface Method (RSM), and Artificial Neural Networks (ANN) was introduced in [5]. In all the methods mentioned above, the factors were the physical parameters of channel such as material, channel length, via size, etc.

The DOE method with implementation of RSM and ANN is much better than the simple one factor at a time (OFAT) experiment since only one factor is changed in each experiment in OFAT way. It cannot consider the mutual effects between factors while DOE can include the interaction between factors, and thus solve the issue well with a larger region of the variable space.

In the mentioned DOE, the RSM is realized by a regression model of the self and mutual effects caused by physical parameters. The RSM explores the relationships between several explanatory variables and one or more response variables. Response distribution is generated based on operational factors, and is used to find the best set to satisfy the DOE designs. The disadvantage is that RSM method is accurate for 1st or 2nd order designs (max three levels), but it might be inaccurate for higher order designs [5]. An alternative method called ANN as illustrated in Fig. 3 was proposed to handle the insufficient accuracy of RSM for non-linear and higher order responses. A wide range of physical parameters of components in channel are used as the input data to train the nonlinear functions as neurons in the hidden layer, and the generated outputs are the result of COM values. The accuracy of the ANN is able to be improved with increasing number of trainings, thus it would be a quite useful tool in the DOE for high speed channel design. However, large enough output data of COM with corresponding physical parameters as inputs to ensure a required accuracy is not possible to be obtained in the early design stage of channel. Therefore, a fast method with acceptable accuracy based on COM for channel DOE is demanded in the early design stage.

Fig. 3. A typical Artificial Neural Network used in DOE.

3. Proposed Design Flow by the Fast Hierarchical Optimization Method

The proposed fast hierarchical optimization COM method for high speed channel design performs the design by a vertical flow in the level of electrical characteristic while not the usual horizontal structure of physical parameters. Since the characteristics of physical parameters for a passive component such as transmission line, via or a cable can be represented by a single factor as impedance, the key enhancement of our method to the traditional optimization way based on COM is to take the impedance as the variable in the most top level, and then figure out the corresponding physical parameters in lower levels. By changing a multiply operation of huge physical variables only in one level to a summation of relative smaller variables with diverse characteristics (electrical and physical) in multiple levels, the simulation cases and time can be significantly reduced. It is able to lead to an efficient design in the early development stage of high speed channel, and also shrink the time of product to market. The flow of the proposed method is illustrated as in Fig. 4 detail.

Fig. 4. Flow chart for proposed hierarchical optimization method using COM.

As the COM is a hot topic for the channel design of 100G, 200G and 400G network, in the system-level optimization, we take the high speed long-reach (LR) channel as our target to demonstrate the proposed method. The typical LR channel was defined in OIF CEI interfaces as depicted in Fig. 5, and contains one backplane, and two line cards with Tx and Rx above separately [6]. Components such as stackup and material of PCB, transmission lines, via and connectors are the main design targets for the backplane and line cards.

Fig. 5. Configuration of long reach channel defined by OIE-CEI.

The optimization starts on the top level with three layers of the channel, and they are line card layer A, backplane layer C and line card layer B as shown as the design process of the method in Fig. 6. In high speed channel design, although we have the target impedance of 50 ohm for single-ended case and 100 ohm for differential one, the best performance of channel may not be achieved by the target one. Usually, the real impedance has a bias but is close to the target one. Hence, each layer in our flow is represented by its own impedance with 10% variance from the target impedance.

Fig. 6. Design process of 56G LR channel based on the proposed fast COM method.

In the beginning stage of the optimization, a COM based on the impedance sweeping helps us obtain the demanded value for each layer by means of operations in the first block. After figuring out the appropriate impedance of each layer, the single impedance per layer was expanded to impedance of components in each layer in the channel model to describe the characteristics of via, stripline and connector. Taking the same operating

did in the first block, the proper impedance for each component with best COM value is able to be derived. Since the conventional 2D channel simulator cannot handle the modeling of structures which has not uniform distribution in vertical axis as Via or connector, in the final block, we execute the extraction in 3D full wave commercial extractor to enhance the accuracy for calculating the physical parameters (pad and anti-pad size for via, width, gap of differential pair for transmission line, etc.) based on determined impedance.

The consumed iterations for traditional horizontal optimization and our proposed hierarchical method for the mentioned LR channel are described in Fig. 7 and Fig. 8. A comparison of the iteration and accuracy using COM happened in those two methods is shown in Fig. 9. The COM describes the return/insertion loss, crosstalk, jitter, impedance mismatching and other characteristics of channel, thus the quality of COM is affected by every component from transmitter to receiver. To capture the interactive effects among components, the COM analysis for components should not be considered as a separate function, the conventional needs a huge number of calculations to include all the combinations of components at one time. In other word, it should be a multiplication to include all the factors of components if we take a horizontal optimization way. The characteristic of impedance provides us a possible solution to overcome the burdened multiplication because the impedance is a set to describe the interactions of various physical parameters.

From the comparison, the iterations are obviously decreased to a profound grade in the proposed process, and keep a better accuracy to the conventional way. The significant merit of the proposed method is that the hierarchical analysis flow based on the collective value of impedance in electrical level can narrow the range of variables in each stage by a top-down characteristic.

Simulation Times Required by Conventional Horizontal Optimization							
	Via_layerA	Trace_layer A	Via_layerB	Trace_layerB	Connector_layerC	Via_layerC	Trace_layerC
Variables (Physical Parameters)	2 (Pad & Antipad)	2 (Trace Width & gap of diff. lines)	2 (Pad & Antipad)	2 (Trace Width & gap of diff. lines)	1 (Impedance)	2 (Pad & Antipad)	2 (Trace Width & gap of diff. lines)
Sweep variables in a $\pm 10\%$ range (At least 5 set-5% as step to ensure accuracy)	10	10	10	10	10	10	10
Total Simulation Times:	$2^6 * 10^7$						

Fig. 7. Iterations cost in conventional horizontal optimization approach.

Fig. 8. Iterations cost in proposed hierarchical optimization method.

Comparison of Iterations and Accuracy of Different Methods		
Opt. method	Conventional (Physical Parameters based)	Proposed (Hierarchy)
Loop Sweeping	$2^6 * 10^7$	13064
Estimated Time Cost (Avg. 5 min. for each COM calculation of 56G)	74074 Months	1.512 Months
TAT reduction	$(1 - 1.512/74074) * 100\% = 99.9979\%$	
Accuracy	Normal (2D Channel Designer)	High (Enhanced by 2.5D/3D simulator)

Fig. 9. Comparison of iterations and accuracy of different methods

4. Design Strategy of Via in High Speed Channel

4.1. Fluctuation of Impedance caused by characteristics of via

Via is the most common discontinuity in passive channel and is widely used as the transition for traces to switch layers. It is also applied to offer a connection between power and ground planes in active devices. Especially in the high speed channel with data rate up to multi-giga bits per second, amateur design of the discontinuity may cause unwanted loss, reflection, noise and even serious signal/power integrity as well as electromagnetic interference (EMI) issues. Therefore, after extracting the impedance of via and calculating the approximate physical parameters of via by its impedance in 2D

modeling tool, the design strategy for obtaining a SI/PI and EMI compliant via based on 3D modeling technique has vital meaning to the performance of high speed channel.

The basic factors of a typical via are via barrel, via pad and anti-pad as shown in Fig. 10. High speed signal on strip line under the top pad of via is easy to be exposed to external environment and gets interfered by the radio frequency (RF) components around. The safe design is to make sure there is a shielding layer above the line at via area, and locates via far from any wireless components. The more important phenomenon is the coupling through the dielectric material between two vertical vias. To minimize the crosstalk between two vias carrying high speed signals, the fence established by ground vias near every signal via can be used and it works well with mitigating the crosstalk as also depicted in Fig. 10.

Fig. 10. Structure of via in high speed channel.

In the typical via structure, via barrel acts as a vertical signal switching in different layers and contributes most of the resistive loss and inductance of vias. Capacitive effect is usually seen at the pad generated by the coupling between pad and nearby ground. Anti-pad is used to isolate via barrel and those planes which are not wanted to be connected with via. An impedance of via is able to be obtained by Time-domain Reflectometry (TDR). A fluctuation happened in impedance of via is caused by the parasitic inductive and capacitive effects of specific parts in via as represented in the lower right part of Fig. 11. Fan in/out trace connecting with via inevitably generates an inductive change on the flat impedance since there are anti-pads and no return paths right below or above the trace in the transition area between transmission line and via. The pad of via which plays a role of platform for signal switching between vertical and horizontal directions, has a capacitive effect due to the couplings in the gap filled with dielectric material to nearby ground. Vertical inductive coupling comes from the barrel as we mentioned above.

Therefore, the effects of each portion in via on the impedance is clearly demonstrated and shown in the upper side of Fig. 11.

Fig. 11. Impedance variation caused by the inductive and capacitive parts of via.

4.2 Strategy to Mitigate the Variance on Impedance

The variance on impedance of via definitely deteriorates the quality of high speed signal propagation in channel. To mitigate the fluctuation of impedance caused by the inductive and capacitive couplings, actions in detail should be taken by looking at each stage of via. The barrel of via is determined by the switching layers, and is usually fixed with almost no margin to change. Our strategy to weaken the variance on impedance mainly focuses on the other four stages as in Fig. 11, and realized by our proposed three solutions as shown in Fig. 12. The transition coupled area working as capacitance compensation can effectively restrain the first inductive leap caused by the absence of the near return path for the transmission line connecting to via. The size adjustment of anti-pad avoids the excessive capacitive coupling between pad and adjacent grounds. Most of the capacitive effect comes from the pads at the two outer terminals linking with transmission lines, and the internal non-functional pads contributed much less. Therefore, the diameters of anti-pads are diverse and distribution of anti-pads is not uniform. For getting an appropriate control on the capacitive resonance by pad of via, anti-pads at two terminals is designed with larger diameters on purpose, and leaves a relative smaller anti-pad for the internal non-functional pads. Since anti-pad is only able to reduce the horizontal capacitance of pads, usually the thickness of dielectric material around pad is even less than the gap of anti-pad, the vertical capacitive couplings between pad and grounds at above or below layer would generate more capacitance. A defected structure on the adjacent ground

layers vertically to the pad is used here to handle the redundant vertical capacitance and it is a flexible solution with a changeable shapes and sizes of the defected structure. The final stable impedance with implementing our proposed strategy is achieved as the red waveform in Fig. 13 with isolated solution to the coupling happened of each section of via.

Fig. 12. Proposed solution to mitigate the fluctuation on impedance of via.

Fig. 13. Effect of the proposed structures on stabilizing impedance.

Three compensated capacitance structures for impedance control of via are proposed as depicted in Fig. 14, and they are shapes of bump, closer line and interdigital capacitance. Implementation of specific shape is determined by the demanded amplitude of compensated capacitance and the available space in real via design. Here we take the bump shape as a study case to demonstrate the influence of the geometrical parameters on the capacitive couplings.

Fig. 14. Proposed capacitance compensation structure for impedance control of via.

To figure out the effect of shape on the capacitive compensated bump structure, we designed a bunch of coupled bumps with diverse sizes and locations. For a future comparison with measurement, via is designed as the structure in Fig. 13 with a narrow tail for probing pads. Since the anti-pad and defected ground structure is fixed in those cases, only the impact of capacitance compensation area is discussed. Five representative cases among all of them are chosen to demonstrate the impact on the impedance of via as shown in Fig. 15. A proper value of the shape depends on the width, height and location of the coupled areas, and it is also determined on the gap between inductance peak as the mark m1 in Fig. 15 and the target impedance which is 85 ohm in our design. The location of compensation area slightly influences on the impedance and dominates the horizontal location of capacitive coupling in time domain. Width and height of the bump change the amplitude of impedance by generating diverse additional capacitances. The appropriate w_1 and h_1 are chosen to achieve an impedance of 86.292 ohm of via to match the target impedance 85 ohm. The obvious second and third inductive peaks after the transition area without return path are caused by the inductance of via barrel and another smaller transition area connecting the probing pads. By applying the compensated capacitive coupling area, the inductive peak is able to be counteracted, and stable impedance occurs. Furthermore, the compensated area does not bring a bad side effect on the loss of via as we can find in Fig. 16. A negligible variance of insertion loss for via without and with diverse compensated bumps lasts until 40GHz. Considering the Nyquist frequency of 25Gbps/56Gbps/112Gbps with PAM4 modulation, the implementation of compensated area can achieve a mitigation on impedance fluctuation but not bring in a large loss into channel.

Fig. 15. Impact of diverse factors in capacitance compensation bump area on impedance of via.

Fig. 16. Comparison of insertion loss for the structure without and with diverse compensated bumps.

The caused fluctuation by the differential vias also affects the eye performance. A channel of 17 cm with 3 differential via pairs is established to discuss the phenomena. The target impedance of channel is 45 ohm, and two kinds of differential vias are designed, which are not optimized vias with 12.6% fluctuation on the impedance with reference to 45 ohm and optimized vias with fluctuation on the impedance reduced to 2.4%. Even in TDR analysis, there is 10% difference for the fluctuation of via impedance, more than 20% bias happened on eye height and 10% variation is caused to eye width in the 56Gbps PAM4 modulation. The reason to amplify the disadvantage of the fluctuation is the multiple reflections on each transition between trace and via with unmatched impedance.

Figure 17. Eye performance at BER=1e-4 for channel with diverse via fluctuations.
Upper (Via with fluctuated impedance): fluctuation of via=12.6%;
Lower (Via with matched impedance) : fluctuation of via=2.4%;

Table 1. Effect of via impedance on the eye performance of entire channel.

BER=1e-4	Eye Height (V)	Eye Width (ps)
Via impedance fluctuation: 12.6%	0.028633	8.28559
Via impedance fluctuation: 2.4%	0.0364164	9.24427
Variation	27.18%	11.57%

5. Channel Operating Margin Analysis for Designed Channel

Entire channel is designed based on both the 2.5D and 3D simulators. The 2.5D extractor is used for those components have the same distribution in vertical direction as strip and microstrip lines, and 3D full wave extractor can handle the complicated structures that have not uniform distribution in vertical plane such as via.

Two channels with different insertion loss and crosstalk levels are design to demonstrate the effect of loss and crosstalk on the channel operating margin. Channel 1 has more insertion loss at Nyquist frequency of 14GHz but less power sum RMS value for crosstalk and channel 2 is designed with a less insertion loss to channel1 but with a worse condition of crosstalk. Four lanes exist in the two channels and thus 3 far-end crosstalk and 4 near-end crosstalk are extracted in the calculation of COM value. Insertion loss and and crosstalk for channel 1 and channel 2 are illustrated in Fig. 18 and Fig. 19, separately. Since the channel is defined by IEEE 802.3 specification as a path from ball of Tx to ball of Rx, in Fig. 18 and Fig. 19, the characteristic of package is not included.

Fig. 18. Insertion loss and crosstalk for designed channel 1 from ball to ball.

Fig. 19. Insertion loss and crosstalk for designed channel 2 from ball to ball.

Although package is regarded as a part of chip, and not included in the range of channel, the package more or less takes into effect on the channel operating margin and performance of SerDes system. In IEEE 802.3 100G Ethernet specification, the package model was described as a transmission line with a device capacitance C_d and a board capacitance C_p as well as a termination resistance. In our most current pre-settings for COM extraction defined in the IEEE 802.3 taskforce, those parameters are shown in Table 2.

Table 2: Definition of parameters for the package model used in COM extraction.

Parameter	Definition	Setting	Units
C_d	Single-ended device capacitance	[1.8e-4 1.8e-4]	nF
z_p select	Test cases of package model	[1 2]	Test case
z_p (TX)	Victim transmitter package trace lengths	[12 30]	mm
z_p (NEXT)	NEXT aggressor transmitter package trace lengths	[12 12]	mm
z_p (FEXT)	FEXT aggressor transmitter package trace lengths	[12 30]	mm
z_p (RX)	Victim receiver package trace lengths	[12 30]	mm
C_p	Single-ended package-to-board capacitance	[1.1e-4 1.1e-4]	nF
R_0	Reference single-ended impedance	50	Ohm
R_d	Single-ended termination resistance	[55 55]	Ohm

It seems the termination of package is fixed and the crosstalk inside package was not included as a consideration for the COM. Actually, the crosstalk happens at the bump of receiver package is the most crucial factor for the near-end crosstalk of channel because it is the nearest coupling source among all passive components in channel. The differential insertion loss of the 30mm length package by the parameters defined in Table 2 is calculated as 3.3229dB at 14GHz, and we can obtain the total loss from bump of transmitter to the bump of receiver and also the COM value based on it.

To figure out the effect of package, we designed a real package with 3.42dB of differential loss at 14GHz. The insertion loss and crosstalk level of the channel 1 and 2 with the real package are depicted in Fig. 20 and Fig. 21. By a comparison from Fig. 18 to Fig. 21, an obvious change is found on loss and crosstalk. It inevitably affects the performance of channel from bump to bump and adds a variance of the COM.

Fig. 20. Insertion loss and crosstalk for designed channel 1 from bump to bump with real package.

Fig. 21. Insertion loss and crosstalk for designed channel 2 from bump to bump with real package.

The threshold of a high speed channel is defined as 3dB in the IEEE 802.3 specification with the pre-defined single-ended package model. As we mentioned, the real package might have different loss and termination condition, and naturally includes the crosstalk among lanes. Therefore, the 3dB criterion may need to be adjusted to adapt the real designed package situation. A comparison of COM values at 26.5325Gb/s for channel 1 and 2 without package, with IEEE pre-defined package model and real designed package

is described in Table 3. Although there is the similar level for loss, a difference is observed between the IEEE pre-defined package and real package. IEEE pre-defined package has a better COM than the real one, and the decrease in the COM of real package probably came from the crosstalk. Furthermore, even with the same package, due to the different crosstalk level for the ball to ball paths in channel 1 and channel, the variance on COM did not give the same value. The future determination of COM may consider the characteristic of real package into flow and make an appropriate evaluation of its crosstalk.

Table 3: Comparison of COM for channels with diverse package conditions.

Cases	Package Condition	COM (dB)
Channel 1	Without package	5.7470
	With IEEE pre-defined package	3.9445
	With real package	3.5176
Channel 2	Without package	4.5540
	With IEEE pre-defined package	3.5175
	With real package	3.4785

6. Conclusion and Future Plan

Channel operating margin is getting attracted in high speed channel area as a figure of merit to provide a channel performance evaluation flow. In this paper, we first propose a design flow for channel design by a fast hierarchical optimization method based on COM. Conventional channel design method based on OFAT, RSM, DOE and ANN by applying COM was introduced and the advantages on accuracy and speed for our proposed hierarchical design flow was demonstrated. By taking an evolution from electrical property to physical parameters in vertical levels, it offers a relative much faster design flow in the early design stage for high speed channel. Moreover, the implementation of 2.5D and 3D simulator in the components design also enhances the accuracy. The discontinuity, via, plays a significant role in the quality of the signal propagation in high speed channel. Novel design strategy to mitigate the fluctuation of impedance at via was addressed by diagnosing the reason of fluctuation corresponding to each part of via.

Characteristic such as loss and crosstalk of the designed channel is demonstrated and the effect of package on the COM was discussed by a comparison of diverse package conditions. In future works, we will concentrated on the enhancement of the design flow and contribute to the accurate COM criterion for high speed links.

7. Reference

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