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Integrated Photonics Based High Speed Arbitrary Waveform Generation

Shivangi Chugh and Shalabh Gupta

Abstract—We propose high speed arbitrary waveform generation using photonic integrated circuits. The proposed approach leverages the currently maturing photonic integration technology to overcome the bandwidth bottleneck associated with the interconnect parasitics in purely electronic circuits. As a proof of concept, we experimentally demonstrate PAM-4 and PAM-8 signal generation at up to 12.4 Gbaud, using this approach.

Index Terms—Photonic integrated circuits, silicon photonics, arbitrary waveform generator, photonic digital-to-analog converter.

I. INTRODUCTION

WITH link capacities increasing to cope with the growing bandwidth demand, the development of high-speed digital to analog converters (DACs) becomes necessary, as these enable the generation of transmission signals. The conventional DACs, designed in purely electronic integrated circuit technology are expected to soon render insufficient in facilitating ultra-high speed signal generation [1]. Use of photonics enabled digital to analog converters (PDACs) for waveform generation provides a way to circumvent the stated issue with the inherent advantages of photonics.

Previously investigated PDACs include parallel architectures based on summation of weighted multi wavelength signals [2], use of large area photodetectors [3], where the implementation is complex, and [4], [5], where coherent summation of optical fields is used by precise phase control. Other schemes as demonstrated in [6], [7] use dispersion components, while [8] is based on cross phase modulation and is vulnerable to pump noise.

In this letter, we present an arbitrary waveform generator (AWG) based on time domain waveform synthesis by a PDAC (presented earlier in our works [9], [10]). It removes the bottleneck due to bandwidth limitation arising from electrical interconnect parasitics in electronic DACs. For verifying the feasibility of the proposed architecture, we experimentally demonstrate the generation of uniform four level pulse amplitude modulated (PAM-4) and eight level pulse amplitude modulated (PAM-8) signals.

II. OPERATION AND SIMULATION

The implementation details of the proposed architecture of an AWG based on a PDAC are given in Fig. 1. This is an incoherent PDAC as phases of the signals are not precisely controlled. The continuous wave (CW) lightwave from the laser is divided into multiple CW lightwaves depending on the

number of channels required for generating the desired signal. The architecture follows a weighted summation approach. For N-bit PDAC operation, laser output is split into N-lightwaves, which are binary weighted by the tree architecture (or attenuators in each channel) used for dividing the power. Each of the lightwaves is given as a carrier to an intensity modulator, individually being driven by an independent electrical signal. Electric field at the output of each modulator is given by:

$$E_{o,k}(t) = \frac{E_{in}(t)}{\sqrt{2^k}} \cos \left(\frac{\pi}{2V_{\pi}} (V_{RF,k}(t) + V_{b,k}) \right), \quad (1)$$

where $E_{o,k}(t)$, $V_{RF,k}(t)$, and $V_{b,k}$ are the output electric field, RF signal voltage, and DC bias voltage of the modulator, respectively, on k^{th} -channel with input electric field being $E_{in}(t)$.

Fig. 1. Architecture of the proposed arbitrary waveform generator. OA: optical amplifier, PS: power splitter, MZM: Mach-Zehnder modulator, VOA: variable optical attenuator, TD: time delay, PD: photodetector, and TIA: trans-impedance amplifier.

The modulated optical signals are then given to variable optical attenuators (VOAs) and optical time delays (TDs) for precise control of amplitude and time as dictated by the waveform required. The optical signals are combined and subsequently converted to electrical domain using a configuration of photodetectors (PDs) shown in Fig. 1. Signals to be added are given to PDs, PD_{p1} through PD_{px} , which have their anodes connected to the input node of trans-impedance amplifier (TIA) and for any negative excursion, signals are applied to PDs, PD_{n1} through PD_{ny} , which have their cathodes connected to the input node of TIA. The number of these PDs, (used for addition and subtraction) may not necessarily be the same. Current at the PD configuration output is

Fig. 2. Simulation results: (a) uniform sixteen level signal generation; and (b) 4-bit PDAC transfer curve and the introduced DNL with 10% variation in responsivity.

$$I(t) = \sum_x I_{px}(t) - \sum_y I_{ny}(t) \quad (2)$$

$$I(t) = \alpha \Re P_{in} \sum_{k=1}^N \frac{1}{2^k} \cos^2 \left(\frac{\pi}{2V_\pi} (V_{RF,k}(t) + V_{b,k}) \right), \quad (3)$$

where I_{px} and I_{ny} correspond to photocurrents through PD_{px} and PD_{ny} , α is loss factor of the modulator, $\Re$ represents responsivity of the PD, and P_{in} is the power associated with the electric field E_{in} . Equation 3 gives the output of an ideal PDAC where the modulators and PDs are considered to be identical for each path. The electrical inputs to the modulators need to be synchronized and the length of waveguides to be matched for jitter free operation. With every component that deviates from the requisite behavior, non-ideality is introduced in the PDAC operation. For instance, if there is a change in responsivity of a PD, power through a modulator, or biasing of modulator, the analog signal at the output PD configuration becomes

$$I'(t) = I(t) + \sum_{k=1}^N \left(\alpha \Re'_k P_{in} + \alpha \Re'_{in,k} P_{in} + \alpha'_k \Re P_{in} \right) \times \cos^2 \left(\frac{\pi}{2V_\pi} (V_{RFk}(t) + V_{bk}) \right) \quad (4)$$

Here, $\Re'_k$, $\Re'_{in,k}$, and α'_k represent deviation in responsivity, power, and fraction associated with the deviation of bias point/loss of the modulator in the k^{th} -path, respectively, considered the input electrical signals are in synchronization. The terms in the summation in Eq. (4) contribute to differential non-linearity (DNL) of the PDAC.

For conversion of analog current signal to analog voltage signal and providing the gain, TIA can be used. With the availability of ultra small capacitance PDs [11], reduction of interconnect parasitics due to the availability of multi-input PDs and small interconnect lengths due to signal routing in optical domain and placement of PDs in close proximity, the overall parasitics are reduced (compared to that in electrical circuits) and hence the high bandwidth operation is obtained. This architecture implemented on a photonic integrated circuit, forms a small footprint, high bandwidth AWG based on a PDAC.

For verification of the proposed architecture, we simulated the 4-bit PDAC for generation of 50 GBd PAM-16 signal in Lumerical Interconnect. Here, four channels are enabled and all the four PDs are connected in parallel. The extinction ratio of each MZM and responsivity of each PD is set to 30 dB

Fig. 3. (a) Block diagram of the experimental set-up used for the proof of concept demonstration; (b) Micrograph of photonic die; (c) Probe station set-up for bare photonic die testing. CW: continuous wave, MZM: Mach Zehnder modulator, RF: radio frequency signal, EDFA: erbium doped fiber amplifier, OBPF: optical band-pass filter, SMF: single mode fiber, VOA: variable optical attenuator, PC: polarization controller, and SiPIC: silicon photonic integrated circuit.

and 1 A/W, respectively. The effect of RF drivers, used for applying modulating signals at 50 Gbps to the modulators, is also included. The PD thermal noise, shot noise, laser relative intensity noise (RIN), and TIA equivalent noise are enabled. A sixteen level signal generated is shown in Fig. 2(a). With a variation of $\pm 10\%$ in the responsivity of PD in channel with most significant bit (that has most significant effect on the PDAC performance), gives a DNL of 0.8 LSB as observed from the transfer curve in Fig. 2(b).

III. EXPERIMENT

The block diagram of experimental set-up used for the proof of concept demonstration of the proposed PDAC based AWG is shown in Fig. 3(a). Here, only a part of this architecture is implemented on-chip (for optimizing use of chip area). A silicon photonic integrated circuit (SiPIC) with the stated circuit (along with multiple other circuits), is fabricated in CMOS compatible 220 nm silicon on insulator technology. Micrograph of the SiPIC is given in Fig. 3(b).

To simplify the set-up, one modulator with an electrical signal input is used. We use a single frequency external cavity laser (ECL) operating at 1550 nm to provide carrier lightwave. The lightwave is modulated by a Lithium Niobate MZM, biased at quadrature point, driven by an electrical binary signal (non-return to zero) with a pseudo-random binary sequence (PRBS) having a length of $2^{23} - 1$ at a rate of 12.4 Gbps. Due to the high insertion loss of the MZM, modulated optical signal has low power of ~ 6 dBm and is, thus, boosted using an erbium doped fiber amplifier (EDFA) which is operated in constant output power mode and is set to give 15 dBm output optical signal power. This amplified signal is passed through an optical band-pass filter (OBPF) with a bandwidth of 100 GHz to remove out of band amplified spontaneous emission noise. The optical modulated signal is split using a 50:50 power splitter and passed onto two channels for PAM-4 generation. Each channel provides a time delay (provided by different lengths of optical fibers) so as to de-correlate and then time synchronize the signals in both channels. Variable optical

Fig. 4. Eyediagrams of the experimentally generated signals: (a) uniform four level pulse amplitude modulation at 24.8 Gbps; and (b) uniform eight level pulse amplitude modulation at 6 Gbps.

attenuators (VOAs) are used to maintain relative amplitudes of the signals on each channel where second channel, corresponding to least significant bit, has 3 dB less power than the power in the first channel (most significant bit path). The optical signals in the two channels are coupled to the SiPIC using grating couplers (GCs), while maintaining the polarization using off-chip polarization controllers (PCs) for obtaining maximum coupling efficiency. Each optical signal undergoes a coupling loss of 5 dB (due to limitation of alignment set-up). These signals are then applied to the PDs, connected in parallel, through the waveguides. The PDs have a responsivity of 0.45 A/W and a dark current of 20 nA at a reverse bias voltage of 1 V. Output is taken across an on-chip 50 Ω resistor using an RF probe (in ground-signal-ground configuration) and observed on a real time oscilloscope. Set-up for coupling light to and taking output from the SiPIC is shown in Fig. 3(c). For PAM-8 generation, a similar setup is used where a 2 Gbps modulated, amplified, and filtered optical signal is divided and given to three channels using two 50:50 power splitters. The signals in all the three channels are de-correlated and time synchronized using different lengths of optical fibers. The signals in second and third channel are attenuated with 3 dB and 6 dB attenuators, respectively and are coupled to chip using GCs through PCs. Two of these signals are given to a dual input PD, while the third is applied to a different PD.

Fig. 5. (a) Full range spectrum obtained on electrical signal analyzer for the two tone test with no observable intermodulation products (with input tones at 3.9 GHz and 4.1 GHz).

To inspect for the non-linear behaviour of the proposed AWG (or PDAC), a two tone test is carried out. For observation of non-linearity, sinusoidal signals are needed at two independent frequencies mandating use of two intensity modulators. Both the modulators are given the same optical carrier at a wavelength of 1550 nm. While one of the modulators is driven by a sinusoidal signal of 3.9 GHz, the other is driven by 4.1 GHz. The two modulated optical signals are coupled to two different PDs on the SiPIC. Output electrical signal spectrum is observed on electrical signal analyzer.

IV. RESULTS AND DISCUSSION

The PDAC operation with 2-bit and 3-bit resolution is validated. The eyediagrams in Figs. 4(a), (b) display PAM-4 generated at 12.4 GBd and PAM-8 generated at 2 GBd. Ratio level mismatch can be optimized using VOAs. A part of optical noise observed in the signals generated is due to vibration of the fiber array. With the two tones sent at 3.9 GHz and 4.1 GHz, no intermodulation (IM) products are observed. Spectrum obtained at the electrical signal analyzer is given in Fig. 5, which shows presence of second and third harmonics at frequencies 8.2 GHz and 12.3 GHz, respectively that are generated by the modulators but no tones at IM frequencies which means that PDAC does not generate any harmonics.

Fig. 6. Variation of FoM as a function of ENOB for 40 GHz bandwidth PDAC with and without TIA.

With availability of fully integrated lasers on silicon having good wall plug efficiency [12], [13], state-of-art electro-optic modulators which are thermally stable with low drive voltage and operate at sub-pJ/bit efficiency [14], low power drivers [15] and TIAs [16], the proposed AWG potentially provides a 40 GHz, 6-bit operation consuming only ~ 318 mW of power for generating a signal with an amplitude of 1 V_{pp}. The power consumption breakdown along with the corresponding references is given in Table I.

TABLE I
PROJECTED POWER BREAKDOWN OF 6-BIT PDAC FOR 40 GHz OPERATION.

Component [Ref]	# Units	Unit power	Total power (%)
PDAC with TIA			
Laser [12]	1	24.6 mW	24.6 mW (7.7)
Driver [15]	6	40 mW	240 mW (75.4)
TIA [16]	1	53.8 mW	53.8 mW (16.9)
PDAC without TIA			
Laser [12]	1	436.5 mW	436.5 mW (64.5)
Driver [15]	6	40 mW	240 mW (35.5)

The PDAC with TIA has a figure of merit (FoM) of 73.4 fJ/c-s and an effective number of bits (ENOB) of 5.76 for 40 GHz, 6-bit architecture. The projection shows an improvement, in terms of FoM, over state-of-the-art electronic DAC [17] that provides 30 GHz operation at a FoM of 90.2 fJ/c-s. Here,

$$FoM = \frac{P}{2^{ENOB} \times f_{s,nyq}} \quad (5)$$

where P is the power dissipation, and $f_{s,nyq}$ is the Nyquist sampling frequency. The resolution is limited by the total harmonic distortion (THD) introduced by TIA, which in turn reduces the signal to noise and distortion (SINAD) ratio

defined as the ratio of signal power level to the noise and distortion power level, calculated by

$$SINAD(dB) = -10 \log \left(10^{-SNR/10} + 10^{-THD/10} \right), \quad (6)$$

$$SNR = \frac{i_{av}^2}{i_{av}^2 RIN.B + 2q i_{av} B + i_{n,th}^2 B + Q_n}, \quad (7)$$

Here, i_{av} , RIN , B , $i_{n,th}$, and Q_n represent average current at the output of PD configuration, relative intensity noise of the laser, bandwidth, thermal noise, and quantization noise, respectively. ENOB is then correspondingly calculated, assuming single tone, using the equation

$$ENOB = \frac{SINAD - 1.76}{6.02}. \quad (8)$$

With the advancement in TIA design, achievable ENOB is likely to increase. For overcoming the limitation of resolution due to THD, PDAC can be used without TIA where laser RIN limits the resolution but at a considerably improved ENOB value of 8.4. Variation of FoM with ENOB for the PDAC with and without TIA is shown in Fig. 6 for 40 GHz operation. This is obtained by taking into consideration the splitter excess loss, modulator insertion loss, and multiple noise sources including thermal noise, shot noise, relative intensity noise, and quantization noise. The increase in resolution is accompanied with minimal increase in noise as shot noise depends on total power which remains unchanged.

In an integrated platform, high resolution operation can be achieved when an on chip modulator with good extinction ratio and stable bias point is used alongside PDs with small dark current and higher responsivity. The demonstrated data rate is restricted due to the absence of TIA, and high coupling loss from fiber to chip, and not due to intrinsic characteristics of the design. The architecture is simple, energy efficient and is not specific to a modulator type.

Use of very high speed modulators [18] and detectors [19] can make this architecture capable of surpassing bandwidth capability of the available electronic AWGs. The PDs available are highly linear and linearity of the architecture is majorly defined by TIA. An efficient pre-emphasis equalization is possible integrating the PDAC with equalizer demonstrated in our earlier work [20] which helps in realizing high quality signals.

Fig. 7. Proposed co-packaged integrated photonics based arbitrary waveform generator.

V. CONCLUSION

An AWG with ultra high speed signal generation using highly linear PDAC operation is presented. We propose to leverage the PIC technology to increase the bandwidth suppressing the electronic bottleneck using high bandwidth components and by reducing the interconnect lengths. An AWG

architecture with co-packaged integrated photonics and CMOS electronics, as shown in Fig. 7, enables compact, low power, high bandwidth signal generation solution for futuristic high bandwidth applications.

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