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Modeling the Evolution of Trap States with Thermal Post-deposition Treatments in Sol-gel Indium Zinc Oxide TFTs

Neel Chatterjee, *Graduate Student Member, IEEE*, Adam M. Weidling, P. Paul Ruden and Sarah L. Swisher, *Member, IEEE*

Abstract—Metal oxides have been investigated for use in displays and wearable electronics, owing to their high mobility in the amorphous state. In solution-processed oxide thin-film transistors, post-deposition thermal processing significantly change the film's transport properties, and is essential for high-performance devices. The mobility, bias stability and trapping-detraping related hysteresis are improved with higher processing temperatures, which is generally attributed to decreased localized states which act as electron traps. Here we develop a model to validate that post-deposition processing indeed changes the density and properties of the localized states. We obtain good agreement between this model and the experimental data measured from sol-gel indium zinc oxide TFTs. When the processing temperature increases from 300 to 500 °C, the model indicates that the trap state density in the bulk semiconductor and at the interface decrease by a factor of 5 and a factor of 3, respectively. Furthermore, the localized states become shallower, and the band mobility increases at higher processing temperatures.

Index Terms—Thin Film Transistors, Amorphous semiconductors, Indium Zinc Oxide, Semiconductor device modeling, Inorganic materials

I. INTRODUCTION

THIN film transistors (TFTs) find themselves in numerous applications such as AMOLED (Active Matrix Organic Light Emitting Diode) displays [1], wearable integrated systems [2], [3] and medical implants [4], [5]. Metal oxides such as indium gallium zinc oxide (IGZO), indium zinc oxide (IZO) and zinc tin oxide (ZTO) are excellent candidates for the active layer in TFTs because they provide at least an order of magnitude higher charge carrier mobility ($\sim 10\text{--}100\text{ cm}^2/\text{Vs}$) compared to a-Si ($< 1\text{ cm}^2/\text{Vs}$) [6], [7]. When compared to low-temperature poly-Si (LTPS), amorphous metal oxides are

beneficial for large-area applications because they are more uniform, whereas grain boundaries and non-uniform grain sizes degrade transport in LTPS [8]. In contrast to traditional vacuum-based deposition methods, solution-processing methods for metal oxides are low cost, can be processed at atmospheric conditions, can be easily deposited on large areas, and have roll-to-roll capability [9], [10]. Metal salt-based sol-gel chemistry is one of the preferred routes for synthesizing metal oxide inks.

Sol-gel chemistry is a mechanism where a phase transition occurs from a colloidal suspension (sol) to a network-like structure (gel). The metal salts are dissolved in an alcohol or an aqueous solution to form metal hydroxides (M—OH) from the metal cations. A condensation reaction occurs where the metal hydroxides form metal oxides (M—O—M) [9], [11]. Part of the condensation reaction occurs in solution during the synthesis. The as-deposited films often perform poorly as active materials in TFTs. Synthesis typically results in an intermediate metal hydroxide (M—OH) bonding which yield films with poor or no TFT performance due to high defect densities. Post-deposition thermal treatment at temperatures of 300–500 °C is often required to remove the unwanted solvents and facilitate the formation of M—O—M network, which enables efficient charge transport.

In addition to traditional thermal annealing, an array of novel post-deposition treatment methods have been investigated for sol-gel films. These include O_2/O_3 annealing [12], high-pressure annealing [13], deep-ultraviolet annealing [14], photonic curing [15]–[18]. Studies have been done to elucidate the effect of the presence of different ambient gases during the post-deposition annealing [19]–[22]. These improved post-deposition treatment techniques bring about changes in the semiconductor films. These changes can be manifested in the form of improved mobility, lower density of traps, and negative flatband voltage shift among many other phenomenon [19], [22]–[24]. To understand these phenomena, a deeper understanding of charge transport becomes useful.

Charge transport in inorganic TFTs is primarily modeled using percolation theory or trap-limited band transport, also called multiple trap and release (MTR). Percolation theory in oxides is best described assuming the random band edge model [25], [26]. In this model, the IGZO conduction band edge (E_m) is assumed to have potential barriers and wells due

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The authors are with the Department of Electrical and Computer Engineering, University of Minnesota, Twin Cities, Minneapolis, MN 55455, United States. (e-mail: sswisher@umn.edu)

to Ga^{3+} and Zn^{2+} ions, which is represented by a Gaussian distribution, where δ represents the standard deviation of the distribution. In the case of very high disorder or at low temperatures ($kT \ll e\delta$), the conductivity is dominated by the mobile electrons which have more energy than the percolation threshold energy level (E_p). The conductivity is then the average of the regional conductivities where $E_m > E_p$ [26], [27]. Under low disorder and at high temperatures ($kT \sim e\delta$), the conduction electrons have high thermal energy and their energy is comparable to the barrier distribution width. Under these conditions, the barrier distribution plays no role [27]. In cases where the temperature is high or the disorder is low, MTR can be readily used to describe the charge transport [26], [28]–[30]. Here, the charge transport is primarily through the extended states above the conduction band edge (also called the mobility edge or transport level). Charge carriers injected from the contacts either contribute to the conduction (delocalized electrons) or get trapped in the localized states. These localized electrons can then subsequently contribute to the current by thermal activation or a high field.

In the MTR framework, we take a deeper look at some models where different localized states have been introduced to explain a variety of experimental results. Models with an exponential and a Gaussian for the density of states (DoS) have been developed to explain the performance of oxide TFTs [31]. The improved operation of dual-active layer TFT over a single-active layer has been explained by a reduced density of trap states at the interface [32]. IGZO back-channel surface fixed charge has been modeled as electron traps to explain the increasing V_{ON} with decreasing channel thickness [33]. It has been proposed that the formation energy of defects increases as the annealing temperature is increased, resulting in a lower trap density [34]. In this work, we develop a model to quantify how the density of these localized states evolve with different thermal processing temperatures.

In this study, we fabricate TFTs with IZO as the active material which were thermally processed in a tube furnace at 300, 400 and 500 °C. We hypothesize that the localized states evolve with thermal processing which affects the device characteristics. A device model is proposed to model the mobility of these TFTs under the MTR framework to gain insight on how these states evolve and affect the charge transport. To gain a deeper understanding of the evolution of these localized states in the device stack, we introduce separate localized states for the semiconductor-dielectric interface and semiconductor (bulk) states. We confirm that with higher processing temperature, the localized states at the interface and bulk are reduced.

II. EXPERIMENTAL METHODS

A. Device Fabrication and Semiconductor Post-deposition Treatment

The bottom-gated TFTs were fabricated on a Silicon wafer with 500 nm of buffer oxide. First, 150 nm molybdenum (Mo) was sputtered to form the gate electrode. Then, 42 nm of hafnium dioxide (HfO_2) was deposited using Plasma Enhanced ALD at 100 °C to form the gate dielectric. Solution-processed indium zinc oxide (IZO) was synthesized using

Fig. 1: (a) Schematic of IZO TFTs (b) Optical micrograph of IZO TFT with W/L of 500 μm /80 μm .

15 mL of 2-methoxymethanol and 0.27 g of indium (III) nitrate hydrate and 0.17 g of zinc nitrate hexahydrate and was stirred at 80 °C for an hour. The resulting solution gives a 0.1 M IZO solution with an indium:zinc ratio of 60:40. Prior to semiconductor deposition, the dielectric surface underwent cleaning in a 4:1 mixture of sulfuric acid and hydrogen peroxide. The semiconductor was spin coated at 3000 rpm at room temperature in ambient conditions. After spin coating, the samples were baked on a hotplate at 150 °C for 10 minutes to remove residual solvents. This was repeated once, yielding a two-layer film.

Post-deposition treatment of the device stack consisted of a tube furnace anneal at 300, 400, or 500 °C for 1 hour in ambient conditions. The semiconductor was patterned and etched using an ion-mill. The source and drain contacts were then patterned and deposited using 100 nm of electron beam evaporated aluminum (Al). A gate hole was etched using an ion-mill to access the Mo gate. A schematic cross-sectional illustration and top-view optical micrograph of the completed devices are shown in Fig. 1 (a) and Fig. 1 (b), respectively.

B. Current-Voltage and Capacitance-Voltage Characteristics

The transfer curves (I_{ds} vs V_{gs}) were measured using Keysight B1500A by sweeping the gate voltage while holding the drain voltage constant. The source voltage was held at 0V for all the measurements and hence we call the gate-source and drain-source voltage the gate and drain voltages respectively. A hold time of 5 s was applied at the beginning of each sweep to avoid transient-related artifacts.

Capacitance-voltage measurements were performed using the step voltage quasi-static capacitance voltage (QSCV) technique. During the measurement, the source and drains of the TFTs are shorted and step voltage at the gate terminal is applied. The displacement current is measured after the voltage is applied at the gate electrode and the charge is computed by integrating the displacement current measured at the gate electrode. The capacitance is then computed using $C = \Delta Q / \Delta V$. Before each measurement, a hold time of 10 s was applied. The capacitance measurements were obtained using a delay time of 200 ms between successive voltage steps. A current integration time of 100 ms and a leakage integration time of 200 ms were used.

Fig. 2: Transfer characteristics for the different processing temperatures. The solid lines represent the forward sweep. The dashed lines represent the reverse sweep. The solid symbols are the gate currents for different drain voltages.

Fig. 3: QSCV forward and reverse sweeps for all the processing temperatures. Inset text indicates the flatband voltage shift in the forward and reverse sweeps for the three processing conditions.

III. EXPERIMENTAL RESULTS AND DISCUSSIONS

A. TFT Characteristics

Fig. 2 shows the transfer characteristics for the TFTs fabricated with the three processing temperatures. Forward (solid lines) and reverse sweeps (dashed lines) were obtained to assess the hysteretic behavior of the devices. It can be observed that as the processing temperature is increased from 300 to 500 °C, the hysteretic behavior reduces. The saturation current increases by an order of magnitude and the forward saturation turn-on voltage (V_{ON}) shifts towards negative gate voltages from 3 V to -5.5 V. Similar phenomena have been observed previously [19], [23].

Fig. 3 shows the QSCV measurements from one representative device from each of the three processing temperatures. The change in the flatband voltage (V_{FB}) between the forward and reverse sweep decreases as the processing temperature is increased. The flatband voltage for each of the sweeps was computed by taking the voltage at which the first derivative of the measured capacitance was maximum.

The maximum values of the capacitance curves decreases as the processing temperature increases. We hypothesize that this might be caused by a difference in the densification and composition of IZO films across the three post-deposition

treatments. Additionally, one important phenomenon to note in Fig. 3 is that the capacitance in the reverse sweep is shifted towards positive gate voltages when compared to the forward sweeps in all the cases. This indicates that acceptor-like states are dominant in the semiconductor and at the semiconductor-dielectric interface. Due to such a phenomenon, we model the localized states as having an acceptor-like behavior, as discussed in Section IV.

B. Effective Mobility Extraction

In the present work, we focus on the low lateral (low drain bias) and perpendicular field (low gate bias), linear effective mobility of the channel electrons in an IZO TFT. Experimentally, this parameter was extracted using the modified Hoffman method [35], [36], which is similar to the effective mobility extraction method used for MOSFETs. The effective mobility is determined at a small drain bias so that the charge is essentially uniformly distributed along the channel. The effective mobility is given as,

$$\mu_{eff}(V_{gs}) = \frac{L}{W} \frac{g_{ds}(V_{gs})}{Q_{acc}(V_{gs})} \quad (1)$$

where L and W are the channel length and width, respectively, and Q_{acc} is the accumulated charge per unit area discussed below. First, we calculate the drain conductance, g_{ds} , by measuring the drain current while sweeping the drain voltage (I_{ds} vs V_{ds}) from 0 to 100 mV. This is repeated for multiple gate voltages, with the gate voltage being stepped finely starting from the depletion region to the accumulation region. We then obtain the drain conductance (g_{ds}) at each gate voltage (V_{gs}) using,

$$g_{ds} = \left. \frac{\partial I_{ds}}{\partial V_{ds}} \right|_{V_{gs}} \quad (2)$$

This procedure is repeated for all the gate voltages spanning the depletion and accumulation regions. The resulting drain conductance curves for all the three processing temperatures is shown in Fig. 4(a).

Second, we calculate the accumulation charge per unit area, Q_{acc} , from the forward QSCV sweeps of Fig. 3 for the three processing temperatures using,

$$Q_{acc} = \frac{1}{WL} \int_{V_{FB}}^{V_{g,max}} (C - C_{ov}) dV \quad (3)$$

Here, C_{ov} is the overlap capacitance computed using the following relationship,

$$C_{ov} = \frac{\hat{C}_{ox} \hat{C}_{semi}}{\hat{C}_{ox} + \hat{C}_{semi}} \times 2 \times Area_{ov} \quad (4)$$

where $Area_{ov}$ represents the overlap area between the source/drain and the gate electrodes as can be seen in Fig. 1, $\hat{C}_{ox}$ and $\hat{C}_{semi}$ represent the areal oxide capacitance of the dielectric and depletion capacitance of the semiconductor layer, respectively. $\hat{C}_{semi}$ was computed using a dielectric constant of 7.8, which was determined using capacitance measurements of TFTs. The computed accumulated charge as a function of gate voltage is shown in Fig. 4(b).

Fig. 4: (a) Drain conductance (b) Accumulation charge from the QSCV measurements (c) Mobility vs gate voltage for one representative device across all the three processing temperatures.

Finally, the effective mobility is extracted from the drain conductance and accumulation charge using Equation 1. The results are shown in Fig. 4(c). The mobility at any given gate voltage increases with higher processing temperature, and the maximum achievable mobility is highest for the 500 °C processing temperature. The mobility curve keeps shifting towards negative gate voltages as the processing temperature increases, which may indicate a decreasing density of acceptor-like traps. A lower trap state density means there are more free electrons available to contribute to transport.

IV. MODEL DEVELOPMENT

In this section, we develop a TFT model to gain insight into the charge transport properties of TFTs which are processed at different temperatures. The model assumes a perfect metal contact with its Fermi level denoted as E_{FM} . The extended states are modeled as a two-dimensional, parabolic band with

Fig. 5: Band diagram for the TFT model. The horizontal axis shows the DoS for the different distributions whereas the vertical axis denoted the energy. E_C is the mobility edge above which delocalized states exist which we model as a 2D parabolic band. Below E_C , there are localized states which we model using a delta and exponential function DoS.

a degeneracy of 2 (for up and down spins). Assuming an effective mass, $m_e^* = 0.56$ [37], [38], we obtain our constant density of states (DoS), $D = (m_e^*)/(\pi\hbar^2)$ as $2.36 \times 10^{14}/\text{cm}^2\text{eV}$, above the mobility edge, E_C . The applied gate voltage, eV_g manifests itself as the difference between the Fermi level of the semiconductor, E_{FS} and the metal contact, E_{FM} as $eV_g = E_{FS} - E_{FM}$. The difference between E_C and E_{FS} , is denoted as ϵ_F , as shown in Fig. 5. To model the localized states below the mobility edge, we use an exponential and a delta function DoS. The discrete trap level, described by a delta function DoS, is E_t away from the mobility edge and has a density N_t . The exponential DoS is described using its density at the mobility edge, D_{exp} and its characteristic temperature, T_{exp} . The characteristic temperature describes the slope of the exponential tail states. We assume $T_{exp} = 150$ K for all our model fits, unless stated otherwise [31], [39]. We associate the exponential tail states with the semiconductor bulk [31], [39]–[41] and we tentatively associate the delta function DoS with the semiconductor-dielectric interface [42].

Both types of localized states in our model are assumed to be acceptor-like states, in the sense that they are (negatively) charged when occupied by an electron and neutral when unoccupied. In this work, we are only concerned with the effective mobility, which is extracted from the drain conductance assuming that the charge is uniformly distributed across the whole channel. Hence, there is no spatial variation of the effective mobility along the channel.

A. Free and Trapped Electron Concentrations

The total electron concentration can be divided into two types of carriers: free and trapped electrons. Before computing the free and trapped electron concentrations, it behooves us to write the complete DoS for our model. The DoS for all the energy levels in our model below and above the mobility edge, E_C are given as,

$$g(E) = \begin{cases} D, & E > E_C \\ D_{exp} \exp\left(\frac{E-E_C}{kT_{exp}}\right) + N_t \delta(E-E_t), & E \leq E_C \end{cases} \quad (5)$$

The free electron concentration, n_f above the mobility edge, is calculated using the Fermi-Dirac distribution function, $f_D(E, E_{FS})$ and constant 2D density of states for our delocalized states as,

$$n_f = \int_{E_C}^{\infty} D \times f_D(E, E_{FS}) dE \quad (6)$$

where D is the density of states for the delocalized states. To obtain the trap concentration for the delta function DoS located at E_t , below the mobility edge, we use the following,

$$n_{t,\delta} = \int_{-\infty}^{\infty} N_t \delta(E - E_t) \times f_D(E, E_{FS}) dE \quad (7)$$

where $n_{t,\delta}$ is the trapped electron concentration for the trap level, which depends on its density and the relative energy difference from the mobility edge. We now need to compute the trapped electron concentration for the exponential tail states. For the exponential tail states, we can write the trapped electron concentration as,

$$n_{t,exp} = D_{exp} \int_{-\infty}^{E_C} \exp\left(\frac{E - E_C}{kT_{exp}}\right) \times f_D(E, E_{FS}) dE \quad (8)$$

The expression for total trapped charges is then given as $n_t = n_{t,\delta} + n_{t,exp}$. We now relate the electron quasi-Fermi level to the applied bias at the gate contact. As noted earlier, the applied bias, $eV_g = E_{FS} - E_{FM}$, which can be further broken down as, $eV_g = \varepsilon_F - (E_{FM} - E_C)$. The quasi-Fermi level for our model, with respect to the mobility edge is given as,

$$\varepsilon_F = kT \ln \left[\exp\left(\frac{n_f}{n_0}\right) - 1 \right] \quad (9)$$

Here, $n_0 = kTD$. Now, we relate the mobility edge to the applied gate bias as,

$$E_C - E_{FM} = eV_0 + \frac{e^2}{C_{ox}}(n_f + n_t) \quad (10)$$

where C_{ox} is the oxide capacitance of the gate dielectric. The mobility edge is related to the gate metal Fermi level by the potential drop across the dielectric and some fixed charges. The V_0 in our model accounts for the fixed charges in the dielectric, the donor-like states in the semiconductor and work function differences between the metal contact and the semiconductor. We keep V_0 fixed at -5 V for all our fitting purposes.

B. Mobility Model

The mobility is modeled using a MTR model [28]–[30]. The premise of the model is that the conduction occurs through the delocalized states, although at low gate bias, most of the injected charge carriers are trapped in the localized states. The trapped carriers contribute to the conduction by thermal

Fig. 6: Mobility fits for different processing temperatures. The solid lines represent simulated data from the TFT model, and the open symbols represent extracted effective mobilities.

activation across the conduction band edge, also called the mobility edge. The injected charge from contacts can thus, either contribute to the current as free carriers or get trapped in the numerous trapped states below the band edge. The effective mobility for a given applied bias can be written as,

$$\mu_{eff} = \mu_0 \frac{n_f}{n_f + n_t} \quad (11)$$

The coefficient μ_0 is the intrinsic charge-carrier ‘band mobility’ in the delocalized states. It may depend on temperature and electron concentration. For the sake of simplicity, we consider μ_0 a constant and it serves as a fitting parameter for our model [25], [26].

V. MOBILITY FITS AND PARAMETER EXTRACTION

The TFT model developed was used to model the mobilities of the three processing temperatures and gain insight about the charge transport. The fitting parameters include the discrete trap level which has a density, N_t while its relative energy difference from the conduction band edge is E_t , density of states of the exponential tail states, D_{exp} and the band mobility, μ_0 . Fig. 6 shows the mobility curve of one representative device from each processing group which have been modeled.

For each of the representative devices shown in Fig. 6, the corresponding free and trapped electron concentrations are shown in Fig. 7. The free and trapped electron concentrations are shown on separate axes. For the complete gate voltage range investigated, higher processing temperature results in a higher free electron concentration (left axis) and lower trapped electron concentration (right axis). One interesting point to note are the gate voltages at which the free electron concentration abruptly increases, and the trapped electron concentration begins to saturate, for all the three cases. Let’s call this voltage V_C . The parameter V_C was determined as the point with maximum rate of change in the free electron concentrations for the three processing conditions. The numerical values of V_C are 0.15, -2.23 and -3.25 V for 300, 400 and 500 °C devices. As the density of traps decrease, V_C keeps shifting towards negative gate voltages. This observation is consistent with the negative gate voltage shifts we observed in V_{ON} and V_{FB} as the processing temperature is increased from 300 to 500 °C.

Fig. 7: Free (solid lines, left axis) and trapped (dash-dotted lines, right axis) electron concentrations for the three processing conditions. These are extracted from the model, for one representative device from each group.

Fig. 8: Box and whisker plots showing (a) semiconductor-dielectric interface trap density (N_t) (left axis) and its depth from the mobility edge (E_t) (right axis) (b) semiconductor bulk trap state density ($kT_{exp}D_{exp}$) (left axis) and the band mobility in the delocalized states (μ_0) (right axis) for the three processing temperatures. The horizontal line within each box represents the median for the data. The edges of the boxes represent the first and third quartiles. The lower and upper error bars represent the minimum and maximum values in the data, respectively.

Next, we discuss the extracted fitting parameters used to fit the experimental effective mobility for the devices in the 500 (10 devices), 400 (10 devices) and 300 °C (9 devices) processing conditions. Fig. 8(a) shows the interface trap density and depth from the mobility edge of the localized states associated with the delta function DoS as a function of processing temperatures. It can be observed that the density of these localized states decreases for increasing processing temperatures. The average trap density for the 500 °C devices is roughly half of that in the 400 °C devices, and the average density for the 400 °C devices is about one third that in the 300 °C devices. Furthermore, an interesting phenomenon to note is that these localized states are shallower for the higher processing temperatures. The depth of these traps linearly increases from ~ 4.5 kT in 500 °C to ~ 11 kT in the 300 °C devices. In the case of acceptor-like traps, shallow traps are less effective trap centers than the deeper ones. This implies that the relatively deeper traps in the case of 300 than the 400 and 500 °C, impedes the transport more effectively. Deeper traps generally have longer trapping/de-trapping time constants and thus give rise to more hysteretic behavior, as observed in the transfer characteristics (Fig. 2) and QSCV curves (Fig. 3). Thus, having shallower trap levels is desirable, which is induced by processing the semiconductor film at higher temperatures.

Next, we look at how the exponential tail states in the bulk evolve as a function of the processing temperatures. As noted earlier, we keep the characteristic temperature of the exponential tail states constant ($T_{exp}=150$ K). The DoS for the tail states at the mobility edge (D_{exp}) serves as our fitting parameter to best fit the data. In Fig. 8(b), we plot the total concentration ($kT_{exp}D_{exp}$) of the exponential tail states below the mobility edge for all the devices. We can observe that the exponential tail state densities (or the DoS at the mobility edge) decreased from $\sim 2 \times 10^{12}/\text{cm}^2$ to $\sim 4 \times 10^{11}/\text{cm}^2$ as the processing temperature of the devices was increased from 300 to 500 °C. This result can be attributed to the efficient removal of solvents and organic residues at higher processing temperatures [43]–[46].

The mobility of the electrons in the delocalized states, μ_0 is discussed next, which is shown on the right axis of Fig. 8(b). As can be observed in Fig. 8(b), the band mobility increases almost linearly from ~ 1 to ~ 10 to ~ 20 cm^2/Vs for the 300, 400, and 500 °C processing conditions, respectively. We hypothesize that the band mobility can be directly correlated to the metal oxide (M—O) to metal hydroxide (M—OH) conversion ratio and an improvement in the gel network. A higher M—O fraction could correspond to a higher band mobility since the M—O network assists in the conduction of electrons and is desirable for high quality TFTs [18], [47].

VI. CONCLUSIONS

It was observed that for different thermal treatments of solution-processed IZO, the extracted effective mobility shows a clear phenomenon of decreased localized state densities as the processing temperature increases. To explain these phenomena, we propose a model which considers both, the

semiconductor and interface trap states modeled as exponential and a delta function DoS. We fit the effective mobilities obtained from different processing temperatures with the ones obtained from our model. Our model provides an excellent fit for the mobility curve across all the devices (~ 10 in each group) in the three processing temperatures. The model fits provide crucial insights. The exponential tail states decrease in density as the processing temperature is increased. The traps associated with the delta function DoS become shallower and fewer density as the processing temperature is increased, which in turn improves the charge transport. The band mobility in the delocalized states also improves significantly as the processing temperature is increased.

Here, we evaluate the evolution of traps with one dielectric material and one sol-gel chemistry. We can employ this model to find optimal combinations of sol-gel chemistry, processing conditions and effect of ambient gases among other factors to design high-performance TFTs for plastic or other low temperature substrates. Furthermore, we can explore electro-structural evolution of metal oxides by utilizing this model in combination with analysis of chemical composition and bonding environments, crystallinity, and nanostructures at semiconductor-dielectric interfaces. This will allow us to delve deeper into the origin of the trap states in metal oxides and how to effectively reduce these to obtain high-performance TFTs. These insights will be especially valuable in the pursuit of high-performance TFTs on low-cost flexible substrates with low thermal budgets. These topics will be the subject of future work.

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