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Influence of Thermal Post-deposition on Trap States in Sol-gel Indium Zinc Oxide TFTs

Neel Chatterjee, *Graduate Student Member, IEEE*, Adam M. Weidling, Yuchen Zhou, P. Paul Ruden and Sarah L. Swisher, *Member, IEEE*

Abstract—In solution-processed oxide thin-film transistors, post-deposition thermal processing significantly changes the film's transport properties and is essential for high-performance devices. The mobility, bias stability and trapping-detrapping related hysteresis are improved with higher processing temperatures, which is generally attributed to decreased concentrations of localized states that act as electron traps. Fabricating and characterizing 29 devices, we provide further experimental evidence that post-deposition processing indeed leads to enhanced channel electron mobility in sol-gel indium zinc oxide TFTs, and, on the basis of a simple model, we extract physical parameters that yield a quantitative assessment of the changes in the densities and the properties of the localized trap states. The data is obtained for sol-gel indium zinc oxide thin films and TFTs subjected to thermal post-deposition processing from 300 to 500 °C. The extracted parameters indicate that the trap state density in the bulk semiconductor and at the interface decrease by factors of 5 and 3, respectively. Furthermore, the localized states become shallower, and the band mobility increases with higher processing temperatures.

Index Terms—Thin Film Transistors, Amorphous semiconductors, Indium Zinc Oxide, Semiconductor device modeling, Inorganic materials

I. INTRODUCTION

THIN film transistors (TFTs) find themselves in numerous applications such as AMOLED (Active Matrix Organic Light Emitting Diode) displays [1], wearable integrated systems [2] and medical implants [3]. Metal oxides such as indium gallium zinc oxide (IGZO), indium zinc oxide (IZO) and zinc tin oxide (ZTO) are excellent candidates for the

active layer in TFTs because they provide at least an order of magnitude higher charge carrier mobility (~ 10 – 100 cm^2/Vs) compared to a-Si (< 1 cm^2/Vs) [4]. When compared to low-temperature poly-Si (LTPS), amorphous metal oxides are beneficial for large-area applications because they are more uniform, whereas grain boundaries and non-uniform grain sizes degrade transport in LTPS [5]. Amorphous IGZO has been commercially employed for LCD backplanes and is typically deposited using sputtering [6], [7]. In contrast to traditional vacuum-based deposition methods, solution-processing methods for metal oxides are low cost, can be processed at atmospheric conditions, can be deposited on large areas, and have roll-to-roll capability [7], [8]. Sol-gel chemistry is one of the preferred routes for synthesizing metal oxide inks.

In a sol-gel, metal salts are dissolved in an alcohol or an aqueous solution to form metal hydroxides ($\text{M}-\text{OH}$). A condensation reaction occurs where $\text{M}-\text{OH}$ form metal oxides ($\text{M}-\text{O}-\text{M}$) [7]. The condensation reaction begins to occur in solution, but as-deposited films do not produce functional TFTs. Post-deposition thermal treatment at 300–500 °C is often required to convert metal hydroxides into oxides, and to remove any residual nitrate or acetate components of the metal salts. This densifies the film and facilitates the formation of a $\text{M}-\text{O}-\text{M}$ network, which enables efficient charge transport. These post-deposition thermal treatments bring about changes in the semiconductor films that can manifest themselves in the form of improved mobility, lower density of traps, and negative flatband voltage shift among many other phenomenon [9]–[12]. To understand these phenomena, a deeper understanding of charge transport becomes useful.

Charge transport in amorphous oxide TFTs, whether deposited by vacuum-based or solution-processed methods, is primarily modeled using percolation theory or the multiple trap and release (MTR) theory. Percolation theory in oxides is best described assuming the random band edge model [13]. In this model, the IGZO conduction band edge (E_m) is assumed to have potential barriers and wells due to Ga^{3+} and Zn^{2+} ions, which is represented by a Gaussian distribution, where δ represents the standard deviation of the distribution. In the case of very high disorder or at low temperatures ($kT \ll e\delta$), the conductivity is dominated by the mobile electrons which have more energy than the percolation threshold energy level (E_p). The conductivity is then the average of the regional conductivities where $E_m > E_p$ [13], [14]. Under low disorder

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The authors are with the Department of Electrical and Computer Engineering, University of Minnesota, Twin Cities, Minneapolis, MN 55455, United States. (e-mail: sswisher@umn.edu)

and at high temperatures ($kT \sim e\delta$), the conduction electrons have high thermal energy and their energy is comparable to the barrier distribution width and the barrier distribution plays no role [14]. In cases where the temperature is high or the disorder is low, MTR can be readily used to describe the charge transport [13], [15]. Here, the charge transport is primarily through the extended states above the conduction band edge (also called the mobility edge or transport level). Charge carriers injected from the contacts either contribute to the conduction (delocalized electrons) or get trapped in the localized states. These localized electrons can then subsequently contribute to the current by thermal activation or through field-induced delocalization.

The MTR framework has been used to introduce different localized states to explain a variety of experimental results. Models with an exponential and a Gaussian for the density of states (DoS) have been developed to explain the performance of oxide TFTs [16]. The improved operation of dual-active layer TFT over a single-active layer has been explained by a reduced density of trap states at the interface [17]. IGZO back-channel surface fixed charge has been modeled as electron traps to explain the increasing V_{ON} with decreasing channel thickness [18]. It has been proposed that the formation energy of defects increases as the annealing temperature is increased, resulting in a lower trap density [19].

In this work, we look at how sol-gel IZO thin-films evolve with annealing temperatures in terms of crystal structure, surface morphology and metal-oxide composition. After investigating these, we fabricate TFTs with sol-gel IZO as the active material. Three groups of TFTs that are thermally processed at 300, 400 and 500 °C are produced. Electrical characterization yields effective electron mobilities that vary with gate voltage. We then develop a simple model that relates the effective mobility to the population of localized and delocalized states. Physical parameters that characterize the localized (trap) states are extracted from experimental data. We confirm that with higher processing temperature, the channel electron mobility increases, and we present quantitative results for the reduction in density and trap efficiency of the localized states.

II. EXPERIMENTAL METHODS

A. IZO Synthesis, Thin Film Deposition and Post-deposition treatments

Solution-processed indium zinc oxide (IZO) was synthesized using 15 mL of 2-methoxyethanol and 0.27 g of indium (III) nitrate hydrate and 0.17 g of zinc nitrate hexahydrate and was stirred at 80 °C for an hour. The resulting solution gives a 0.1M IZO with an In:Zn ratio of 60:40. Prior to semiconductor deposition, the dielectric surface underwent cleaning in a 4:1 mixture of sulfuric acid and hydrogen peroxide. The semiconductor was spin coated at 3000 rpm at room temperature in ambient conditions. After spinning the devices, they were baked on a hotplate at 150 °C for 10 minutes to remove residual solvents. This was repeated once, yielding a two-layer film. Post-deposition treatment of the device stack consisted of a tube furnace anneal for one hour at 300, 400, or 500 °C in ambient conditions.

Fig. 1: (a) Schematic of IZO TFTs (b) Optical micrograph of IZO TFT with W/L of 500 μm /80 μm .

B. IZO Thin Film Characterization

IZO films were deposited as described above onto 46 nm thermally-grown SiO_2 and annealed at 300, 400 and 500 °C. X-ray photoelectron spectroscopy (XPS) using an Ulvac PHI VersaProbe III system was employed to investigate the chemical composition of the three thin films. The survey scans were obtained using a pass energy of 280 eV using 1 eV per step. High-resolution scans were then obtained using a pass energy of 55 eV using 0.1 eV per step. Surface contaminants from each sample were removed using an Ar sputter prior to each measurement. Peak-fitting software was used to perform compositional analysis. Grazing incidence X-ray diffraction (GIXRD) using a Bruker X-ray microdiffractometer and a 2D detector with a Co X-ray source ($\lambda=0.179$ nm) was used to analyze the crystallinity of the thin films. K_β contributions were removed by conditioning the X-ray beam with a graphite monochromator. Two frames were collected covering a total range of 40° (2θ) at an incident angle of 5° . Atomic force microscopy (AFM) was used to analyze the surface morphology of a $1 \mu\text{m} \times 1 \mu\text{m}$ area using a Digital Instruments NanoScope III scanning probe microscope in tapping mode. Gwyddion software was used to analyze the surface roughness and extract cluster radius using the watershed algorithm.

C. TFT Fabrication

The bottom gated TFTs were fabricated on a silicon wafer with 500 nm of buffer oxide. First, 150 nm molybdenum was sputtered to form the gate electrode. Then, 42 nm of HfO_2 was deposited using Plasma Enhanced ALD at 100 °C to form the gate dielectric. The IZO sol-gel was spin coated onto the gate dielectric and then annealed in the tube furnace, as described above. The semiconductor was lithographically patterned and etched using an ion-mill. The source and drain contacts were then patterned and deposited using 100 nm of electron beam evaporated aluminum. A gate contact hole was etched using an ion-mill. A schematic cross-sectional illustration and top-view optical micrograph of the device is shown in Fig. 1.

D. Electrical Characterization of IZO TFTs

All electrical measurements were performed using Keysight B1500A. The transfer curves (I_{ds} vs V_{gs}) were obtained by sweeping the gate voltage while holding the drain voltage constant. The source voltage was held at 0 V. A hold time of 5 s was applied at the beginning of each sweep to avoid transient-related artifacts. Capacitance-voltage measurements

were performed using the step voltage quasi-static capacitance voltage (QSCV) technique. During the measurement, the source and drain of the TFTs are shorted and step voltage at the gate terminal is applied. The displacement current is measured after the voltage is applied at the gate electrode and the charge is computed by integrating the displacement current measured at the gate electrode. The capacitance is then computed using $C = \Delta Q / \Delta V$. Before each measurement, a hold time of 10 s was applied. The capacitance measurements were obtained using a delay time of 200 ms between successive voltage steps. A current integration time of 100 ms and a leakage integration time of 200 ms were used. Finally, TFT stability was characterized using constant bias stress measurements. After obtaining the pre-stressed transfer curves, a constant gate bias of $V_{gs} - V_{ON} = 10$ V was applied for each device. The source and the drain were grounded for the entire stress period. The transfer curves were measured after various stress intervals, and V_{ON} was obtained from each forward linear sweep. ΔV_{ON} represents the change with respect to the pre-stressed transfer curve. The maximum accumulated stress that each device experienced was 6000 s. All electrical measurements were taken at room temperature, and $T = 300$ K in all that follows.

III. EXPERIMENTAL RESULTS AND DISCUSSIONS

A. IZO Thin Film Characteristics

Thin film characterization data obtained from XPS, XRD and AFM analysis of IZO films annealed at 300, 400 and 500 °C are shown in Fig. 2. Fig. 2 (a)-(c) show the O1s spectra obtained from XPS for the IZO films. A series of Gaussian and Lorentzian peaks were fit to the data to deconvolute the peaks. The spectral deconvolutions include two peaks: the peak at ~ 529.9 eV represents the metal oxygen (M-O) bonding and the peak at ~ 531.3 eV is attributed to M-OH and other oxygen-related defects [20], [21]. To compare the different samples, the data were normalized and the relative areas of M—O and M—OH were extracted. The ratio of M—OH decreased from 21% to 16% when the processing temperature was increased from 300 to 400 and 500 °C, indicating a better M—O network to assist the electron conduction. The M—O to M—OH ratio remained similar in the case of 400 and 500 °C, indicating that no further conversion in terms of M—O concentration was achieved when annealed at 500 °C.

To investigate the crystal structure of the films, GIXRD was performed and the results are summarized in Fig. 2 (d). No detectable crystallites were observed as none of the films show diffraction peaks. For reference, we include the spectra of bulk In_2O_3 and ZnO to show that none of the constituent peaks are visible in any of the IZO films.

We next investigated the surface morphology using AFM. The height profile for each film and the calculated mean surface roughness are shown in Fig. 2 (e-g). The morphology remained smooth and the surface roughness was below 1 nm_{RMS} for all the cases. As the processing temperature was increased from 300 to 500 °C, the surface roughness decreased from ~ 0.9 to ~ 0.6 nm_{RMS} . Furthermore, the surface morphology changed as the processing temperature was increased.

In Fig. 2 (e), it can be observed that for the 300 °C sample, the surface features, which we call *surface clusters*, are small in size. However, once the annealing temperature is increased to 400 and 500 °C, these surface clusters become larger. The distribution of the extracted cluster radii for the three films are shown in Fig. 2 (h). The surface cluster radius increased from ~ 1 to ~ 5 to ~ 15 nm as the temperature was increased from 300 to 400 to 500 °C, respectively.

B. IZO TFT Characteristics

In this section, we characterize the electrical behaviour of the IZO TFTs, providing the information that will be used in following sections to extract the effective electron mobility and relate it to the density of localized states. Transfer characteristics of the three processing temperatures are shown in Fig. 3. Forward and reverse sweeps were obtained to assess the hysteretic behavior of the devices. It can be observed that as the processing temperature is increased from 300 to 500 °C, the hysteretic behavior reduces. The saturation current increases by an order of magnitude and the forward saturation turn-on voltage (V_{ON}) shifts towards negative gate voltages from 3 V to -5.5 V. The negative turn-on voltage implies the presence of a large electron concentration in the film [19], and a similar negative shift of V_{ON} with increased annealing temperature has been observed previously [9], [11].

Fig. 4 shows the QSCV measurements from one representative device from each of the three processing temperatures. The change in the flatband voltage (V_{FB}) between the forward and reverse sweep decreases as the processing temperature is increased. The flatband voltage for each of the sweeps was computed by taking the voltage at which the first derivative of the measured capacitance was maximum. One important phenomenon to note in Fig. 4 is that the capacitance in the reverse sweeps are shifted towards positive gate voltages when compared to the forward sweeps in all the cases. This indicates that acceptor-like trap states are dominant in the semiconductor and at the semiconductor-dielectric interface. The maximum capacitance also decreases as the processing temperature increases, which can be attributed to the reduction in the HfO_2 capacitance. HfO_2 capacitors ($\text{Mo}/\text{HfO}_2/\text{Al}$) processed at 300, 400, and 500 °C exhibited a similar decrease in capacitance from 3.55 to 3.43 to 3.11×10^{-7} F/cm^2 .

To further explore the nature of the traps, the stability of the IZO TFTs under a constant gate bias stress is shown in Fig. 5. The change in V_{ON} from the pre-stressed condition is shown as a function of stress time. The positive gate bias gradually fills up the available trap states, making them negatively charged. A positive V_{ON} shift occurs due to the charge screening by the occupied negatively charged trap states. This leads to additional applied gate bias required to turn on the device. The magnitude of the V_{ON} shift is larger in the case of 400 than the 500 °C device. This indicates the presence of a larger density of trap states at the semiconductor-dielectric interface and the IZO bulk in the device processed at 400 °C [22], [23]. In the case of 300 °C, V_{ON} keeps increasing and doesn't saturate even after the application of 6000 s of stress, indicating a larger density of localized states

Fig. 2: (a-c) The O1s spectra of IZO films annealed at 300, 400 and 500 °C. The WSSR (weighted residual sum of squares) above each spectra indicates the goodness of fit. (d) Diffraction spectra obtained using GIXRD for the IZO films. The XRD peaks of In₂O₃ (PDF no. 98-001-9088) and ZnO (PDF no. 98-000-0483) are shown for reference. (e-g) AFM images of a 1 μm × 1 μm area of the three IZO films. The insets show the RMS surface roughness. (h) Evolution of cluster radii as a function of processing temperature, extracted from AFM images. The horizontal line within each box represents the median. The edges of the boxes represent the first and third quartiles. The upper and lower whiskers are 1.5× the third and first quartiles respectively. The solid symbols represent outliers.

Fig. 3: Transfer characteristics for the different processing temperatures. The solid lines represent the forward sweep. The dashed lines represent the reverse sweep. The solid symbols are the gate currents for different drain voltages. The solid arrow represents the forward sweep and the dashed arrow represents the reverse sweep.

in the device stack than the 400 and 500 °C devices. Due to positive V_{ON} shifts, coupled with the clockwise hysteresis in the QSCV measurements, we model the localized states as having an acceptor-like behavior, as discussed in Section IV.

C. Effective Mobility Extraction

In the present work, we focus on the effective mobility of the channel electrons in IZO TFTs as a function of gate bias at

Fig. 4: QSCV forward and reverse sweeps for IZO TFTs at different processing temperatures. The solid and the dashed arrows represent the forward and reverse sweeps respectively. Inset text indicates the flatband voltage shift in the forward and reverse sweeps for the three.

low drain bias. Experimentally, this parameter was extracted using the modified Hoffman method [22], which is similar to the effective mobility extraction method used for MOSFETs. The effective mobility is determined at a small drain bias so that the charge is essentially uniformly distributed along the

Fig. 5: Bias stress stability of IZO TFTs. The change in the turn-on voltage from the pre-stressed condition (ΔV_{ON}) with accumulated stress time is shown for different processing temperatures.

Fig. 6: Extracted effective mobility (open symbols) of IZO TFTs for different processing temperatures. Also shown (solid lines) are the model results based on the extracted parameters discussed below.

channel. It is given by,

$$\mu_{eff}(V_{gs}) = \frac{L}{W} \frac{g_{ds}(V_{gs})}{Q_{acc}(V_{gs})} \quad (1)$$

where L and W are the channel length and width, respectively, and Q_{acc} is the accumulated charge per unit area discussed below. First, we calculate the drain conductance, g_{ds} , by measuring the drain current while sweeping the drain voltage (I_{ds} vs V_{ds}) from 0 to 100 mV. This is repeated for multiple gate voltages, with the gate voltage being stepped finely starting from the depletion region to the accumulation region. We then obtain the drain conductance (g_{ds}) at each gate voltage (V_{gs}) using, $g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}}|_{V_{gs}}$. This procedure is repeated for all the gate voltages spanning the depletion and accumulation regions. Second, we calculate the accumulation charge per unit area, Q_{acc} , from the forward QSCV sweeps of Fig. 4 for the three processing temperatures using, $Q_{acc} = \frac{1}{WL} \int_{V_{FB}}^{V_{gs, max}} (C - C_{ov}) dV$. Here, V_{FB} is the flat-band voltage, determined as the gate voltage at which the capacitance becomes appreciable. C_{ov} is the overlap capacitance computed using the following

relationship,

$$C_{ov} = \frac{\hat{C}_{ox} \hat{C}_{semi}}{\hat{C}_{ox} + \hat{C}_{semi}} \times 2 \times Area_{ov} \quad (2)$$

where $Area_{ov}$ represents the overlap area between the source/drain and the gate electrodes as can be seen in Fig. 1, $\hat{C}_{ox}$ and $\hat{C}_{semi}$ represent the areal oxide capacitance of the dielectric and depletion capacitance of the semiconductor layer, respectively. $\hat{C}_{semi}$ was computed using a dielectric constant of 7.8, which was determined using capacitance measurements of TFTs.

Finally, the effective mobility is extracted from the drain conductance and accumulation charge using Equation 1. The results are shown in Fig. 6. The mobility at any given gate voltage increases with higher processing temperature, and the maximum achievable mobility is highest for the 500 °C processing temperature. The mobility curve keeps shifting towards negative gate voltages as the processing temperature increases, which may indicate a decreasing density of acceptor-like traps. A lower trap state density means there are more free electrons available to contribute to transport.

IV. MODEL DEVELOPMENT

In this section, we develop a simple model to gain insight into the trap-related charge transport properties of TFTs that are processed at different temperatures. The model assumes a perfect metal contact with a Fermi level denoted as E_{FM} . The extended states are modeled as a two-dimensional, parabolic band (with spin degeneracy). Assuming an effective mass, $m_e^* = 0.56$ [23], [24], we obtain our constant density of states (DoS), $D = (m_e^*)/(\pi \hbar^2)$ as $2.36 \times 10^{14}/\text{cm}^2\text{eV}$, above the mobility edge, E_C . The latter energy can be considered the mobility edge. The applied gate voltage, eV_g manifests itself as the difference between the Fermi level of the semiconductor, E_{FS} and the metal contact, E_{FM} as $eV_g = E_{FS} - E_{FM}$. The difference between E_C and E_{FS} , is denoted as ϵ_F , as shown in Fig. 7.

To model the localized states below the mobility edge, we use an exponential tail and a delta function. The discrete trap level, described by a delta function DoS, is E_t (relative to E_C) and has a density N_t . The exponential DoS is described using its density at the mobility edge, D_{exp} and a characteristic temperature, T_{exp} that is taken to be $T_{exp} = 150$ K. The characteristic temperature describes the slope of the exponential tail states. We assume $T_{exp} = 150$ K for all cases considered in this work [16], [25]. We associate the exponential tail states with the semiconductor bulk [16], [25], [26] and we tentatively associate the delta function DoS with the semiconductor-dielectric interface [27]. Both types of localized states in our model are assumed to be acceptor-like states, in the sense that they are (negatively) charged when occupied by an electron and neutral when unoccupied. The states in the exponential tail form rather shallow traps as $T_{exp} = T/2$. In this work, we are only concerned with the effective mobility, which is extracted from the drain conductance at low drain bias. Hence, there is no spatial variation of the effective mobility along the channel.

Fig. 7: Band diagram for the TFT model. The horizontal axis shows the DoS for the different distributions whereas the vertical axis denotes the energy.

A. Free and Trapped Electron Concentrations

The total electron concentration can be divided into two types of carriers: free and trapped electrons. Before computing the free and trapped electron concentrations, it behooves us to write the complete DoS for our model. It is given by,

$$g(E) = \begin{cases} D, & E > E_C \\ D_{exp} \exp\left(\frac{E-E_C}{kT_{exp}}\right) + N_t \delta(E-E_t), & E \leq E_C \end{cases} \quad (3)$$

In all cases considered in this work the density of states of the exponential tail is extremely small at E_t .

The free electron concentration, n_f , is calculated using the Fermi-Dirac distribution function, $f_D(E, E_{FS})$ and constant 2D density of states of the delocalized states as,

$$n_f = \int_{E_C}^{\infty} D \times f_D(E, E_{FS}) dE \quad (4)$$

To obtain the trapped electron concentration for the delta function DoS located at E_t , below the mobility edge, we use the following,

$$n_{t,\delta} = \int_{-\infty}^{\infty} N_t \delta(E-E_t) \times f_D(E, E_{FS}) dE \quad (5)$$

We then compute the trapped electron concentration for the exponential tail states as,

$$n_{t,exp} = D_{exp} \int_{-\infty}^{E_C} \exp\left(\frac{E-E_C}{kT_{exp}}\right) \times f_D(E, E_{FS}) dE \quad (6)$$

The expression for total trapped charges is then given as $n_t = n_{t,\delta} + n_{t,exp}$. We now relate the electron quasi-Fermi level to the applied bias at the gate contact. As noted earlier, the applied bias, $eV_g = E_{FS} - E_{FM}$, which can be further broken down as, $eV_g = \varepsilon_F - (E_{FM} - E_C)$. The quasi-Fermi level for our model, with respect to the mobility edge is given as, $\varepsilon_F = kT \ln \left[\exp\left(\frac{n_f}{n_0}\right) - 1 \right]$, where, $n_0 = kTD$. Next, we relate E_C to the applied gate bias as,

$$E_C - E_{FM} = eV_0 + \frac{e^2}{C_{ox}}(n_f + n_t) \quad (7)$$

where C_{ox} is the oxide capacitance of the gate dielectric. E_C is related to the gate metal Fermi level by the potential drop across the dielectric which is associated with the total electron concentration. V_0 accounts for any fixed charges in the gate dielectric and for work function differences between the metal contact and the semiconductor. We keep V_0 fixed at -5 V for all examples discussed here.

B. Mobility Model

The mobility is modeled using the MTR theory [15], [28]. The premise of the model is that the conduction occurs through the delocalized states, although at low gate bias, most of the injected charge carriers are trapped in the localized states. The trapped carriers contribute to the conduction by thermal activation across the conduction band edge, also called the mobility edge. Injected charge carriers can thus, either contribute to the current as free carriers or get trapped in the numerous trapped states below the band edge. The effective mobility for a given applied bias can be written as,

$$\mu_{eff} = \mu_0 \frac{n_f}{n_f + n_t} \quad (8)$$

where μ_0 is the intrinsic (temperature dependent) charge-carrier ‘band mobility’ of electrons in the delocalized states. For the sake of simplicity, we consider μ_0 to be independent of the electron concentration, but it will vary with semiconductor and/or interface morphology, which in turn may be affected by the post-deposition treatments that are the focus of this work [13].

V. MOBILITY FITS AND PARAMETER EXTRACTION

The model described above was used to analyze the effective mobilities of devices subjected to three processing temperatures. The parameters extracted include the discrete trap level, E_t , and its density N_t . Furthermore, the density of states of the exponential tail states, D_{exp} , and the band mobility, μ_0 . Fig. 6 shows the mobility curve of one representative device from each processing group.

For each of the devices shown in Fig. 6, the corresponding free and trapped electron concentrations are shown in Fig. 8 (a-b). For the gate voltage range investigated, higher processing temperature results in a higher free electron concentration and lower trapped electron concentration. In the very low gate bias regime, both n_t and n_f are non-degenerate, i.e. E_{FS} is well below E_t , but E_{FS} rises directly with V_g because the voltage drop across the gate oxide due to the electrons is negligible. Consequently, n_t and n_f increase exponentially with eV_g/kT (kT/e is very small on the scale shown). Evidently, the larger the E_t , the smaller is the ratio of free to trapped electrons, n_f/n_t . Only when the total electron concentration reaches about $\sim 6 \times 10^{10}/\text{cm}^2$, does the associated voltage drop become appreciable on that energy scale ($\sim (kTC_{ox})/e \simeq 6.2 \times 10^{10}/\text{cm}^2$, where $C_{ox} \simeq 3.8 \times 10^{-7} \text{ F}/(\text{cm}^2)$). This phenomenon is reflected clearly in Fig. 8b where, for the devices processed at 400 and 500 °C and $V_g < -5 \text{ V}$. For the device processed at 300 °C, the rapid rise of n_f pertains only to extremely low concentrations because, as will be discussed

Fig. 8: Free (solid lines, left axis) and trapped (dash-dotted lines, right axis) electron concentrations for the three processing conditions on (a) linear-linear and (b) log-linear scale. These are extracted from the model, for one representative device from each group.

below, E_t is large in that case. However, in all cases, E_{FS} is rising slowly with V_g when $n_{t,\delta}$ becomes comparable to N_t (E_{FS} is then essentially pinned at E_t). Once these localized states are filled, E_{FS} again rises more rapidly with increasing V_g and consequently the free electron concentration increases quickly. Only for the devices processed at 300 °C is the total DoS of the exponential tail non-negligible compared to kTD and thus causes appreciable trapping in the shallow tail states. In all the cases, this eventually leads to situations in which the free electron induced voltage drop across the gate insulator dominates over ε_F and consequently, the free electron concentration becomes proportional to V_g . This is evident in Fig. 8a. We denote the voltage extrapolated from the linear rise of the free electron concentration by V_C . This parameter for the three processing conditions is obtained as: 0.15, -2.33 and -3.15 V for 300, 400 and 500 °C devices.

Next, we discuss the parameters extracted from the experimental effective mobility for groups of the devices subjected to 500 (10 devices), 400 (10 devices) and 300 °C (9 devices) post-deposition thermal processing. Fig. 9(a) shows the interface trap density and depth from the mobility edge of the localized states associated with the delta function DoS as a function of processing temperatures. The density of these localized states decreases for increasing processing temperatures. The average trap density for the 500 °C devices is roughly half of that in the 400 °C devices, and the average density for the 400 °C devices is about one third that in the 300 °C devices. Furthermore, an interesting phenomenon to

Fig. 9: (a) The semiconductor-dielectric interface trap density (N_t , left axis) and its depth from the mobility edge (E_t , right axis) obtained from the model for the three processing temperatures. (b) The semiconductor bulk trap state density ($kT_{exp}D_{exp}$, left axis) and the band mobility in the delocalized states (μ_0 , right axis) for the three processing temperatures. For the box and whisker plots, the horizontal line within each box represents the median, the edges represent the first and third quartiles. The lower and upper whiskers represent the minimum and maximum values, respectively.

note is that these localized states are shallower for the higher processing temperatures. The depth of these traps linearly decreases from ~ 11 kT in the 300 °C to ~ 4.5 kT in the 500 °C. In the case of acceptor-like traps, shallow traps are less effective trap centers than the deeper ones. This implies that the relatively deeper traps in the case of 300 than the 400 and 500 °C, impedes the transport more effectively. Deeper traps generally have longer trapping/de-trapping time constants and thus give rise to more hysteretic behavior, as observed in the transfer characteristics (Fig. 3) and QSCV curves (Fig. 4). Thus, having shallower trap levels is desirable, which is achieved by processing the semiconductor film at higher temperatures.

Next, we look at how the exponential tail states in the bulk evolve as a function of the processing temperature. As noted earlier, we keep the characteristic temperature of the exponential tail states constant ($T_{exp}=150$ K). The DoS for the tail states at the mobility edge (D_{exp}) is adjusted to best fit the data. In Fig. 9(b), we plot the total concentration ($kT_{exp}D_{exp}$) of the exponential tail states below the mobility edge for all the devices. We can observe that the exponential tail state densities (or the DoS at the mobility edge) decreased from

$\sim 2 \times 10^{12}/\text{cm}^2$ to $\sim 4 \times 10^{11}/\text{cm}^2$ as the processing temperature of the devices was increased from 300 to 500 °C.

The mobility of the electrons in the delocalized states, μ_0 is discussed next, which is shown on the right axis of Fig. 9(b). As can be observed in Fig. 9(b), the band mobility increases almost linearly from ~ 1 to ~ 10 to ~ 20 cm^2/Vs for the 300, 400, and 500 °C processing conditions, respectively.

The decrease in the density of extracted trap states in the semiconductor and at the semiconductor-dielectric interface and the increase in the band mobility are consistent with the experimentally obtained thin-film characteristics. IZO films annealed at 500 °C exhibited a higher concentration of M-O bonding and a reduced M-OH concentration, and the resulting films were smoother with larger surface clusters, but with no change in crystallinity. We hypothesize that the band mobility can be directly correlated to the M—O to M—OH conversion ratio (as shown in Fig. 2 (a)-(c)) and an improvement in the gel network. A higher M—O fraction could correspond to a higher band mobility since the M—O network assists in the conduction of electrons and is desirable for high quality TFTs [21], [29]. These data, coupled with the modeled trap densities, lead us to hypothesize that the 500 °C anneal produces a more uniform IZO thin film with an extensive M-O-M network and fewer M-OH impurity defects, creating a larger and more efficient electron transport network and a lower concentration of bulk and interface traps.

Previous reports have attributed a reduction in tail states to the efficient removal of solvents and organic residues at higher processing temperatures [30]–[32], but we hypothesize that it is the combination of the chemical and morphological changes that improve the electron transport. For example, it is well-established that decreasing the M-OH concentration in sol-gel oxides improves TFT performance [21], [29], [33]. While our device model does not identify the atomic nature of the trap states, first-principles calculations have previously predicted that hydroxyl groups in IGZO should not generate trap states in the bandgap [34]. This is consistent with our findings: increasing the processing temperature from 400 to 500 °C produced no change in the M-OH concentration extracted from XPS, yet the band mobility increased, and the trap state density decreased. These findings imply that efficient conversion from the M-OH to M-O phase is necessary but not sufficient for good electron transport in oxide TFTs. This phenomenon is not specific to sol-gels since M-OH defects have a low formation energy and can form spontaneously in oxide films [34], irrespective of the deposition method. Studies have shown that post-deposition annealing reduces the M-OH concentration in vacuum-deposited oxide films as well [35]. Thus, we hypothesize that the model can also be applied to oxide TFTs where the active material was deposited using vacuum-based methods.

VI. CONCLUSIONS

It was observed that for different thermal treatments of solution-processed IZO, the extracted effective mobility shows clear features associated with decreased localized state densities as the processing temperature increases. Increasing pro-

cessing temperature reduces M-OH concentration, reduces surface roughness, and leads to an increase in the size of surface cluster. Lastly, it has no impact on crystallinity of the films. The TFTs show a higher saturation current, higher carrier mobility and reduced hysteresis with increasing processing temperature. To explain the trapping-related phenomena, we propose a simple model which considers semiconductor and interface trap states modeled, respectively, as exponential and a delta-function densities of state below the mobility edge. We extract parameters characterizing these trap states from the experimentally determined gate voltage dependence of the low-field effective mobilities obtained from groups of devices subjected to different processing temperatures. Both, the traps giving rise to a delta-function DoS and the exponential tail states decrease in density as the processing temperature is increased. In addition, the traps associated with the delta-function DoS become shallower. Lastly, the band mobility in the delocalized states also improves as the processing temperature is increased. In the future, we plan to include the trap dynamics into the model [36], [37], such as to address the hysteresis observed. Ultimately, our objective is to employ this approach to the exploration of optimal combinations of sol-gel chemistry, processing conditions, and the effect of ambient gases among other factors to further improve IZO TFT performance.

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