Modified Startup Delay Providing Circuit for Integrated Circuits

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Abstract—Power management in integrated circuits is critical and some ICs require voltages to be applied in a particular sequence. Integrated circuits consist of various distinct sub-circuits and power delivery to each of those circuits at the proper time is required for proper operation. Some examples are Subscriber line interface circuit (SLIC), switching voltage regulators, etc. Thus, startup delay circuits are necessary as they ensure the delivery of power to circuits at the appropriate time. Time delays are conventionally generated by resistor-capacitor pair but the time constant is very small, for higher time delay, we have to increase resistor-capacitor sizes which require more space and is not economical. In this paper, a new technique is proposed for the generation of sufficient time delays eliminating the need for larger resistor and capacitor combination. The proposed startup delay circuit is designed in 180 nm. CMOS process and simulated in LTSpice.

Index Terms—Analog integrated circuits, Added delay, Delay systems, Rail to rail amplifiers, Power management

I. INTRODUCTION

FOR some integrated circuits, supply voltages should be applied in a sequence. For example, it is often necessary for a switching regulator to be prevented from activating until all of its internal circuits are powered up and operational [1]. And thus, startup delay circuits are necessary. Startup delay circuits ensure the delivery of power to circuits at the appropriate time. Conventional startup delay circuits use resistor and capacitor pair to generate RC time constant which provides insufficient delay relative to the chip area covered or in other words, the delay is insufficient relative to the size of resistor-capacitor pair. Many circuits can generate a delay of few RC time constants [1] but for higher delay for example, in the order of few seconds, they rely on large resistor size.

Furthermore, as it is known that circuits with large components occupy a larger area, and consequently, the fabrication cost of the IC is increased, and thus, having a large capacitor and resistor size is not an economical solution. In this paper, a current-source-based delay sub-circuit is designed. The basic idea is to charge the capacitor with the help of a current source. The amount of delay can be controlled by the current supplied to the capacitor. The advantage of this circuit is that there is no need for large resistor-capacitor pair. The current

source can be easily implemented by a current mirror.

With this technique, a 1s delay is generated. Although this technique can generate large amounts of delay, for example, 10s, the 20s, etc., and that too with a capacitance of 10pF which is very small relative to the delay generated.

Fig. 1 Delay sub-circuit consisting of a capacitor charged by a current source with finite resistance.

Fig. 2 Voltage waveform across the capacitor charged by a current source.

II. DELAY SUB-CIRCUIT

The startup delay system is based on a current limiting sub-circuit consisting of a current source and a capacitor. The capacitor charges exponentially and the rate of charging can be controlled by the current source. In the majority of the circuits, a resistor is used for generating RC time constants but in integrated circuits, using large resistors is not feasible and besides, very large resistors and capacitors are required to generate a time constant for the target delay.

The equation for the voltage across the capacitor when it is charged by a constant current source is given by,

$$V(t) = \frac{1}{C} \int I dt + V(0)$$

Where $V(0)$ is the initial voltage across the capacitor.

The voltage across the capacitor rises exponentially and when this voltage is fed to the gate of a MOSFET, the timing depends on the threshold voltage of the MOSFET. When the gate-source voltage is less than the threshold voltage, the MOSFET turns OFF completely, and taking advantage of this, a delay signal can be generated.

The current source can be implemented by a current mirror. Reference current can be generated by a fixed bandgap reference and the current across the capacitor can be adjusted by adjusting the W/L ratios in the current mirror circuit.

Fig. 3 Delay sub-circuit with current mirror

Fig. 4 Schematic of the proposed startup delay circuit

III. STAGE 1: COMMON SOURCE STAGE

The voltage across the capacitor is applied to the gate of a PMOS transistor and its source and bulk are connected to the supply voltage (V_{CC}). The PMOS will remain ON until the gate-source voltage is greater than or equal to the threshold voltage. And

$$V_{GS} = V(t) - V_{CC}$$

Therefore, the transistor will be ON if

$$V(t) - V_{CC} \geq V_{TH}$$

In other words, the PMOS transistor will turn off if $V(t)$ is greater than $V_{TH} + V_{DD}$. In this case, PMOS turns off at around 0.61V and the output at node B goes to zero.

The NMOS transistor acts as an active load in the common source stage with resistance r_o . The current from the PMOS is given by,

$$I_D = \frac{\mu_p C_{ox}}{2} \left(\frac{W}{L} \right) \left[(V(t) - V_{CC} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] (1 + \lambda V_{DS})$$

The drain current flows through the output resistance ($r_{op} || r_{on}$) and generates an output voltage which is shown in figure 6.

IV. STAGE 2: CASCODE COMMON SOURCE STAGE

The output from Stage 1 is inverted and does not have a sharp transition as desired. And so, a high gain inverting stage like cascode common source stage is used. The gain for this stage is given by:

$$A_v \sim -g_{m4} (g_{m5} r_{o5} r_{o4} || g_{m7} r_{o7} r_{o6})$$

In addition to this, a 10pF capacitor is used at the output for the bypass to eliminate high-frequency spikes occurring at the startup as shown in figure 3.

Fig. 5 Delay signal of 1s generated at Vout

Fig. 6 The voltage across the capacitor C1 (Black), Voltage at node B (Red), and the output delay signal (Blue)

Fig. 7 Delay signal of 10s generated at Vout

V. SIMULATION RESULTS

The delay of 1s is successfully generated as shown in figure 5 with the current source 80nA, the capacitor size of 10pF, and supply voltage of 1V. The transistors' sizes in the proposed startup delay circuit design are listed in table 1. The current consumption of the system is shown in figure 8 which is a maximum of 800nA at startup.

Figure 7 is of 10s delay generated by the current across the capacitor of 25nA and capacitance of 25pF.

Fig. 8 Waveform showing the current drawn from the supply voltage

TABLE I
TRANSISTORS' SIZES IN THE PROPOSED CIRCUIT

Device	Parameter
M1	4.65u/0.18u
M2, M11	2u/0.18u
M3	0.18u/0.18u
M4, M5, M10	0.5u/0.18u
M6, M7, M8	1u/0.18u

VI. CONCLUSION

A startup delay circuit has been designed in 180 nm. CMOS process and simulated in LTSpice software. With this modified circuit, the need for large-size resistor-capacitor pair is eliminated and the delays in the order of few seconds can be easily generated with a very small amount of capacitance. Also, the current consumption is quite small i.e. 800nA maximum (in case of 1s delay generation with 80nA of current source).

REFERENCES

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