Preparation, Imaging, and Design Extraction of the Front-End-of-Line and Middle-of-Line in a 14 nm Node FinFET Device

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Abstract—This paper presents the first design reconstruction on the Front-End-of-Line and Middle-of-Line layers of a 14 nm node FinFET design. To accomplish this, a large region of interest within a custom designed 14 nm node ASIC device was delayered, imaged, and analyzed to reconstruct the GDSII design file and verify a 100% match to the golden GDSII design. This work leveraged previous developments in each stage of the front half of the cooperative Verification and Validation (V&V) workflow combined with new techniques and processes developed for processing 3D architecture FET devices. We have demonstrated the critical first step to performing a full V&V workflow on an advanced technology node device, starting from the fabricated silicon device to the design extraction. The process development knowledge gained while reaching this milestone will further accelerate future advancements toward providing trusted advanced technology node devices in a timely manner.

I. INTRODUCTION

The semiconductor industry global supply chain has created the enormous challenge of providing authentic, trusted microelectronics devices, a concern for both industry and government alike [1]. The untrusted foundry threat is not mitigated through cursory device electrical testing, requiring a much more robust and invasive analysis of the fabricated part and comparison to the golden design files for a high quantitative level of trust in a device through a cooperative Verification and Validation (V&V) workflow [2, 3]. While the V&V workflow demands a considerable amount of time, a diverse expertise in manpower, and a wide array of tools and facilities for execution, it can fully verify that a part is physically and functionally identical to the original design with a high degree of confidence. Exacerbating the intricacy of the workflow, microelectronics continue to scale in ever increasing complexity, packing more transistors into smaller areas, where new challenges will arise in the V&V workflow.

Furthermore, FinFET technology has added an even greater obstacle to overcome in the V&V workflow with the introduction of 3D transistors. Instead of planar, non-overlapping layers that can be serially delayered and imaged, FinFET devices offer unique challenges in sample preparation, imaging, and image analysis for design extraction. While some

techniques developed for higher technology node devices can still be applied to advanced technology nodes, new techniques and processes must be developed to meet the novel challenges presented.

In our previous efforts, we demonstrated the full design extractions of a 130 nm node region of interest (ROI) [4] and a 45 nm node ROI [5]. The focus of this study was on the sample preparation, imaging, and design extraction of the Front-End-of-Line (FEOL) and Middle-of-Line (MOL) layers of a 14 nm node FinFET device. Covering the first three of the five steps in the cooperative V&V workflow [6], this collective work is not only applicable for the V&V community, but failure analysis and other adjacent communities. The demonstration of sample preparation techniques, imaging, and design extraction of the FEOL/MOL in a 14 nm FinFET device are herein presented for the first time in peer reviewed literature.

II. IC DECOMPOSITION

The device investigated was a 14 nm node custom designed ASIC with 14 BEOL interconnect layers. The optical micrograph of the 2.12 mm x 2.12 mm decapsulated die (a), the secondary electron micrograph mosaic of the 480 μm x 300 μm ROI (b), and a highlighted subregion of the backside etched Active Silicon Fin layer are displayed in Figure 1.

Figure 1: Optical micrograph of the entire 2.12 mm x 2.12 mm die after decapsulation (a), the 480 μm x 300 μm region of interest (b), and a subregion of the ROI displaying the backside-etched Active Silicon Fin layer of a device functional group (c).

The process of assuring a manufactured chip's design begins with high precision material decomposition. The MOL includes the Contact A (CA) layer, the Contact B (CB) layer, and the Source/Drain stack (SD) layer. The FEOL contains the gate metal (GM) contact line layer and the Active Silicon Fin (AF) layer. The layout of the FEOL and MOL is displayed in the cross-sectional scanning transmission electron micrograph in Figure 2.

Figure 2: Cross-sectional scanning electron micrograph of the FEOL/MOL in a custom 14 nm node ASIC device. The notable feature layers are Contact A (CA), Contact B (CB), Source/Drain stack (SD), Gate Metal (GM) contact lines, and Active Silicon Fins (AF).

Leveraging previous sample preparation workflow developments, each layer of this device required either front side or back side delayering workflows in preparation for imaging [4]. In the front-side delayering workflow, the BEOL layers needed to be removed to approach the FEOL and MOL layers. The CA, CB, SD, and GM layers were all prepared in this manner. The top metal layer was first removed using a 1 μm diamond lapping film polish. After reaching the first copper layer, the device was delayered down to the M1 layer by iterating chemical-mechanical polishing (CMP) with colloidal silica to remove the interlayer dielectric (ILD) and ferric chloride (FeCl_3) etching to remove the copper interconnects. Several devices were processed to this layer in preparation for dual beam plasma focused ion beam (PFIB) scanning electron microscope delayering.

The top MOL layer (CA) was delayered in the PFIB-SEM utilizing a 15 kV acceleration voltage, a 27 nA ion beam emission current, and vapor injection of methyl nitroacetate (MNA) maintained at a chamber background pressure of approximately 1×10^{-5} mbar. The MNA vapor injection was employed to balance copper and ILD milling rates to evenly remove the M1 and V0 layers in 20 nm to 50 nm increments.

Additionally, another device was delayered with the PFIB-SEM to the CB layer. Delayering to the CB layer was particularly challenging because a portion of its features were in direct contact with CA features. The CA/CB overlap complicated SEM imaging that used either secondary or backscatter electrons, as the feature signals were almost indistinguishable from each other. This is reflected by the CA layer electron micrograph in Figure 3a, where a CA feature

(green) overlaps a CB feature (red) without a discernable boundary. Fortunately, this issue was solved by thinning the entire layer in the PFIB-SEM to remove most of the overlaid CA lines. When the CA lines were sufficiently thin, the buried CB layer features were distinguishable from the CA features. Subsequently, the CB layer was approached using the same PFIB settings used to reach the CA layer. Figure 3b depicts the same overlap of CA and CB features from the CB electron micrograph set, demonstrating an evident removal of the CA line within the green box. Just below the CA layer lies the SD layer, which is partially coplanar with the CB layer. Consequently, no additional sample preparation was required to image the SD layer.

Figure 3: Electron micrographs depicting a feature where the CA layer (green) and CB (red) layer overlap in the CA layer image set (a) and the slight change in feature morphology after the CA portion of the feature is removed in the CB image set (b).

Continuing with the FEOL, the GM layer was reached with a combination of PFIB delayering and wet etching. First, a new device previously delayered to M1 was milled down to the BEOL/MOL interface, employing the same PFIB settings as the CA layer. The CA and CB lines were thinned as much as possible while removing the majority of the surrounding ILD by using the same milling settings minus the MNA vapor injection. The sample was subsequently etched in a 30% hydrogen peroxide (H_2O_2) solution for three minutes at 60°C . This removed the exposed CA and CB lines, leaving empty trenches in their place. Lastly, the sample was further milled in the PFIB to thin the trenched surface enough to expose the gate metal electrode lines.

As the final layer, the AF layer containing the silicon fins was the only one in this workflow to be delayered from the backside. As an exceptionally small 3D structure, this layer would have been considerably problematic to expose from the topside. Additionally, achieving sufficient contrast in the SEM between the silicon fins, the dielectric, and the silicon substrate would be extremely challenging. Approaching this layer from the backside of the device, though, would ideally resolve the

contrast problem. Therefore, the backside of a device was mounted to a conductive silicon carrier and etched with xenon difluoride (XeF_2) vapor. Because this device was not fabricated on a silicon on insulator wafer, the XeF_2 etched away the entire Si substrate and Active fins. As a result, the trenches remaining from the backside etch provided sufficient contrast for SEM imaging and feature extraction.

III. IMAGE ACQUISITION

Each layer of the 14 nm node FEOL/MOL was imaged on a Raith 150 Chipscanner or a Raith eLINE Plus using the Everhart-Thornley (ET) secondary electron detector. Electron column acceleration voltages were set to 3 or 5 kV with either 30 or 60 μm apertures. Image tiles for all layers were acquired at 5k resolution and 2 nm/pixel, yielding a 10 μm x 10 μm image field. The overlap between image tiles was set to 10% to afford reliable stitching of the mosaic. Typically, using the In-Lens (IL) detector inside the electron column produces images of higher quality compared to those from the ET detector. However, subsequent image analysis demonstrated a clear advantage to using the ET over the IL for acquiring image sets. The location of the ET detector, unlike the IL detector, is at a significant angle from normal to the sample surface, which takes advantage of shadowing effects, thus resulting in enhanced image contrast. This advantage was especially apparent when imaging the AF layer. Figure 4 presents electron micrographs of the subregion

Figure 4: Electron micrographs (left) and golden GDSII overlays (right) of each FEOL/MOL layer in the blue highlighted box in Figure 1. The layers displayed are CA (a and b), CB and SD (c and d, red and blue, respectively), GM (e and f), and AF (g and h).

of the device ROI highlighted in the blue box in Figure 1. Figure 4a and b depict the CA layer and the golden GDSII polygon overlay. As both the CB and SD layers were acquired from the same image acquisition, Figure 4c displays the CB and SD layers and Figure 4d highlights their golden GDSII overlays in red and blue, respectively. Figure 4e and f show the GM layer and its GDSII overlay in orange. Finally, Figure 4g and h reveal the AF layer with the golden GDSII polygons in violet.

IV. FEOL AND MOL DESIGN EXTRACTION

A. Image Preprocessing with N2V

As it was apparent that there were significant contrast differences across the AF image set, polygon extraction was first tested to ensure acceptable quality. While a large majority of the fins could be extracted, there were still a considerable number of errors, the majority being bridges or gaps. While neither type was overwhelmingly dominant, it was concluded that the extraction could not be further optimized with standard image processing filters. The error checking process for the entire device ROI was extrapolated to yield approximately 12,000 errors, which would be a significant undertaking to perform manual verification and correction. Denoising was considered as an image pre-processing step to yield higher polygon extraction accuracy. Unfortunately, the standard image processing and denoising filters found in Fiji software (National

Figure 5: The raw image (a), post-N2V processed image (b) and respective pixel intensity histograms (c) of the blue rectangle region in Figure 1c.

Institute of Health) [7] did not yield significant gains. Therefore, the denoising deep neural net applications in the Fiji based CSBDeep deep learning toolbox were investigated. CSBDeep utilizes the TensorFlow framework to run a deep neural net training scheme called Noise2Void (N2V) [8]. Supplied with a few training and validation images, the N2V model training only required a few epochs, at 100 steps per epoch, with a neighborhood radius of 5 pixels. Figure 5 displays the blue highlighted subregion from Figure 1c with the raw image (a) and post-N2V processed image (b). At first glance, the raw and post-N2V processed images look similar, but slight changes are apparent. The histograms in Figure 5c, though, demonstrate that the changes were quite drastic. Instead of a smooth curve of pixel intensities where the noise complicates accurate polygon extraction, the post-N2V histogram has several distinct peaks and plateaus, which are useful for choosing filter thresholds and thus greatly enhancing polygon extraction quality.

The incredible impact of the N2V denoising on the polygon extraction accuracy is demonstrated in Table 1. From the whole functional group subregion in Figure 1c (green box), the raw images yielded a total of 171 errors, while images processed by N2V yielded only 30 errors. For the entire ROI, the N2V processing reduced the estimated number of errors to be manually checked from over 12,000 to approximately 2,100.

Table 1: Comparison of extraction error types and total errors between the raw images and the post-N2V processed images of the Figure 1c subregion.

Error Type	Number of Errors	
	Raw Images	N2V Images
Gap	137	16
Bridge	33	13
Missing	1	1
Unknown	0	0
Total	171	30

B. Layer Design Extraction

After the N2V deep neural net processing, the AF layer image set, along with the image sets for the rest of the FEOL and MOL layers were imported into the Pix2Net analysis software (P2N, MicroNet Solutions, Inc.). In P2N, each layer was stitched, manually aligned to the golden GDSII files, and prepared for polygon extraction by applying a myriad of image filters. The extracted polygon layer for each device layer was then error checked using a custom built homeomorphic error checking tool built upon topological equivalence and topological coverage concepts [5]. The homeomorphic error-checking tool has previously been demonstrated to significantly reduce error checking times while offering 100% accuracy in matching the golden GDSII design topology.

Each layer in the FEOL and MOL offered unique challenges in achieving an accurate design extraction. As depicted in Figure 3, Figure 4a, and Figure 4b, the CA layer is easily visible in the image layer, but so is the CB layer. Therefore, the full layer was extracted and then, using conditional filtering, split into layers where contacts were touching (CA/CB) and not touching (CA).

The golden GDSII CB polygons were subsequently subtracted from the CA/CB layer, leaving only partial CA polygons and small residuals. Finally, to complete the CA layer, the corrected CA/CB layer was added back to the first split CA layer by filtering out the residuals and verifying that each partial CA polygon was present as demonstrated in Figure 3. Extraction of the remaining layers was simpler due to material differences, sample preparation techniques, and the 3D nature layout of the FinFET. The CB/SD layer (Figure 4c and d) was first processed with a higher pixel intensity threshold to extract only the CB layer polygons. Afterwards, a separate polygon extraction used a lower threshold extracting both the SD and CB layers. The SD polygons were then isolated from this layer simply by subtracting the known CB polygons. No differential analysis of overlapping polygons was required for the CB/SD image set due to the original design layout, where the CB layer connected only to the GM layer and had no connections to the SD contacts. Since no features from other layers were visible in the image sets for either GM (Figure 4e and f) or AF (Figure 4g and h), differential analysis was not required to obtain the complete extracted polygon layers for the ROI.

C. Final Error Checks on the Extracted Design

After each extracted layer was aligned to its respective golden GDSII layer, the final design stack of the FEOL and MOL was complete, except for a final error check. Because each extracted layer was error checked against its golden GDSII and not the other extracted layers, small changes in extracted feature size and placement could result in errors. One such example is seen in Figure 6, where the center SD polygon (red) overlaps its GDSII polygon (yellow) and the CA GDSII polygon (green), thus satisfying topological equivalence. Although, when compared to the extracted CA polygon (blue), there is no overlap, which creates an open circuit in the device. These kinds of errors, while rare, demonstrate the cruciality of performing a final error-checking step on the full device stack before generating a GDSII.

Figure 6: A CA/SD final stack uncovered contact gap error (arrow) in the CA/SD final stack where the center extracted SD polygon (red) overlaps the GDSII polygons for SD (yellow) and CA (green) but not the extracted CA polygon (blue).

D. Full ROI FEOL/MOL Design

Once the whole extracted design was completely error checked, it was then exported from P2N into a GDSII file.

Figure 7: The extracted designs for the FEOL and MOL of a custom 14 nm node ASIC device: full ROI (a), the subregion of the extracted design matching the subregion in Figure 1c (b), and a detailed subregion of the extracted design from the blue box in Figure 1c (c). The depicted layers are as follows: AF (green), SD (yellow), GM (brown), CA (red), and CB (blue).

Figure 7 depicts the final extracted FEOL and MOL of the ROI on the 14 nm node device, showing extracted layers for AF (green), SD (yellow), GM (brown), CA (red), and CB (blue).

V. CONCLUSIONS

In this work, we have demonstrated the decomposition, imaging, polygon extraction, and FEOL/MOL design recovery of a ROI on a 14 nm node device for the cooperative Verification and Validation workflow. Recent developments in sample preparation, imaging, design extraction, and error checking have culminated in the ability to finally extract the design of a large ROI on a modern technology node FinFET device in a relatively short period of time. Future advancements will enable even

shorter processing times, increased tool automation, and a reduced need for operator intervention for improved and timely processing of entire advanced technology node devices in the Verification and Validation workflow.

ACKNOWLEDGEMENTS

This research was sponsored by the Sensors Directorate of the Air Force Research Laboratory at Wright Patterson Air Force Base in Dayton, OH as part of the OUSD Trusted and Assured Microelectronics Program.

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