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SUBMISSION DATE / POSTED DATE

02-08-2021 / 03-08-2021

CITATION

Thambidurai, Chembiyan (2021): Reference Spur Reduction in Sampled-loop filter PLLs by Oversampling. TechRxiv. Preprint. <https://doi.org/10.36227/techrxiv.15094008.v1>

DOI

[10.36227/techrxiv.15094008.v1](https://doi.org/10.36227/techrxiv.15094008.v1)

Reference Spur Reduction in Sampled-loop filter PLLs by Oversampling

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Abstract—A technique to eliminate reference spurs in both Integer-N and Fractional-N charge pump phase locked loops (PLLs) based on an oversampled loop filter architecture is proposed. A rigorous analysis of the performance of the proposed technique in the presence of implementation non-idealities is also presented. It is shown through analysis and simulations that the proposed technique, in addition to completely eliminating reference spurs, adds an insignificant area and power overhead when applied to Integer-N PLLs and less than 6% increase in area and power in case of Fractional-N PLLs.

I. INTRODUCTION

One of the major problems in charge pump PLLs is reference spurs which arise from its periodic sampling nature in the presence of phase frequency detector (PFD) and charge pump (CP) non-idealities [1], [2], [3], [4], [5], [6]. Due to PFD/CP non-idealities, the charge pump injects a finite current into the loop filter ($Z(s)$) at the beginning of every reference cycle in the steady state. Even though the average value of the current is zero, the CP current injected into the loop filter impedance ($Z(s)$) causes sudden voltage excursions which manifests as reference spurs at the VCO output. Reference Spurs increase period jitter and out of band emissions of the PLL and to filter these spurs, the bandwidth of the PLL is reduced. A reduced bandwidth results in poor rejection of VCO Phase noise and an increased settling time. Hence reducing reference spurs is a major concern when designing wide bandwidth PLLs.

One popular approach to reduce reference spurs in CP-PLLs is the sampled loop filter (SLF) technique [3], [6], [7], [8] shown in Fig.1. By sampling the charge injected from CP onto a sampling capacitor (C_s) and then deliver the charge after a delay T_D (when $i_{cp}(t) = 0$), the loop filter (and hence the VCO) does not 'see' the sudden voltage variations caused by the transient CP current. Thus the reference spurs are reduced in a SLF PLL. Fig.2 shows the simulated phase noise of the SLF-PLL and a conventional Fractional-N CP-PLL with a 5% CP current mismatch. The reference spurs in the SLF PLL is ≈ 13 dB lower than the conventional PLL.

However the charge injection from the sampling switch in the SLF-PLL can still produce significant reference spurs. Using dummy switches alongside the actual sampling switch can reduce the reference spurs to some extent. Since this relies on circuit techniques, a complete elimination is not practically feasible due to device mismatches. In this work a technique to completely eliminate reference spurs in SLF-PLL

Fig. 1. Sampled loop filter PLL architecture

Fig. 2. PLL output phase noise before and after applying SLF technique

by using a sampling clock of higher frequency is proposed. The proposed technique, when applied to Integer-N PLLs eliminates reference spurs without any additional area or power overhead and in the case of Fractional-N PLLs, with a marginal increase ($< 6\%$) in area and power. Furthermore mathematical analysis (corroborated by simulation results) of the performance of the techniques in the presence of implementation non-idealities like jitter of the over-sampled clock is also presented.

Section II discusses the proposed technique in Integer-N and Fractional-N PLLs and the implementation details. A detailed analysis and comparison of spur levels is discussed in Section III. Section IV presents the test bench and the simulation results for the proposed techniques. The performance in the presence of oversampling clock jitter is then discussed in Section V. The conclusions are summarised in Section VI.

II. REFERENCE SPUR REDUCTION BY OVERSAMPLED LOOP FILTER (OSLF) TECHNIQUE

The source of reference spurs in SLF PLL is the periodic charge injection from the sampling switch into the loop filter. The proposed solution in this work is to increase the frequency of the sampling switch control signal by M times the reference frequency. By doing so, the reference spurs will be absent upto Mf_r . The problem now, is to derive the high frequency switch control signal S_{os} without adding much to the complexity or power consumption of the PLL.

1) *Integer-N PLLs*: In case of Integer-N PLLs, the VCO frequency is an integer multiple of the reference frequency ($f_{vco} = Nf_r$). Therefore the higher sampling frequency

Fig. 3. Proposed over-sampled loop filter architecture in an Integer-N PLL

clock Mf_r can be derived from the VCO clock using a frequency divider. But adding an additional divider increases the power consumption as it operates at the VCO frequency. So the feedback divider can be split into two parts and the high frequency signal can be derived from the feedback divider path as shown in Fig.3. The divider is split into N_1 and M . The value of N_1 can be computed as

$$Mf_r = f_{vco}/N_1 \rightarrow N_1 = \frac{N}{M} \quad (1)$$

2) *Fractional-N PLLs*: In case of Fractional-N PLLs, one possible approach to generate the high frequency sampling clock is to split the Fractional-N divider in the feedback path into two parts M and $N_1.f_1$ as shown in Fig.4, where $N_1.f_1 = N.f/M$. The output of the fractional divider $N_1.f_1$ gives the oversampling clock Mf_r . There are two problems with this

Fig. 4. Generating the oversampling clock from the feedback divider in a Fractional-N PLL

approach, 1) Like any Fractional-N clock, the oversampling clock period changes every cycle and is only equal to Mf_r on

Fig. 5. Proposed OSLF architecture with MPLL in a Fractional-N PLL

an average and 2) The $\Sigma - \Delta$ noise of the Fractional-N PLL is now increased as the quantization step size seen at the PFD input increases by $20\log_{10}(M)$.

To avoid the aforementioned problems, the oversampling clock Mf_r is derived from the reference clock directly using a frequency multiplying PLL (MPLL) as shown in Fig.5. As it is later shown in Section V, the jitter of the MPLL is not a major concern and hence the MPLL can be realised with much lower power (using ring oscillator based VCO) and smaller area compared to the Fractional-N PLL. The OSLF technique is used in the MPLL as well to ensure the oversampling signal Mf_r does not contain any reference spurs. The output of the MPLL is chosen to be twice the oversampling frequency $f_{mvco} = 2Mf_r$, so that the signal S_{os} has a 50% duty cycle.

3) *Choosing the delay T_D* : The delay should be chosen such that the signal S_{os} is 'low' at the beginning of the reference cycle when the CP current is not zero as shown in the shaded region in Fig.6.(a). Let Δ_{max}^1 be the maximum phase excursion seen at the PFD input in the steady state. Then the signal S_{os} should be delayed by T_D seconds such that $T_D > \Delta_{max}$. Furthermore, since the frequency of the signal S_{os} is much higher than the reference frequency, it should be ensured that the off-time of S_{os} , $T_{off} = T/2M > \Delta_{max} + T_m$, where T_m is an additional time margin given to ensure that S_{os} does not go 'high' in that region. This condition puts an upper limit on the value of M .

In case of Integer-N PLLs, the delay T_D can be rounded-off to the nearest integral multiple of $0.5T_{vco}$ and realised using a series of flip flops clocked at the alternate edges of VCO clock as shown in Fig.6.(b). The output of the flip-flops change at

¹ Δ_{max} can be estimated from the behavioural level simulations of the PLL.

the oversampling frequency of Mf_r and the power consumed in the delay element will be a small fraction of the frequency divider (N_1 in Fig.3) in the feedback path.

In case of Fractional-N PLLs the steady state phase error is much higher in comparison to Integer-N PLLs. The delay T_D can be realised in a much simpler way by exploiting the multi-stage ring oscillator in the MVCO. In this work, the MVCO is designed as a four stage differential ring oscillator running at $2Mf_r$ and thus the oversampling clock Mf_r can be delayed in steps of $T/16M$. The delay T_D can be rounded off to the nearest multiple of $T/16M$ and then realised using a single flip-flop clocked by one of the eight appropriate phases (ϕ_x) of the MVCO as shown in Fig.6.(c). The same sampling signal can be used in the MPLL as well to save power.

Fig. 6. a) Timing diagrams of reference and the switch control signal S_{os} and Implementation details of delay T_D in b) Integer-N mode and c) Fractional-N mode

III. SPURS IN SLF VS OSLF

Fig. 7. Switch control signals and current injected into the loop filter in SLF and OSLF techniques

After applying the OSLF technique, the reference spurs up to Mf_r are absent and the highest spur level occurs at Mf_r . It is instructive to compare the highest spur level in OSLF

with the reference spur at f_r in the SLF technique. The charge injection current can be modeled as two impulses of opposing polarity spaced T_{on} seconds apart as shown in Fig.7. In both SLF and OSLF technique the duty cycle of the switch control signal S/S_{os} is chosen to be 50%. In case of SLF technique $T_{on} = T/2$ and in case of the OSLF technique $T_{on} = T/2M$. This is done to ensure that the average ON resistance of the switch is same in both the techniques [12] and also the even harmonics will be absent in spectrum. The spectrum of the injected current into the loop filter impedance $Z(s)$ in case of the SLF and OSLF technique is given by

$$S_{i,SLF}(f) = (2Q_{inj}f_r)^2 \sum_k \delta(f - (2k+1)f_r) \quad (2)$$

$$S_{i,OSLF}(f) = (2MQ_{inj}f_r)^2 \sum_k \delta(f - (2k+1)Mf_r) \quad (3)$$

The reference spur at the PLL output can be shown to be [1], [2], [3], [4]

$$S_{\phi}(kf_r) = 10 \log_{10} \left(S_i(f) \left| \frac{Z(kf_r)K_v}{2kf_r} \right|^2 \right) \quad (4)$$

The highest spur level difference in both the techniques can be computed from Eq.(2), Eq.(3) and Eq.(4)

$$S_{\phi,OSLF}(Mf_r) - S_{\phi,SLF}(f_r) = -20 \log \left(\frac{Z(f_r)}{Z(Mf_r)} \right) \quad (5)$$

$$\approx -20P \log(M) \quad (6)$$

where $P = N_p - N_z$ is the difference between the number of poles (N_p) and zeroes (N_z) of the impedance $Z(s)$. Thus the highest spur level in OSLF technique is $20P \log(M)$ lower than the highest spur in SLF technique.

IV. SIMULATION RESULTS

A 2.4 GHz output PLL with a $f_r = 20$ MHz reference frequency as shown at block level in Fig.8 is simulated to validate the proposed technique. The PLL is a Type-II PLL with two poles at DC, a stabilising zero and two high frequency poles after the unity gain bandwidth to reduce spurs. The parameters of the PLL are chosen to optimise the integrated jitter at the PLL output. The UGB (f_u) of the Fractional-N PLL is $f_u \approx 400$ kHz. The zero is placed at $f_z = 100$ kHz, and the poles are at $f_{p1} = 1.67$ MHz and $f_{p2} = 8$ MHz. The phase margin of the PLL is $\approx 60^\circ$. The nominal divide value in Integer-N mode is $N = 120$ and in Fractional-N mode $N.f = 120.333$. The VCO gain is $K_v = 200$ MHz/V.

An offset is introduced in the PFD/CP characteristics by adding a mismatch in the reset path of the UP and DN signals to reduce the $\Sigma - \Delta$ noise folding into the in-band due to the PFD/CP non-linearity [3], [9], [10], [11]. The MPLL on the other hand was designed to keep its area and power minimum. So the UGB of the MPLL is chosen to the maximum value of $f_r/10 = 2$ MHz. The value of M is chosen to be 4.

All the blocks in the PLL are modeled behaviorally except the loop filter (including the CMOS switches) of the Fractional-N PLL and the MPLL, which are at schematic level. The devices used in the sampling switch are from the UMC 180 nm CMOS process. A 5% mismatch in the CP current is modeled

remains the same. The current injected into the loop filter can be modelled as

$$i_{inj}(t) = Q_{inj} \sum_k p\left(t - \frac{kT}{M} - e(t)\right) \quad (7)$$

where $p(t) = \delta(t) - \delta(t - T/2M)$ and $e(t)$ is the jitter of the MPLL clock characterised by a probability density function $f_e(e)$. The spectrum of the injected current is given by [4]

$$\frac{Q_T^2}{T^2} \sum_k \delta(f - kMf_r) |P(f)C(f)|^2 + \frac{Q_T^2}{T} (1 - |E(f)|^2) |P(f)|^2$$

where $|P(f)| = |1 - e^{-j\pi fT/M}|$ and $E(f)$ is the characteristic function [15] of the jitter probability density function. In the absence of jitter $E(f) = 1$ and the current injected into loop filter will contain only spurs at multiples of Mf_r . The above expression shows that in the presence of jitter, the spurs at kMf_r undergo some kind of filtering and an additional noise is injected into the loop filter. This is expected because randomising the positions of the injected current pulses reduces its periodicity and the energy removed from the tones is distributed as noise [4]. To quantify the effect, the charge injected from the switches is estimated from a transient simulation of the PLL and the output phase noise due to the oversampling clock jitter is estimated by modelling the jitter of the MPLL as a gaussian random variable with a variance of 50 ps. The maximum phase noise contributed by the MPLL jitter at the Fractional-N PLL's output is -275.5 dBc/Hz as shown Fig.11, which is several orders of magnitude smaller than the in-band phase noise (≈ -90 dBc/Hz) of the PLL. Hence the jitter of the MPLL is not a major concern.

Fig. 11. Output phase noise due to jitter in the oversampling clock

VI. CONCLUSION

Reference spurs in CP PLLs can be eliminated in both Fractional-N and Integer-N PLLs by applying the proposed OSLF technique. In case of Integer-N PLLs, it was shown that reference spurs can be completely eliminated by an insignificant power and area overhead. In case of Fractional-N PLLs, the reference spurs can be eliminated with a slight ($< 6\%$) increase in power and area. A rigorous analysis to compare the spurs in both the techniques showed that the proposed OSLF technique offers much lower spur levels compared to SLF technique. Finally it is also shown that the jitter of the oversampling clock has insignificant effect on the phase noise of the main PLL.

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