Spin Wave Based Approximate 4:2 Compressor

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In this paper, we propose an energy efficient SW based approximate 4:2 compressor comprising a 3-input and a 5-input Majority gate. We validate our proposal by means of micromagnetic simulations, and assess and compare its performance with one of the state-of-the-art SW, 45 nm CMOS, and Spin-CMOS counterparts. The evaluation results indicate that the proposed compressor consumes 31.5% less energy in comparison with its accurate SW design version. Furthermore, it has the same energy consumption and error rate as the approximate compressor with Directional Coupler (DC), but it exhibits 3x lower delay. In addition, it consumes 14% less energy, while having 17% lower average error rate than the approximate 45 nm CMOS counterpart. When compared with the other emerging technologies, the proposed compressor outperforms approximate Spin-CMOS based compressor by 3 orders of magnitude in term of energy consumption while providing the same error rate. Finally, the proposed compressor requires the smallest chip real-estate measured in terms of devices

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I. INTRODUCTION

The information technology revolution has led to a rapid raw data rapid increase, which processing calls for high performance computing platforms¹. Up to date, downscaling Complementary Metal Oxide Semiconductor (CMOS) has been effective to satisfy these requirements, however, Moore's law has reached its near economical end as CMOS feature size reduction is becoming increasingly difficult due to leakage, reliability, and cost walls². As a result, different technologies have been investigated to replace CMOS such as graphene devices³, memristor⁴, and spintronics⁵. In this paper, we chose to study one type of spintronics technology, the Spin Wave (SW) technology, which appears to open the way towards the most energy efficient digital computing paradigm⁶⁻⁹. SW based computing is promising for three main reasons⁶⁻⁹: 1) it has ultra-low energy consumption potential because it does not rely on electrons movements but just on their spinning around the magnetic field orientation⁶⁻⁹, 2) it is highly scalable because SW's wavelength (which is the distance between two electrons that exhibit the same behavior) can reach the nanometer scale⁶⁻⁹, and 3) it has an acceptable delay⁶⁻⁹. As a consequence of these promising features, different researcher groups have made use of SW interaction to build logic gates and circuits.

The first experimental SW logic gate is an inverter, designed by utilizing a Mach-Zehnder interferometer¹⁰. Moreover, the Mach-Zehnder interferometer has been used to build a single output Majority, (N)AND, (N)OR, and X(N)OR gates¹⁰, while multi-output SW logic gates have been introduced in^{9,11,12}. Furthermore, multi-frequency logic gates that enhance SW computing and storage capabilities have been proposed in^{8,13}, and wavepipelining has been achieved with pulse mode operation in the SW domain by utilizing four cascaded Majority gates¹⁴. In addition, different SW circuits have been also demonstrated at conceptual level¹⁵, simulation level^{7,16}, and practical millimeter scale prototypes¹⁷. All the aforementioned logic gates and circuits were designed to provide accurate results; however, many applications such as multimedia processing and social media are error-tolerant, and within certain error limits, they still function correctly¹⁸. Hence, those applications can benefit from approximate computing circuits, which save significant energy, delay, and area.

Based on the previous discussion on the SW technology potential and the approximate computing benefits one can conclude that SW approximate circuits are of great interest. In view of this observation, and given that multiplication is heavily utilized in error tolerant

applications, and fast state-of-the-art multipliers are build with 4:2 compressors¹⁹ we introduce in this paper a novel approximate SW 4:2 compressor. The paper main contributions can be summarized as follows:

- Developing and designing an approximate SW 4:2 compressor: We propose an approximate 4:2 compressor consisting of two Majority gates that provides an average error rate of 31%.
- Enabling directional couplers free approximate circuit design: We demonstrate that Majority gates can be directly cascaded, i.e., without amplitude normalization of domain conversion, to form a 4:2 compressor with no additional average error rate penalty.
- Validating the proposed 4:2 Compressor: We demonstrate by means of MuMax3 micromagnetics simulations the correct functionality of the proposed approximate 4:2 compressor.
- Demonstrating the superiority: The proposed approximate SW 4:2 Compressor performance is assessed and compared with state-of-the-art SW, 45 nm CMOS, and Spin-CMOS counterparts. The evaluation results indicate that the proposed compressor saves 31.5% energy in comparison with the accurate SW design, whereas it has the same energy consumption and error rate as the approximate compressor with Directional Coupler (DC), but while being 3x faster. In addition, the proposed compressor consumes 14% less energy while providing 17% less error rate when compared with the approximate 45 nm CMOS counterpart. Moreover, the proposed compressor outperforms approximate Spin-CMOS equivalent design by 3 orders of magnitude in terms of energy while having the same error rate. Finally, the proposed compressor requires the smallest chip real-estate.

The rest of the paper is organized as follows. Section II explains SW computing background. Section III introduces the proposed approximate 4:2 compressor and Section IV provides inside on the simulation setup and results. Section V reports performance evaluation and comparison with state-of-the-art data. Section VI concludes the paper.

II. SPIN WAVE BASED TECHNOLOGY FUNDAMENTAL AND COMPUTING PARADIGM

The magnetization dynamics caused by the magnetic torque when the magnetic material magnetization is out of equilibrium is captured by the Landau-Lifshitz-Gilbert (LLG) equation⁶:

$$\frac{d\vec{M}}{dt} = -|\gamma|\mu_0 \left(\vec{M} \times \vec{H}_{eff} \right) + \frac{\alpha}{M_s} \left(\vec{M} \times \frac{d\vec{M}}{dt} \right), \quad (1)$$

where γ is the gyromagnetic ratio, μ_0 the vacuum permeability, M the magnetization, M_s the saturation magnetization, α the damping factor, and H_{eff} the effective field, which consists of the external field, the exchange field, the demagnetizing field, and the magneto-crystalline field.

Equation (1) has wave-like solutions under small magnetic disturbances, which are called Spin Waves (SWs) and are the collective excitations of the magnetization within the magnetic material⁶. A SW, as any other wave, is described by its amplitude A , phase ϕ , wavelength λ , wavenumber $k = \frac{2\pi}{\lambda}$, and frequency f as graphically presented in Figure 1a)⁶. SW frequency and wavenumber are linked by the so called dispersion relation, which plays a fundamental role during the SW circuit design process⁶.

Generally speaking, information can be encoded in SW amplitude and phase at different frequencies^{6,8}, while the interaction between SWs coexisting in the same waveguide is governed by the interference principle. Figure 1b) presents two SWs interaction situations: if they have the same phase, i.e., $\Delta\phi = 0$, they interfere constructively resulting in a larger amplitude SW, whereas if they have different phases, i.e., $\Delta\phi = \pi$, they interfere destructively resulting in a diminished amplitude SW. Due to their very nature, SWs provide natural support for Majority function evaluation as the interference of an odd number of SWs emulates an Majority decision. For instance, if 3 same amplitude, frequency, and wavelength SWs interfere, the result is a 0 phase SW (logic 0) if no more than one of them has a π phase, and in a π phase SW (logic 1) otherwise, which is equivalent with the behavior of a 3-input Majority gate. Note that a CMOS 3-input majority gate implementation requires 18 transistors, while in SW technology it only requires one waveguide. We note that if the SWs have different A , λ , and f , their interaction results in more sophisticated interferences, which might open different SW based computation paradigms. However, in this paper, we

FIG. 1. a) Constructive and Destructive Interference. b) Spin Wave Device.

only consider the interaction of SWs with phase encoded information, i.e., logic 0 and logic 1 are represented by 0 and π phase, respectively.

Figure 1c) presents a SW device, which consists of an excitation region I , a waveguide B , a functional region FR , and a detection region O ^{6,20}. SW can be excited by means of, e.g., microstrip antennas, magnetoelectric cells, in region I ^{6,20}. B can be made out of different materials such as Permalloy, Yttrium iron garnet, CoFeB, which must be properly chosen as it has a direct impact on the SW properties, and propagation^{6,20}. SWs can be amplified, normalized or interfere with other SWs within FR , and the output is detected at O by using similar or different components than the one utilized in the excitation region^{6,20} by means of phase and threshold detection techniques⁶. Phase detection is based on comparing the resulted SW phase with a predefined phase. For instance, if the output SW has a phase difference $\Delta\phi = 0$, the output is logic 0, whereas the output is logic 1 if the phase $\Delta\phi = \pi$. Threshold detection relies on the comparison of the output SW amplitude with a predefined threshold value T , i.e., if the SW amplitude is larger than T , the output is logic 1, and 0, otherwise^{6,20}.

FIG. 2. Conventional 4:2 Compressor.

III. SW APPROXIMATE 4:2 COMPRESSOR

For many state-of-the-art applications, e.g., artificial neural network, machine vision, detecting events such as visual surveillance and people counting, which heavily rely on multiplications the availability of fast multipliers is essential. Wallace or Dadda tree multipliers are the fastest and can perform a multiplication within 2 clock cycles. They embed 3 stages, i.e., partial product generation, reduction tree, and carry propagation adder. In an n -bit multiplier the first stage requires n^2 gates to produce the partial products matrix, the second stage provides a logarithmic depth reduction of n n -bit numbers to two numbers without carry propagation, and the final stage is a carry propagate adder that sums-up the reduction tree outputs²¹. The n to 2 reduction has been traditionally done by means of Full and Half adders but n :2 compressors based reduction trees can be shallower and have a more regular layout²¹. Thus, most of the state-of-the-art CMOS implementations make use of 4:2 compressors for which faster than 2 cascaded FA implementations exists^{19,22,23}. Essentially speaking, a 4:2 compressor processes 4 dots in the same column and generate one dot in the current column and a carry to the next column. To properly preserve the value carried by the inputs, after a FA delay, the 4:2 compressor generates a transport to the next column and receives a transport from the previous position, which it further process to generate the sum and a carry for the next column. Thus, the compressor has 5 inputs (one of them coming from the previous column) and 2 real outputs and one intermediate transport to the next column. Given that multiplication dominated error tolerant applications exist, e.g., multimedia processing and social media¹⁸, approximate CMOS 4:2 compressors have been proposed¹⁹, which enable significant energy consumptions and area saving.

Figure 2 presents the conventional structure of an accurate SW 4:2 compressor, which

consists of 2 full adders. When applied in column i of the partial product matrix it processes 4 dots in that column and a Carry-in C_{in} reported by a 4:2 compressor in column $i-1$, and generates 3 outputs, 1 intermediate transport C_{o1} that serves as C_{in} for a counter in column $i+1$, the Sum S and Carry-out C_{o2} . A straightforward SW 4:2 compressor implementation can be built using the SW full adder proposed in¹⁶, which provides accurate results with acceptable delay and energy efficiency as further discussed in Section V. However, as previously mentioned, many applications are error tolerant, and work properly within certain error limits¹⁸. Therefore, by enabling approximate computing, a more energy efficient SW 4:2 compressor can be made.

The straightforward implementation of a SW approximate 4:2 compressor can be done by means of the two approximate SW full adder proposed in²⁴. This requires the cascading of two Full Adders (FAs), which cannot be performed straightforward because different FA input combinations generate different output SW strengths⁷. To solve this issue, and make the compressor functions correctly a directional coupler is required⁷ to normalize the output of the first FA before passing it to the second FA. Figure 3 presents the approximate compressor obtained by cascading two approximate FAs by means of a normalizer (directional coupler). However, the directional coupler induces substantial delay and area overheads, which makes working without it desirable. Therefore, we propose the novel directional coupler free approximate compressor depicted in Figure 4. The behaviour of the 2 directly cascaded FAs is now obtained with a 3-input Majority gate and a 5-input Majority gate computing $C_{o1} = MAJ(X, Y, C_i)$, and $S = \overline{C_{o2}} = \overline{MAJ(I_1, I_2, I_3, \overline{I_4}, \overline{C_{in}})}$, respectively. The proposed 4:2 approximate compressor generates C_{o1} without any error, and S and C_{o2} with an average error rate of 31.25%, and 18.75%, respectively. Table I presents the truth table of the accurate 4:2 compressor C_{o1} , S_{ac} , and C_{o2ac} , the approximate 4:2 compressor without directional coupler C_{o1} , C_{o2ap1} , and S_{ap1} , and the approximate 4:2 compressor with directional coupler C_{o1} , C_{o2ap2} , and S_{ap2} . As it can be observed from the Table, approximate 4:2 compressors with and without directional coupler provide the same average error rate of 25% because S_{ap1} , and C_{o2ap1} have an error rate of 37.5%, and 12.5%, respectively, whereas S_{ap1} , and C_{o2ap1} have an error rate of 31.25%, and 18.75%, respectively. Note that the erroneous outputs values in the Table are underlined and typeset in bold to highlight them.

To achieve proper functionality for the structure in Figure 4, the waveguide width must be smaller or equal to the SW wavelength to simplify the interference patterns, all SWs must

FIG. 3. Approximate Spin Wave Based FA with Normalizer.

be excited at the same amplitude, wavelength, and frequency, and the waveguide lengths must be accurately computed as they determine the SWs interaction modes. For example, if SW constructive (destructive) interference is envisaged for in phase (out of phase) SWs, the distances must be equal with $n \times \lambda$, where $n = 0, 1, 2, \dots$; this is the case for d_1 , d_3 , d_4 , and d_6 in Figure 4. In contrast, if SW constructive (destructive) interference is envisaged for out of phase (in phase) SWs, the distances must be equal with $(n + 1/2) \times \lambda$; this is the case for d_2 and d_5 in Figure 4. On the output side, it is important to detect the output at specific position, i.e., if the desired output is the output itself, which is the case for C_{o1} in Figure 4, d_7 must be equal with $n \times \lambda$, whereas if the inverted output is desired, the distance must be equal with $(n + 1)/2 \times \lambda$. Moreover, the outputs must be detected as near as possible from

FIG. 4. Approximate Spin Wave Based FA without Normalizer.

the last interference point to capture large SW amplitude.

The proposed SW 4:2 compressor operation principle is as follows:

- C_{o1} : SWs are excited at I_1 , I_2 , and I_3 with the same amplitude, wavelength, and frequency at the same time moment. The I_2 SW interfere constructively or destructively with I_3 SW depending on their phase difference, the resulted SW propagates through the waveguide, and subsequently interferes with the I_1 SW. The resulted SW is captured at the output C_{o1} based on phase detection.
- S and C_{o2} : I_2 SW interferes constructively or destructively with I_3 SW depending on their phase difference, and the resulted SW propagates through the waveguide to interfere with the SWs excited at I_4 and C_{in} . The resulted SW propagates, and subsequently interferes with the I_1 SW. Finally, the resulted SW is captured at the outputs S and C_{o2} based on the threshold detection.

IV. SIMULATION SETUP AND RESULTS

In order to validate the proposed structure by MuMax3²⁵, we made use of the parameters specified in Table III²⁶. In addition, we assumed waveguide thickness and width of 1 nm and

TABLE I. Accurate and Approximate SW-based 4:2 Compressor.

$C_{in}I_4I_3I_2I_1$	C_{o1}	C_{o2ac}	C_{o2ap1}	C_{o2ap2}	S_{ac}	S_{ap1}	S_{ap2}
00000	0	0	0	<u>1</u>	0	<u>1</u>	0
00001	0	0	0	0	1	1	1
00010	0	0	0	0	1	1	1
00011	1	0	0	0	0	<u>1</u>	<u>1</u>
00100	0	0	0	0	1	1	1
00101	1	0	0	0	0	<u>1</u>	<u>1</u>
00110	1	0	0	0	0	<u>1</u>	<u>1</u>
00111	1	0	0	0	1	1	1
01000	0	0	<u>1</u>	<u>1</u>	1	<u>0</u>	<u>0</u>
01001	0	1	1	1	0	0	0
01010	0	1	1	1	0	0	0
01011	1	0	0	0	1	1	1
01100	0	1	1	1	0	0	0
01101	1	0	0	0	1	1	1
01110	1	0	0	0	1	1	1
01111	1	1	<u>0</u>	<u>0</u>	0	<u>1</u>	<u>1</u>
10000	0	0	<u>1</u>	<u>1</u>	1	<u>0</u>	<u>0</u>
10001	0	1	1	1	0	0	0
10010	0	1	1	1	0	0	0
10011	1	0	0	0	1	1	1
10100	0	1	1	1	0	0	0
10101	1	0	0	0	1	1	1
10110	1	0	0	0	1	1	1
10111	1	1	<u>0</u>	<u>0</u>	0	<u>1</u>	<u>1</u>
11000	0	1	1	1	0	0	0
11001	0	1	1	1	1	<u>0</u>	<u>0</u>
11010	0	1	1	1	1	<u>0</u>	<u>0</u>
11011	1	1	1	1	0	0	0
11100	0	1	1	1	1	<u>0</u>	<u>0</u>
11101	1	1	1	1	0	0	0
11110	1	1	1	1	0	0	0
11111	1	1	1	<u>0</u>	1	<u>0</u>	1

50 nm, respectively, to guarantee high SW group velocity. Furthermore, we excite the SWs with Gaussian pulses with 500 ps sigma modulated at 10 GHz to save energy, guarantee the excitation of single frequency SWs, and achieve high group velocity. From the SW dispersion relation, at 10 GHz, we determine k as being $36.9 \text{ rad}/\mu\text{m}$, which results in a $\lambda = 2\pi/k = 170 \text{ nm}$. As discussed in Section III, the distances $d_1, d_2, \dots, d_8$ should be equal to integer multiples of λ , and are: $d_1 = 170 \text{ nm}$ ($n = 1$), $d_2 = 595 \text{ nm}$ ($n = 3.5$), $d_3 = 1190 \text{ nm}$ ($n = 7$), $d_4 = 510 \text{ nm}$ ($n = 2$), $d_5 = 595 \text{ nm}$ ($n = 3.5$), $d_6 = 1190 \text{ nm}$ ($n = 7$), $d_7 = 170 \text{ nm}$ ($n = 1$), $d_8 = 85 \text{ nm}$ ($n = 0$), and $d_9 = 170 \text{ nm}$ ($n = 1$).

Figure 5 presents C_{o1} MuMax3 simulation results for $\{I_1, I_2, I_3\} = \{0,0,0\}, \{0,0,0\}, \{0,0,1\}, \{0,1,0\}, \{0,1,1\}, \{1,0,0\}, \{1,0,1\}, \{1,1,0\}$, and $\{1,1,1\}$. One can observe in the Figure that C_{o1} is detected correctly. $C_{o1} = 0$ for $\{I_1, I_2, I_3\} = \{0,0,0\}, \{0,0,1\}, \{0,1,0\}$, and $\{0,1,1\}$, whereas $C_{o1} = 1$ for $\{I_1, I_2, I_3\} = \{1,0,0\}, \{1,0,1\}, \{1,1,0\}$, and $\{1,1,1\}$, as it should, for a

TABLE II. Simulation Parameters.

Parameters	Values
Waveguide Material	$Fe_{60}Co_{20}B_{20}$
Saturation magnetization M_s	1.1×10^6 A/m
Perpendicular anisotropy constant k_{ani}	0.83 MJ/m ³
Damping constant α	0.004
Exchange stiffness A_{exch}	18.5 pJ/m

FIG. 5. Normalized 4:2 Compressor Output C_{o1} .

0.4 ns reading window starting 1.80 ns after the input application.

Table III presents the normalized magnetization of the 4:2 approximate compressor outputs C_{o2} and S for all possible input combinations, i.e., $\{C_{in}, I_4, I_3, I_2, I_1\} = \{0,0,0,0,0\}, \{0,0,0,0,1\}, \dots, \{1,1,1,1,0\},$ and $\{1,1,1,1,1\}$. Note that threshold technique is used to detect C_{o2} , and S , i.e., if the normalized magnetization of the output SW is larger than the threshold, value T , the output is logic 1 and 0, otherwise. For C_{o2} detection $T = 0$ is appropriate, which results in $C_{o2} = 1$ for input combinations $\{C_{in}, I_4, I_3, I_2, I_1\} = \{0,0,0,0,0\}, \{0,1,0,0,0\}, \{0,1,0,0,1\}, \{0,1,0,1,0\}, \{0,1,1,0,0\}, \{1,0,0,0,0\}, \{1,0,0,0,1\}, \{1,0,0,1,0\}, \{1,0,1,0,0\}, \{1,1,0,0,0\}, \{1,1,0,0,1\}, \{1,1,0,1,0\}, \{1,1,0,1,1\}, \{1,1,1,0,0\}, \{1,1,1,0,1\},$ and $\{1,1,1,1,0\}$, and $C_{o2} = 0$ for the remaining cases, as it should.

The same threshold value is suitable for S , but the threshold condition is flipped, i.e., if the resulted SW normalized magnetization is larger than 0, S is logic 0, and logic 1, otherwise. This results in $S = 0$ for $\{C_{in}, I_4, I_3, I_2, I_1\} = \{0,0,0,0,0\}, \{0,1,0,0,0\}, \{0,1,0,0,1\}, \{0,1,0,1,0\}, \{0,1,1,0,0\}, \{1,0,0,0,0\}, \{1,0,0,0,1\}, \{1,0,0,1,0\}, \{1,0,1,0,0\}, \{1,1,0,0,0\}, \{1,1,0,0,1\}, \{1,1,0,1,0\}, \{1,1,0,1,1\}, \{1,1,1,0,0\}, \{1,1,1,0,1\}$, and $S = 1$ for the remaining cases, as it should.

Therefore, the MuMax3 simulations proves that the proposed 4:2 approximate compressor provides the expected functionality.

V. PERFORMANCE EVALUATION AND DISCUSSION

We evaluate the proposed SW approximate 4:2 compressor and compare it in terms of error rate, energy consumption, delay, and area (the number of utilized devices) with the state-of-the-art SW, 45 nm CMOS²⁷, and Spin-CMOS²⁸ counterparts. In order to assess the performance of our proposal, we make the following assumptions: (i) Magnetoelectric (ME) cells having a power consumption of 34 nW, and a delay of 0.42 ns²⁹ are utilized for SW excitation/detection. (ii) SWs consume negligible energy during interference and propagation through waveguides. Note that these assumptions might need to be revisited to better capture SW technology future developments.

The proposed compressor with and without Directional Coupler (DC) delays can be calculated by adding the SW propagation determined by means of micro-magnetic simulations, and the delay of the excitation and detection cells, which sums-up to 11.4 ns and 3.4 ns, respectively. We note that in order to perform amplitude normalization the DC has to be rather long⁷, which results in a large delay overhead.

Table IV presents the evaluation results. When compared with the accurate SW compressor, which is a direct implementation consisting of two accurate SW adders in¹⁶, the proposed 4:2 compressor saves 31.5% energy and is 1.93x faster. Moreover, it has the same energy consumption, and error rate as the approximate compressor with DC, but it requires 3x less delay. In addition, it consumes 20% and 14% less energy, has approximately 2 orders of magnitude higher delay, and exhibits 61% more and 17% less average error rate when compared with CMOS1 and CMOS2 designs in Table IV, respectively. When compared with same error rate Spin-CMOS (Spin-CMOS1 design in Table IV), it consumes 3 orders of

TABLE III. Normalized Approximate SW-based 4:2 Compressor Outputs C_{o2} and S .

$C_{in}I_4I_3I_2I_1$	Resulting SW	C_{o2} after thresholding	S after thresholding
00000	0.45	1	0
00001	-0.08	0	1
00010	-0.07	0	1
00011	-0.59	0	1
00100	-0.01	0	1
00101	-0.46	0	1
00110	-0.49	0	1
00111	-1	0	1
01000	0.66	1	0
01001	0.23	1	0
01010	0.22	1	0
01011	-0.3	0	1
01100	0.3	1	0
01101	-0.21	0	1
01110	-0.2	0	1
01111	-0.69	0	1
10000	0.68	1	0
10001	0.18	1	0
10010	0.21	1	0
10011	-0.28	0	1
10100	0.28	1	0
10101	-0.22	0	1
10110	-0.18	0	1
10111	-0.73	0	1
11000	1	1	0
11001	0.51	1	0
11010	0.47	1	0
11011	0.012	1	0
11100	0.59	1	0
11101	0.07	1	0
11110	0.09	1	0
11111	-0.4	0	1

TABLE IV. Approximate 4:2 Compressor Performance Comparison.

Technology	Type	Error Rate	Energy (fJ)	Delay (ns)	Device No.
Spin Wave	Accurate	0	0.2	6.56	14
Spin Wave (with DC)	Approximate	0.31	0.137	11.4	8
Spin Wave (without DC)	Approximate	0.31	0.137	3.4	8
CMOS1 ²⁷	Approximate	0.125	0.172	0.049	40
CMOS2 ²⁷	Approximate	0.375	0.16	0.048	28
Spin-CMOS1 ²⁸	Approximate	0.31	173	3	28
Spin-CMOS2 ²⁸	Approximate	0.25	338	4	42

magnitude less energy and provides a 17% delay reduction. Although Spin-CMOS2 design provides 19% better average error rate, it is 3 order of magnitude less effective in terms of energy consumption and slower. Note that the proposed compressor requires the smallest number of devices, which indicates that it potentially requires the lowest chip real-estate. .

To get some inside on the implications of our proposal at the application level, we consider the well-known JPEG encoding, which makes use the Discrete Cosine Transform (DCT) ,³⁰ as discussion vehicle. Given that JPEG encoding is error tolerant and DCT is a multiplication dominated algorithm, 4:2 approximate compressors based tree multipliers are quite attractive for practical JPEG codec implementations. Such an approach has been presented in²⁸ and given that the approximate 4:2 compressor in²⁸ has the same average error rate as the one we propose, we can infer that replacing their compressor with ours does not change the image quality while resulting with 3 orders of magnitude less energy consumption.

We note that the main goal of this paper is to propose and validate a SW 4:2 approximate compressor and as such we do not take into consideration thermal and variability effects. However, in³¹, it was suggested that thermal noise, edge roughness, and waveguide trapezoidal cross section do not have noticeable impact on gate functionality. Thus, we expect that the 4:2 approximate compressor functions correctly under their presence. However, further investigation of such phenomena is of great interest but cannot be performed before technology data and suitable simulation tools become available.

VI. CONCLUSIONS

This paper proposed a Spin Wave (SW) based 4:2 approximate compressor, which consists of 3-input and 5-input Majority gates. We reported the design of approximate circuits without directional couplers, which are essential to normalize gate output(s) when cascading them in accurate circuit designs. We validated the proposed compressor by means of micromagnetic simulations, and compared it with the state-of-the-art SW, 22 nm CMOS, 45 nm CMOS, and Spin-CMOS counterparts.

The evaluation results indicated that the proposed 4:2 compressor saves 31.5% energy in comparison with the accurate SW compressor, has the same energy consumption, and error rate as the approximate compressor with DC, but it required 3x less delay. Moreover, it consumes 14% less energy, while having 17% lower error rate when compared with the approximate 45 nm CMOS counterpart. Furthermore, it outperforms the approximate Spin-CMOS based compressor by 3 orders of magnitude in term of energy consumption while providing the same error rate. Last but not least, the proposed compressor requires the smallest number of devices, thus it potentially requires the lowest chip real-estate.

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