Spin Wave Based Approximate Computing

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By their very nature Spin Waves (SWs) enable the realization of energy efficient circuits as they propagate and interfere within waveguides without consuming noticeable energy. However, SW computing can be even more energy efficient by taking advantage of the approximate computing paradigm as many applications are error-tolerant like multimedia and social media. In this paper we propose an ultra-low energy novel Approximate Full Adder (AFA) and a 2-bit inputs Multiplier (AMUL). The approximate FA consists of one Majority gate while the approximate MUL is built by means of 3 AND gates. We validate the correct functionality of our proposal by means of micromagnetic simulations and evaluate the approximate FA figure of merit against state-of-the-art accurate SW, 7nm CMOS, Spin Hall Effect (SHE), Domain Wall Motion (DWM), accurate and approximate 45nm CMOS, Magnetic Tunnel Junction (MTJ), and Spin-CMOS FA implementations. Our results indicate that AFA consumes 43% and 33% less energy than state-of-the-art accurate SW and 7nm CMOS FA, respectively, and saves 69% and 44% when compared with accurate and approximate 45nm CMOS, respectively, and provides a 2 orders of magnitude energy reduction when compared with accurate SHE, accurate and approximate DWM, MTJ, and Spin-CMOS, counterparts. In addition, it achieves the same error rate as approximate 45nm CMOS and Spin-CMOS FA whereas it exhibits 50% less error rate than the approximate DWM FA. Furthermore, it outperforms its contenders in terms of area by saving at least 29% chip real-estate. AMUL is evaluated and compared with state-of-the-art accurate SW and 16nm CMOS accurate and approximate state-of-the-art designs. The evaluation results indicate that it saves at least 2x and 5x energy in comparison with the state-of-the-art SW designs and 16nm CMOS accurate and approximate designs, respectively, and has an average error rate of 10%, while the approximate CMOS MUL has an average error rate of 12.5%, and requires at least 64% less chip real-estate.

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I. INTRODUCTION

While in the last decades CMOS downscaling has been able to enable high performance computing platforms required to process the information technology revolution induced huge data amount¹, it becomes very difficult to keep the same downscaling pace due to²: (i) leakage wall, (ii) reliability wall, and (iii) cost wall. This predicts that Moore's law will come to the end soon and, as a result, researchers have started to explore different technologies (e.g., memristors³⁻⁶, graphene devices⁷⁻⁹, and spintronics¹⁰⁻¹³) among which Spin Wave (SW) stands apart as one of the most promising due to its¹⁴⁻²⁰: (i) Ultra-low energy consumption - SW computing depends on wave interference instead of charge movements. (ii) Acceptable delay. (iii) Highly scalable - SW wavelengths can reach the nanometer range.

Driven by this potential to build energy efficient circuits, several SW based logic gates and circuits have been reported¹⁶⁻³⁰. The Mach-Zehnder interferometer was utilized to build a SW NOT gate, which is considered as the first SW computing device²¹. Moreover, XNOR, (N)AND, and (N)OR gates were reported by making use of the Mach-Zehnder interferometer²²⁻²⁴. Whereas the Mach-Zehnder interferometer utilise SW amplitude to perform the logic operations, other devices utilize SW phase or both phase and amplitude to build fanout enabled Majority, (N)AND, (N)OR, and X(N)OR gates^{19,20,25}. Moreover, SW frequency was utilised as an additional parameter to improve data storage and computing capabilities of multi-frequency Majority and X(N)OR gates^{17,18}. In addition, physical realization of Majority gates were demonstrated²⁶⁻²⁸. Furthermore, SW circuits were proposed at conceptual level, i.e., without simulation or experimental results,²⁹ at simulation level, 2-bit inputs SW multiplier¹⁶ and magnonic half-adder³¹, as well as simulation based practical *mm* range prototypes³⁰.

All the aforementioned logic gates and circuits were designed to provide accurate results, whereas many current applications like multimedia processing and social media are error tolerant and, within certain bounds, are not fundamentally perturbed by computation errors³². Therefore, such applications can benefit from approximate computing circuits, which can save significant amounts of energy, delay, and area, while providing acceptable accuracy. In view of this, this paper introduces novel energy efficient Approximate SW-based Full Adder (AFA) and Approximate 2-bit inputs Multiplier (AMUL), and its main contributions can be summarized as follows:

- Developing and designing a SW based approximate FA: The proposed adder consists of one Majority gate and has a 25 % error rate.
- Developing and designing a SW based Approximate 2-bit inputs MUL: The proposed AMUL is implemented using 3 AND gates and has a 10 % error rate.
- Validation of the proposed AFA and AMUL circuits by means of the MuMax3 software.
- Demonstrating the superiority: The proposed approximate circuits performance is assessed and compared with accurate and approximate state-of-the-art design counterparts. Our results indicate that AFA consumes 43% and 33% less energy than accurate state-of-the-art SW and 7 nm CMOS counterparts, respectively, and saves 69% and 44% in comparison with accurate and approximate 45 nm CMOS, respectively. In addition, it saves more than 2 orders of magnitude in terms of energy when compared with accurate Spin Hall Effect (SHE) and Domain Wall Motion (DWM), accurate and approximate Magnetic Tunnel Junction (MTJ), and Spin-CMOS based counterparts. In addition, it achieves the same error rate as approximate 45 nm CMOS and Spin-CMOS FAs and 50% less error rate than the approximate DWM. Also, it requires at least 29% less chip real-estate in comparison with the other state-of-the-art designs. Moreover, AMUL saves at least 2x and 5x energy in comparison with accurate SW and 16 nm CMOS accurate/approximate designs, respectively, has an average error rate of 10%, while the approximate CMOS MUL has an average error rate of 12.5%, and requires at least 64% less chip real-estate.

The paper is organized as follows. Section II provides SW computing background. Section III introduces the proposed approximate circuits. Section IV presents the simulation setup and simulation results. Section V provides performance evaluation data and discusses variability and thermal noise effects and Section VI concludes the paper.

II. SPIN WAVE BASED TECHNOLOGY BASICS

We explain the SW basics and computing paradigm in this section.

FIG. 1. a) Constructive and Destructive Interference. b) Spin Wave Device

A. Spin Wave Fundamentals

The Landau-Lifshitz-Gilbert (LLG) describes the magnetization dynamics caused by the magnetic torque when magnetic material magnetization is out of equilibrium¹⁴

$$\frac{d\vec{M}}{dt} = -|\gamma|\mu_0 \left(\vec{M} \times \vec{H}_{eff} \right) + \frac{\alpha}{M_s} \left(\vec{M} \times \frac{d\vec{M}}{dt} \right), \quad (1)$$

where γ is the gyromagnetic ratio, α the damping factor, M the magnetization, M_s the saturation magnetization, and H_{eff} the effective field which contains the different magnetic interactions. In this work, the effective field is the summation of the external field, the exchange field, the demagnetizing field, and the magneto-crystalline field.

For small magnetic perturbations, Equation (1) can be linearized and results in wave-like solutions which are known as Spin Waves (SWs), which can also be seen as collective excitations of the magnetization within the magnetic material. Just like any other wave, a SW is completely described by its amplitude A , phase ϕ , frequency f , wavelength λ , and wavenumber $k = \frac{2\pi}{\lambda}$. The relation between frequency f and wavenumber k is called the dispersion relation and is very important for the design of the magnonic devices¹⁴.

B. SW Computation Paradigm

The SW amplitude and phase can be used to encode information at different frequencies, which enables parallelism^{14,17}. The interaction between multiple SWs present in the same waveguide is based on the interference principle. Figure 1a) presents an example of interaction between 2 SWs excited with the same A , λ , and f in the same waveguide. If the 2 SWs have the same phase $\Delta\phi = 0$, they interfere constructively resulting in a SW with higher amplitude, whereas if they are out of phase $\Delta\phi = \pi$, they interfere destructively, resulting in approximately zero amplitude SW. Moreover, SWs interference provides natural support for Majority function evaluation as if an odd number of SWs interfere the resultant SW is obtained by a Majority decision. For example, if 3 same A , λ , and f SWs interfere the resultant SW has a phase of 0 if at most 1 SW has a phase of π and a phase of π if at most 1 SW has a phase of 0. Note that such a 3-input Majority CMOS implementation requires 18 transistors whereas in SW technology it is implemented using one waveguide only. More complex interference cases exist if the propagating SWs have different A , λ , and f , which might be of interest for designing novel magnonic computing systems. However, in this paper, we focus on the simplest case where all the excited SWs have the same A , λ , and f and can take two discrete phases $\phi = 0$ and $\phi = \pi$. Logic 0 refers to a SW with $\phi = 0$, and a logic 1 refers to a SW with $\phi = \pi$.

Figure 1b) presents a generic SW logic device that consists of four regions: Excitation Stage I , Waveguide B , Functional Region FR , and Detection Stage O ¹⁴. In I SWs are generated by means of, e.g., microstrip antennas¹⁴, magnetoelectric cells¹⁴, Spin Orbit Torque¹⁴. B is the medium for SW propagation and can be made of different magnetic materials, e.g., Permalloy, Yttrium iron garnet, CoFeB¹⁴. The waveguide material is an important parameter as it fundamentally determines the SW properties. In FR SWs can be amplified, normalized or interfere with other SWs. In O the output SW is captured and converted to the electrical domain using the same type of cells as in I . Two main SW detection techniques are in place¹⁴: phase and threshold based. In phase detection, the output is determined by comparing the detected SW phase with a predefined phase. For example, if the detected SW has a phase of $0/\pi$ the output is logic 0/1, respectively. Threshold detection determines the output by comparing the detected SW amplitude with a predefined threshold. For instance, if the detected SW amplitude is larger than the predefined threshold, the output is logic 1

FIG. 2. Approximate Spin Wave Based FA.

and logic 0 otherwise.

III. SW APPROXIMATE FUNCTIONS

In this section, we introduce and analyse SW-based Approximate Full Adder (AFA) and 2-bit inputs Multiplier (AMUL).

A. SW Approximate Full Adder

Figure 2 presents the proposed Approximate FA (AFA) structure, which has 3 inputs X , Y , and C_i , and 2 outputs S and C_o and is a 3-input Majority gate that evaluates $S = \overline{C_o} = \overline{MAJ(X, Y, C_i)}$ as suggested in³³. AFA generates C_o without any error as it is detected as the Majority of X , Y , and C_i , which is also the case in accurate FAs. On the

TABLE I. Accurate and Approximate SW-based FA

XYC_i	C_o	S_{ac}	S_{ap}
0 0 0	0	0	<u>1</u>
0 0 1	0	1	1
0 1 0	0	1	1
0 1 1	1	0	0
1 0 0	0	1	1
1 0 1	1	0	0
1 1 0	1	0	0
1 1 1	1	1	<u>0</u>

other hand, S is detected with a 25% error rate as $S = \overline{MAJ(X, Y, C_i)}$ approximate the accurate FA Sum, which equals to $S = XOR(XOR(X, Y), C_i)$. Table I presents FA and AFA truth tables, which clarifies that the approximate FA sum S_{ap} is erroneous when all inputs are 0/1.

To achieve the AFA behaviour the design in Figure 2 has to be properly dimensioned. The waveguide width must be smaller or equal to the SW wavelength λ and SW amplitude, wavelength, and frequency must be the same at every excitation cell. Furthermore, the structure dimensions must be precisely determined because the interference pattern depends on the location and distances between different excitation and detection cells. For example, if the constructive interference pattern is desired when the SWs have the same phase $\Delta\phi = 0$ and destructive when the SWs are out-of-phase $\Delta\phi = \pi$, d_1 , d_2 , and d_3 must be equal with $n\lambda$ (where $n = 0, 1, 2, 3, \dots$). In addition, if the inverted Majority is of interest, which is the case for S , d_4 must be $(n + 1/2) \times \lambda$ and if the non-inverted output is required, which is the case for C_o , d_5 must be $n\lambda$. The AFA operation principle relies on a combined process of SWs propagation and interferences as follows: First, SWs are excited at X and Y and propagate diagonally until they interfere constructively or destructively depending on their phases at the connection point. Then, the resulting SW propagates and interferes constructively or destructively with the SW excited at C_i at the next connection point. This interference result generates the final SW, which travels toward the outputs and $\overline{MAJ(X, Y, C_i)}$ is detected at S and $MAJ(X, Y, C_i)$ at C_o .

TABLE II. Accurate and Approximate SW-based Multiplier

$X_1X_0Y_1Y_0$	Q_0	Q_{1ac}	Q_{1ap}	Q_{2ac}	Q_{2ap}	Q_{3ac}	Q_{3ap}
0 0 0 0	0	0	0	0	0	0	0
0 0 0 1	0	0	0	0	0	0	0
0 0 1 0	0	0	0	0	0	0	0
0 0 1 1	0	0	0	0	0	0	0
0 1 0 0	0	0	0	0	0	0	0
0 1 0 1	1	0	0	0	0	0	0
0 1 1 0	0	1	<u>0</u>	0	0	0	0
0 1 1 1	1	1	<u>0</u>	0	0	0	0
1 0 0 0	0	0	0	0	0	0	0
1 0 0 1	0	1	<u>0</u>	0	0	0	0
1 0 1 0	0	0	<u>1</u>	1	1	0	0
1 0 1 1	0	1	1	1	1	0	0
1 1 0 0	0	0	0	0	0	0	0
1 1 0 1	1	1	<u>0</u>	0	0	0	0
1 1 1 0	0	1	1	1	1	0	<u>1</u>
1 1 1 1	1	0	<u>1</u>	0	<u>1</u>	1	1

To evaluate the error rate we note that in the accurate MUL the outputs bits are computed as $Q_0 = (X_0, Y_0)$, $Q_1 = XOR(AND(X_0, Y_1), AND(X_1, Y_0))$, $Q_2 = XOR(AND(AND(X_0, Y_1), AND(X_1, Y_0)), AND(X_1, Y_1))$, and $Q_3 = AND(AND(X_0, Y_0), AND(X_1, Y_1))$, and present in Table II MUL and AMUL output values for all possible input combinations. Note that the erroneous values are written in bold and underlined. One can observe in the Table that AMUL computes Q_0 without any error, and Q_1 , Q_2 , and Q_3 with 31.25%, 6.25%, and 6.25% error rate, respectively. However if threshold based output detection is utilized the error rate for Q_1 and Q_3 can be reduced to 25% and 0%, respectively, as demonstrated in Section IV, which brings our proposal to an average error rate of 10%.

The previously mentioned design parameters hold true for the AMUL as well. However, in contrast to AFA, AMUL relies on threshold based output detection, which means that the detection cells must be as close as possible to the last interference point, thus d_4 , d_5 , d_6 , and d_7 should be minimized.

IV. SIMULATION SETUP AND RESULTS

The simulation setup and simulation results are provided and explained in this section.

TABLE III. Simulation Parameters

Parameters	Values
Saturation magnetization M_s	1.1×10^6 A/m
Perpendicular anisotropy constant k_{ani}	0.83 MJ/m ³
Damping constant α	0.004
Exchange stiffness A_{exch}	18.5 pJ/m

A. Simulation Setup

We make use of a 50 nm width and 1 nm thick $Fe_{60}Co_{20}B_{20}$ waveguide and the parameters specified in Table III³⁴ to validate the proposed approximate designs (AFA and AMUL) by means of MuMax3³⁵. As previously mentioned, the SW wavelength should be larger than the waveguide width to improve the interference pattern. Therefore, a 55 nm SW wavelength was chosen. After that, the AFA dimension are determined as follows: $d_1=330$ nm, $d_2=880$ nm, $d_3=220$ nm, $d_4=80$ nm, and $d_5=110$ nm and the AMUL are $d_1=330$ nm, $d_2=880$ nm, $d_3=220$ nm, $d_4=40$ nm, $d_5=40$ nm, $d_6=40$ nm, and $d_7=80$ nm. Last, based on the SW dispersion relation, the SW frequency for a wavenumber $k=2\pi/\lambda=50$ rad/ μ m was calculated to correspond to a SW frequency of 10 GHz.

B. Simulation Results

1-bit approximate FA based on phase detection

Figure 4 a) to h) present AFA MuMax3 simulation results for $\{X, Y, C_i\} = \{0,0,0\}$, $\{0,0,0\}$, $\{0,0,1\}$, $\{0,1,0\}$, $\{0,1,1\}$, $\{1,0,0\}$, $\{1,0,1\}$, $\{1,1,0\}$, and $\{1,1,1\}$, respectively. Note that blue represents logic 0 and red logic 1. One can observe in the Figure that the outputs S and C_o are detected as expected. For instance, $C_o = 1$ for $\{I_1, I_2, I_3\} = \{0,1,1\}$, $\{1,0,1\}$, $\{1,1,0\}$, and $\{1,1,1\}$, while $C_o = 0$ for $\{I_1, I_2, I_3\} = \{0,0,0\}$, $\{0,0,1\}$, $\{0,1,0\}$, and $\{1,0,0\}$. Moreover, S is inverted $C_o = 0$ as expected.

FIG. 4. Approximate Spin Wave Based FA MuMax3 Simulation.

2-bit inputs approximate MUL based on threshold detection

Figures 5 to 8 present AMUL MuMax3 simulation results. In the figures, the y -axis presents the SWs M_x over M_s ratio, where M_x is the magnetization projection along the x -direction and M_s the saturation magnetization. Inspecting Figure 5 we observe that Q_1 output SW magnetization at time 2.7 ns for the input values $X_1Y_1X_0Y_0=\{0011,0111,1011,1111\}$, which should corresponds to $Q_0 = 1$, is larger than $0.001M_s$ and smaller than $0.001M_s$ for the rest of the input combinations. Thus, by setting the detection threshold to $0.001M_s$, i.e., SW magnetization larger than $0.001M_s$ means logic 1 and logic 0 otherwise, Q_0 is always properly detected.

Similarly, one can analyze Figure 6. For instance, the SWs magnetization for the input combinations $X_1Y_1X_0Y_0=\{0101,0111,1001,1011,1100,1101,1110,1111\}$ are larger than 0 when reading them at time 2.76 ns, whereas for the other input combinations magnetization is less than 0. Therefore, if the threshold is set to 0 Q_1 value can be derived. Note that by doing so the theoretically predicted Q_1 error rate of 31.25% is diminished to 25%.

FIG. 5. Normalized First AMUL Output.

FIG. 6. Normalized Second AMUL Output.

Using the same way, Figure 7 is analyzed. The SW magnetization for input combinations $X_1Y_1X_0Y_0=\{1100,1101,1110,1111\}$ are larger than $0.0005M_s$ when reading them at time 2.76 ns, whereas for the rest magnetization are less than $0.0005M_s$. Therefore, if the threshold is set to be $0.0005M_s$, Q_2 can be properly obtained with 0% error rate.

FIG. 7. Normalized Third AMUL Output.

FIG. 8. Normalized Forth AMUL Output.

Finally, Figure 8 is analyzed in the same manner. The SWs magnetization for input combination $X_1Y_1X_0Y_0=\{1111\}$ is larger than $0.0014M_s$ when reading them at time 2.76 ns, whereas the rest of magnetization are less than $0.0014M_s$. Therefore, if the threshold is set to be $0.0014M_s$ Q_3 can be obtained with 0% error rate.

V. PERFORMANCE EVALUATION AND DISCUSSION

In this section, the proposed AFA and AMUL are evaluated and compared with the state-of-the-art designs. Furthermore, the variability and thermal noise effects are discussed in addition to some open issues related to SW technology.

Performance Evaluation

To get inside on the practical implications of our proposal we compare AFA with the state-of-the-art accurate SW³⁶, 7 nm CMOS³⁷, SHE³⁸, DWM³⁹, accurate and approximate 45 nm CMOS⁴⁰, MTJ⁴¹, and Spin-CMOS³³ counterparts in terms of energy, delay, and area (the number of utilized devices). To evaluate AFA we make use of the following assumptions: (i) Excitation and detection cells are Magnetoelectric (ME) cells which power consumption and delay are 34 nW and 0.42 ns, respectively⁴². (ii) During propagation and interference, SWs consume negligible amount of energy. (iii) The outputs are driving followup gates, the detection cells are not considered in the energy consumption calculation. (iv) Pulse signals are used to excite SWs. Note that due to SW technology early stage development the aforementioned assumptions might need to be re-evaluated as the SW technology becomes more mature.

The AFA delay is calculated by adding ME cell delay to the SW propagation delay through the waveguide determined by means of micromagnetic simulation and equals to 1.84 ns. Table IV presents the results of the evaluation and comparison. Inspecting the Table, it is clear that AFA outperforms state-of-the-art 7 nm CMOS³⁷ accurate FA by energy reductions of approximately 33%, while exhibiting more than 2 orders of magnitude larger delay. Furthermore, AFA saves approximately 69% and 44% energy while requiring 15x and 18x larger delay when compared with 45 nm CMOS based accurate and approximate FA, respectively, while having the same error rate as the approximate FA in⁴⁰. When compared with other emerging technologies based designs, AFA consumes 5 orders of magnitude less energy than MTJ based accurate and approximate FAs while exhibiting 42% lower delay and having 50% better error rate than the MTJ approximate FA in⁴¹. Moreover, AFA consumes 5 and 3 orders of magnitude less energy than SHE- and DWM- based accurate FAs, respectively, has 3.8x lower and 52% more delay than SHE³⁸ and DWM³⁹ based FAs, respec-

TABLE IV. Full Adder Performance Comparison

Technology	Type	Error Rate	Energy (fJ)	Delay (ns)	Device No.
CMOS ³⁷	Accurate	0	0.065	0.005	28
CMOS ⁴⁰	Accurate	0	0.14	0.12	24
CMOS ⁴⁰	Approximate	0.25	0.077	0.1	14
MTJ ⁴¹	Accurate	0	5685	3.019	29
MTJ ⁴¹	Approximate	0.5	5109	3.016	25
MTJ ⁴¹	Approximate	0.5	2471	3.152	29
SHE ³⁸	Accurate	0	4970	7	26
DWM ³⁹	Accurate	0	74.5	0.877	26
Spin CMOS ³³	Accurate	0	166.7	3	34
Spin CMOS ³³	Approximate	0.25	58	2	34
Spin Wave ³⁶	Accurate	0	0.072	2.86	7
Spin Wave	Approximate	0.25	0.043	1.84	5

tively. Furthermore, AFA consumes approximately 4 and 3 orders of magnitude less energy while requiring 38% and 8% lower delay in comparison with the accurate and approximate Spin-CMOS based FAs, respectively, while having the same error rate as the approximate FA in³³. Last but not least, AFA outperforms the SW based accurate FA³⁶ by 40% and 35% in terms of energy and delay, respectively. Note that as a chip real-estate estimation that the proposed approximate FA requires the lowest number of devices.

Under the same assumptions AMUL delay is 3.3 ns and we compare it with state-of-the-art SW¹⁶ and CMOS⁴³ counterparts. As delay figures are not mentioned for the approximate multiplier in⁴³, its energy consumption was estimated based on the 16 nm CMOS figures provided in⁴⁴. Table V present the results of the evaluation and comparison. Inspecting the Table, it is clear that AMUL outperforms accurate 16 nm CMOS⁴³ and approximate 16 nm CMOS⁴³ counterparts by diminishing the energy consumption by 16x and 5x while exhibiting 33x and 55x larger delay, respectively. AMUL has an average error rate of 10% while 12.5% is the average error rate for the approximate CMOS counterpart⁴³. Note that the average error rate is calculated by adding the average of Q_1 , Q_2 , and Q_3 error rates as the first output Q_0 is accurately compute in both implementations. When compared with accurate

TABLE V. 2-bit inputs Multiplier Performance Comparison

Design	CMOS ^{43,44}		SW ¹⁶		Proposed SW MUL
Implemented method	-		Coupler Cascading	Conversion Cascading	-
Type	Accurate	Approximate	Accurate	Accurate	Approximate
Average Error Rate	0	0.125	0	0	0.1
energy (aJ)	959	300	259	374	58
Delay (ns)	0.1	0.06	21	1.68	3.3
Device No.	52	30	22	30	8

MUL SW implementations, AMUL saves 4x and 6x energy and approximately 6x lower and 2x more delay in comparison with SW coupler and conversion based MUL implementations, respectively. We note that the SW propagation delay is neglected into the evaluation of the SW conversion based MUL in¹⁶. One can observe from the Table that the proposed MUL requires less ME cells than the SW designs in¹⁶ which indicates that the design in¹⁶ has a larger area and by implication a larger delay if SW propagation is also considered.

Variability and Thermal Effect

In this paper, the main target is to propose and validate by means of micromagnetic simulations the approximate FA and MUL as proof of the concepts without considering the impacts of the thermal noise and the variability. However, it was reported that the thermal noise has limited effect on the gate function and consequently the gate works correctly at different temperature⁴⁵. In addition, the effect of the edge roughness and the waveguide trapezoidal cross section were demonstrated⁴⁵. It was suggested that both effects are very small and the gate operates correctly at their presence as well⁴⁵. Therefore, we don't expect neither the thermal noise nor the geometrical variability to have large impact on the proposed circuits. However, we plan to investigate these phenomena in the future.

Discussion

Although the evaluation demonstrated that the SW technology has the needed requirements to improve the state-of-the-art in terms of energy as well as area consumption, but a number of open issues are still to be solved¹⁴:

- Immature technology: It seems that the ME cells are the right option to excite and

detect the SW because of their ultra low energy consumption, acceptable delay and scalability. However, ME cells are not realized experimentally until now.

- Scalability: In terms of area SW circuit have a great scaling potential as for proper functionality SW device dimensions must be greater or equal than the SW wavelength, which can reach down to the nm range. Several SW circuit area benchmarkings have been reported⁴² which indicate that hybrid spin-wave–CMOS circuits have very small area. Although the assumptions the benchmarking is based on might not be fully realistic, they give an indication regarding the expected area. For example, the area of a 32-bit divider (DIV32) implemented in hybrid SW-CMOS is roughly about 3.5x smaller than the one of the 10 nm CMOS counterpart. However, few things are needed before being able to realize nano-scale SW device such as excitation and detection: currently, it is not possible to distinguish nm SWs from noise.

VI. CONCLUSIONS

We proposed and validated by means of micromagnetic simulations a novel approximate energy efficient spin wave based Full Adder (AFA) and 2-bit inputs multiplier (AMUL). Both designs were evaluated and compared with the state-of-the-art counterparts. AFA saves 43% and 33% energy when compared with the state-of-the-art SW and 7 nm CMOS, respectively, and 69% and 44% in comparison with accurate and approximate 45 nm CMOS, respectively. In addition, it saves more than 2 orders of magnitude when compared with accurate SHE, and accurate and approximate DWM, MTJ, and Spin-CMOS FAs. Moreover, it achieves the same error rate as approximate 45 nm CMOS and Spin-CMOS FA whereas it exhibits 50% less error rate than approximate DWM FA and requires at least 29% less chip real-estate in comparison with the other state-of-the-art designs. At its turn AMUL saves at least 2x and 5x energy in comparison with the state-of-the-art accurate SW designs and 16 nm CMOS accurate and approximate designs, respectively. Moreover, the AMUL has an average error rate of 10%, while the approximate CMOS MUL has an average error rate of 12.5%, and requires at least 64% less chip real-estate.

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