The Impact of a Paraelectric layer in the FE/DE Stack on Performance of NCFET

This paper was downloaded from TechRxiv (<https://www.techrxiv.org>).

LICENSE

CC BY-NC-SA 4.0

SUBMISSION DATE / POSTED DATE

12-01-2022 / 14-01-2022

CITATION

Kansal, Harshit; Medury, Aditya S (2022): The Impact of a Paraelectric layer in the FE/DE Stack on Performance of NCFET. TechRxiv. Preprint. <https://doi.org/10.36227/techrxiv.18257987.v1>

DOI

[10.36227/techrxiv.18257987.v1](https://doi.org/10.36227/techrxiv.18257987.v1)

The Impact of a Paraelectric layer in the FE/DE Stack on Performance of NCFET

Harshit Kansal, and Aditya Sankar Medury

Abstract—In this letter, through TCAD simulations, we show that the introduction of a thin paraelectric (PE) layer between the ferroelectric (FE) and dielectric (DE) layers in an MFIS structure, expands the design space for the FE layer enabling hysteresis-free and steep subthreshold behavior, even with a thicker FE layer. This can be explained by analyzing the FE-PE stack from a capacitance perspective where the thickness of the PE layer in the FE-PE stack has the effect of reducing the FE layer thickness, while also reducing the remnant polarization. Finally, for the same FE-PE-DE stack, analog performance parameters such as $\frac{g_m}{g_{ds}}$ and $\frac{g_m}{I_d}$ are analyzed, showing good characteristics over a wide range of gate lengths, at low drain voltages, thus demonstrating applicability for low power applications.

Index Terms—NCFET, FE/PE Gate Stack, Hysteresis-free, Sub-60 mV/Dec, Short-channel

I. INTRODUCTION

FERROELECTRIC-BASED negative capacitance (NC) Field-Effect Transistors (FETs), which can enable sub-60 mV/dec switching, are being actively researched for Ultra-low power applications [1]. Amongst the different NCFET structures, the Metal-Ferroelectric-Insulator-Semiconductor (MFIS) FET has been shown to be more practical in achieving NC behavior [2], where capacitance matching of the ferroelectric (FE) and Dielectric (DE) layers may not be adequate to ensure both steep sub-threshold slope as well as hysteresis free behavior [3]. In addition, an MFIS FET with the same FE-DE stack may not be adequate to ensure both good digital and analog device performance [4] [5]. Therefore, a critical challenge is to design the gate stack to ensure hysteresis free NC behavior demonstrating good digital and analog device behavior.

Before considering the effect of the novel gate stack we propose in this work, it is first important to explain the design and performance of the baseline MOSFET device. In this work, we consider the base-line device to be a Bulk MOSFET structure with a junction-less channel, as shown in Figure 1(a), where the thickness of the dielectric (DE) layer comprising of an $\text{HfO}_2/\text{SiO}_2$ layer gate stack of suitable thickness (EOT = 0.88 nm) is designed to obtain sub-threshold slopes varying between 130 mV/dec and 150 mV/dec, for L_g (gate length) of 10 nm, when the drain-to-source voltage (V_{ds}) varies between 50 mV and 1 V, while the sub-threshold slopes, for L_g of 30

Fig. 1. (a) Schematic of the Baseline Junction-less Bulk MOS Device with a Dielectric Gate Stack; (b) Ferroelectric-Paraelectric/DE Stack over a Baseline Device

nm, over the same range of drain voltages, are approximately 85 mV/dec.

Having briefly discussed the baseline device, we now propose to introduce a ferroelectric (FE)-paraelectric (PE) gate stack which we describe in the second section. We then describe the TCAD simulation methodology used in the paper in the third section, followed by a discussion on the impact of the proposed FE-PE gate stack on the digital and analog device performance parameters in the fourth and fifth sections, respectively, with a brief conclusion in the sixth section.

II. PROPOSED GATE STACK

The free energy profile of a typical FE or PE material is described [6] as shown in equation (1):

$$U = \alpha P^2 + \beta P^4 + \gamma P^6 - P \cdot E \quad (1)$$

Here, α , β and γ are material dependent constants, E is the electric field and P is the polarization. In order to determine the effect of these parameters on the remnant polarization, we determine the polarization, P , when $\frac{dU}{dP} = 0$ and the external electric field $E = 0$. From this condition:

$$P^2 = \left(\frac{-\beta}{3\gamma} \right) + \left(\frac{\beta}{3\gamma} \right) \sqrt{\left(1 - \left(\frac{3\alpha\gamma}{\beta^2} \right) \right)} \quad (2)$$

In equation (2), for an FE layer, since α is negative, therefore, the argument inside the square root always remains positive. In addition, by using Taylor's series expansion for the FE layer in equation (2), considering only the first three terms, the remnant polarization can be obtained from the roots of the equation (3).

$$P^2 = \frac{\alpha}{2\beta} - \left(\frac{3}{8} \right) \frac{\gamma\alpha^2}{\beta^3} \quad (3)$$

Harshit Kansal is with the Indian Institute of Science Education and Research, Bhopal, India (e-mail: harshit16@iiserb.ac.in).

Aditya Sankar Medury is with the Indian Institute of Science Education and Research, Bhopal, India (e-mail: adityam@iiserb.ac.in).

Therefore, the roots of equation (3) (remnant polarization) are dependent on the values of α , β and γ of the FE layer. This also shows that the reduction of the remnant polarization and thus the hysteresis effects seen in gate stacks comprising of FE layers, can be achieved by increasing the value of β , while also increasing the value of γ . Therefore, with a view to obtaining hysteresis free behavior along with steep Sub-Threshold slopes(SS), we now propose to introduce a Ferroelectric (FE)-Paraelectric (PE) gate stack above the Dielectric (DE) layer, as shown in Figure 1(b).

In this FE-PE gate stack, the L-K parameters used to represent the FE layer are similar to those used by Agarwal et.al [7], where $\gamma > 0$ for the FE layer. On the other hand, the parameters meant to present the PE layer are similar to the FE layer, with the only key differences being that the L-K parameter $\gamma = 0$ [8], while α is positive and of the same value as the FE layer. From the FE layer capacitance, $C_{FE}(Q) = \frac{1}{t_{FE}(-2\alpha + 4\beta Q^2 + 6\gamma Q^4)}$ and the PE layer capacitance $C_{PE}(Q) = \frac{1}{t_{PE}(2\alpha + 4\beta Q^2 + 6\gamma Q^4)}$, the series combination of the FE-PE stack can be obtained and is shown in equation (4).

$$C_{eff}(Q) = \frac{1}{(t_{FE} - t_{PE})} \frac{1}{(-2\alpha + 4\beta' Q^2 + 6\gamma' Q^4)} \quad (4)$$

where $\beta' = \beta \left(\frac{t_{FE} + t_{PE}}{t_{FE} - t_{PE}} \right)$, $\gamma' = \gamma \left(\frac{t_{FE}}{t_{FE} - t_{PE}} \right)$. From equation (4), the FE-PE stack is capacitively equivalent to a thinner ferroelectric of thickness $t_{FE} - t_{PE}$, with the same value of α as the original FE material, with an effectively higher value of β and γ (represented through β' and γ' , respectively, in equation (4)), implying a lower remnant polarization, as seen from equation (3), thus also reducing the hysteresis.

III. SIMULATION METHODOLOGY

For all the device simulations of the proposed NCFET structure, shown in Figure 1(b), the Synopsys 2-D TCAD device simulator [9] is used, where physics commonly seen in short-channel junction-less (JL) MOSFETs including carrier transport effects, Quantum Effects and BTBT effects are included in the baseline MOSFET device through considering the band gap narrowing model, Shockley-Read-Hall recombination model, Philips mobility model, Non-local Band-to-Band tunneling model and QC Vandort Model. Furthermore, inclusion of an FE-PE gate stack is made possible through solving the Landau-Khalatnikov equation, along the direction perpendicular to the direction of carrier transport, in the self-consistent loop with Poisson's equation along with the Drift-Diffusion and Continuity equation, thus enabling determination of the electrostatics and the drain current of the NCFET structure.

IV. DIGITAL DEVICE PERFORMANCE

In this section, we analyze the impact of the FE-PE stack on the digital device performance parameters such as the Sub-Threshold slope (SS), including on the hysteresis behavior of the proposed NCFET structure. In this context, we choose an FE layer (t_{FE}) thickness of 7 nm and consider a wide range of PE layer (t_{PE}) thicknesses varying from 1 nm to 3 nm, so as to analyze these aspects. In the NCFET structure proposed

Fig. 2. Drain Current (I_d) as a function of the Drain to Source Voltage (V_{ds}), for different PE layer thicknesses, when (a) $L_g = 10$ nm (b) $L_g = 30$ nm, over a range of Gate to Source Voltages (V_{gs}). V_{ds} , where non-negative Differential Resistance is seen over the entire range of V_{gs} considered, is identified for different PE layer thicknesses.

in Figure 1, we consider a range of gate lengths (L_g) from 10 nm to 30 nm, where the I_d - V_{ds} characteristics for different PE layer thicknesses and gate voltages, are shown in Figures 2(a) and 2(b). From Figure 2(a) and (b), we choose the highest drain voltage (V_{ds}) for each paraelectric (PE) layer thickness, where the drain current (I_d) shows either an increasing or saturating trend (no Negative Differential Resistance (NDR) effect, output conductance, $g_{ds} > 0$) and obtain the switching characteristics (through transient simulations), at that drain voltage. The idea in choosing these drain voltages, which are different for different PE layer thicknesses and gate lengths and where the NDR effect is negligible, is primarily to analyze the FE-PE gate stack in the context of low power Digital device applications as well as non-switching Analog device applications [10]. Through switching characteristics (Drain current (I_d) as a function of the applied gate voltage (V_g)), shown in Figures 3(a) and 3(b), for $L_g = 10$ nm and 30 nm, respectively, for different drain voltages, the drain currents in the forward and reverse paths are found to be exactly overlapping over each other, with no change in either the threshold voltage or sub-threshold slopes, thus demonstrating no hysteresis. In addition, the average sub-threshold slopes for PE layer thickness varying from 1 nm to 3 nm are found to be steep, seen in the range of 35 mV/dec to 45 mV/dec, for $L_g = 10$ nm and from 43 mV/dec to 47 mV/dec, for $L_g = 30$ nm.

V. ANALOG DEVICE PERFORMANCE

Having demonstrated good digital device performance, at relatively low drain voltages, we now investigate the impact of the FE-PE gate stack on various analog device performance parameters. From the I_d - V_{ds} and I_d - V_g results, shown in Figures

Fig. 3. I_d as a function of V_{gs} , under transient sweep, for (a) $L_g = 10\text{nm}$ (b) $L_g = 30\text{nm}$, with suitable V_{ds} identified from Fig. 2, showing Hysteresis-free and steep sub-threshold characteristics.

Fig. 4. Transconductance generation Efficiency versus V_{gs} , for (a) $L_g = 10\text{nm}$ (b) $L_g = 30\text{nm}$, showing lower values over a wider range of V_{gs} with increase in PE layer thicknesses.

Fig. 5. Intrinsic Gain as a function of V_{gs} for (a) $L_g = 10\text{nm}$ (b) $L_g = 30\text{nm}$, showing lower gain over a wider range of V_{gs} with increase in PE layer thickness.

2 and 3, the output conductance (g_{ds}) and transconductance (g_m) are obtained. Increased g_m seen for shorter gate lengths, where much steeper Sub-Threshold slopes are seen, manifests in terms of a much higher transconductance efficiency, $\frac{g_m}{I_d}$, as seen in Figure 4. Figure 4 also shows that an increase in PE layer thickness manifests in terms of a lower peak g_m implying lowered transconductance efficiency, albeit, spread over a wider range of gate voltages. In addition, it is important to note that lower g_{ds} with increasing PE layer thicknesses, but

much more significantly, with increasing gate lengths, results in much higher intrinsic gain ($\frac{g_m}{g_{ds}}$), as seen in Figure 5. In Figure 5(a), with increase in PE layer thickness, for $L_g = 10\text{nm}$, due to the reduction in g_{ds} being nearly compensated by the reduction in g_m , the intrinsic gain is nearly comparable. However in Figure 5(b), for $L_g = 30\text{nm}$, due to greater reduction in g_m compared to g_{ds} , the maximum intrinsic gain decreases with increasing PE layer thickness. Also, it is seen from Figure 5 that with increasing PE layer thickness, reduced peak g_m values and therefore the intrinsic gain tends to be spread over a wider range of gate voltages.

VI. CONCLUSION

The inclusion of a Paraelectric layer between the Ferroelectric and Dielectric layers in an MFIS structure, with a junctionless Bulk MOSFET as the baseline device, has enabled the Ferroelectric layer to be made thicker manifesting in terms of enhanced Digital and Analog device performance, without Hysteresis, over a wide range of gate lengths. Furthermore, obtaining enhanced device characteristics at very low Drain to Source voltages (V_{ds}) has illustrated the applicability of such NCFET structures for low power applications.

REFERENCES

- [1] Gaidhane AD, Pahwa G, Verma A and Chauhan YS, "Compact modeling of drain current, charges, and capacitances in long-channel gate-all-around negative capacitance MFIS transistor," in *IEEE Transactions on Electron Devices*, vol. ED-65, no. 5, pp. 2024-32, Mar. 2018, 10.1109/TED.2018.2813059.
- [2] Kittl JA, Obradovic B, Reddy D, Rakshit T, Hatcher RM and Rodder MS, "On the validity and applicability of models of negative capacitance and implications for MOS applications," in *Applied Physics Letters*, vol. ED-113, Jul. 2018, <https://doi.org/10.1063/1.5036984>.
- [3] Amrouch H, Pahwa G, Gaidhane AD, Henkel J and Chauhan YS, "Negative capacitance transistor to address the fundamental limitations in technology scaling: Processor performance," in *IEEE Access*, vol. ED-6, pp. 52754-65, Sep. 2018, 10.1109/ACCESS.2018.2870916.
- [4] Li Y, Kang Y and Gong X, "Evaluation of negative capacitance ferroelectric MOSFET for analog circuit applications," in *IEEE Transactions on Electron Devices*, vol. ED-64, no. 10, pp. 4317-21, Sep. 2017, 10.1109/TED.2017.2734279.
- [5] Eslahi H, Hamilton TJ and Khandelwal S, "Small signal model and analog performance analysis of negative capacitance FETs," in *Solid-State Electronics*, vol. ED-186, no. 1, Dec. 2021, <https://doi.org/10.1016/j.sse.2021.108161>.
- [6] Khan AI, Chatterjee K, Wang B, Drapcho S, You L, Serrao C, Bakaul SR, Ramesh R and Salahuddin S, "Negative capacitance in a ferroelectric capacitor," in *Nature materials*, vol. ED-14, no. 2, pp. 182-6, Feb. 2015, <https://doi.org/10.1038/nmat4148>.
- [7] Agarwal H, Kushwaha P, Lin YK, Kao MY, Liao YH, Dasgupta A, Salahuddin S and Hu C, "Proposal for capacitance matching in negative capacitance field-effect transistors," in *IEEE Electron Device Letters*, vol. ED-40, no. 3, pp. 463-6, Jan. 2019, 10.1109/LED.2019.2891540.
- [8] Kumar A and De Souza MM, "On the Dynamic characteristics of Ferroelectric and Paraelectric FETs," in *2018 IEEE 2nd Electron Devices Technology and Manufacturing Conference (EDTM)*, pp. 184-186, Mar. 2018, 10.1109/EDTM.2018.8421493.
- [9] Sentaurus Device User Guide, Version O-2018.06, Synopsys, Mountain View, CA, USA, Sep. 2018.
- [10] Agarwal H, Kushwaha P, Duarte JP, Lin YK, Sachid AB, Kao MY, Chang HL, Salahuddin S and Hu C, "Engineering negative differential resistance in NCFETs for analog applications," in *IEEE Transactions on Electron Devices*, vol. ED-65, no. 5, pp. 2033-9, Apr. 2018, 10.1109/TED.2018.2817238.