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Efficient Integration of Three-Phase Step Voltage Regulators in the Z-Bus Power Flow Method

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Abstract—This paper presents a comprehensive three-bus equivalent circuit model of three-phase step voltage regulators (SVRs). The proposed model can accurately simulate any SVR configuration and can be efficiently integrated in the Z-bus power flow method. Its distinct feature is that the taps are simulated outside the Y_{BUS} matrix in the form of current sources. As a result, the re-factorization of the Y_{BUS} matrix is avoided after every tap change reducing significantly the computational burden of the power flow analysis. Furthermore, possible convergence issues caused by the low impedance of SVRs are addressed by introducing fictitious impedances, without, however, affecting the accuracy of the model. The proposed SVR model is validated in the IEEE 4-Bus and an 8-Bus network, while its performance is further investigated in the IEEE 8500-Node test feeder.

Index Terms—Autotransformer, compensation technique, implicit Z_{BUS} power flow, step voltage regulator, tap variations, Y_{BUS} matrix factorization.

1. Introduction

STEP voltage regulators (SVRs) are widely applied to low- (LV) and medium-voltage (MV) distribution networks to maintain voltages within permissible limits. They consist of autotransformers with adjustable turn ratios connected in several configurations e.g open-delta, close-delta, wye [1].

Several methods have been proposed in the literature for the integration of SVRs in the power flow calculation [2]–[4]. More specifically, the authors in [2] and [3] propose a mathematical formulation relating the primary and secondary voltages and currents, which is solved using the backward/forward sweep (BFS) method. Furthermore, in [4], the SVR equations are directly integrated in the Jacobian matrix. However, these approaches are not applicable to the Z-Bus power flow method since the SVR equations of [2]–[4] are not compatible with the formation of Y_{BUS} matrix. The Z-Bus power flow approach is a fixed-point iterative method, which is widely applied in distribution network applications, due to its high robustness, fast convergence, ease of implementation and low computation time [5]–[9]. Therefore, accurate and computationally efficient modelling of SVRs is significant in order for the Z-Bus method to maintain its superior characteristics.

Several SVR models have been proposed in the literature so far, to be implemented in the three-phase implicit Z-Bus power flow. A comprehensive SVR model is proposed in [1], which is applicable in all SVR

configurations, while an open-delta SVR model is proposed in [10]. Although the aforementioned models are applicable in the Z-Bus power flow approach, the tap variables of SVR are simulated in the Y_{BUS} matrix of the network. As a result, the re-factorization (or inversion) of the Y_{BUS} matrix, which is the most time-consuming action of power flow is required to be executed after every tap variation.

The compensation technique is usually implemented in the Z_{BUS} power flow to avoid the re-factorization of the Y_{BUS} matrix every time that one or more elements change [11]. According to this technique, the variable elements are modeled as fictitious current sources outside the Y_{BUS} matrix, thus the Y_{BUS} matrix remains always constant. This technique is applied in [7] and [11] to simulate transformers equipped with on-load tap changer (OLTC) in balanced networks (using single-phase power flow) and by the authors in [12] to simulate three-phase OLTC transformers in Y_g - Y_g configuration. However, in case of the SVRs, the implementation of the compensation technique results in the divergence of the power flow, due to the small impedance of SVRs. Similar conclusions about the divergence issues associated with the modeling of SVRs are derived in [13].

This paper proposes a novel model, which overcomes the aforementioned divergence issues. The proposed model consists of a 3-bus equivalent circuit, which presents the following distinct characteristics:

- It simulates the taps of SVR as fictitious current sources outside the Y_{BUS} matrix, thus avoiding its continuous re-factorization after every tap variation. This property is very important in several real-time distribution management system (DMS) applications that require sequential tap variations e.g state estimation [14], optimal power flow (OPF), Volt/Var control (VVC), optimal feeder reconfiguration (OFR) [11], voltage stability analysis, heuristic optimization [15]. With the proposed 3-Bus SVR model, the DMS applications could be significantly accelerated.

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- It is generic and can be applied in all SVR configurations i.e., wye, open-delta, closed-delta and types of SVRs i.e., Type A and Type B.
- The proposed model presents accurate power flow results since the applied equations are derived considering the exact three-phase SVR circuit. Simulation results confirm that the proposed model outputs identical power flow results with OpenDSS and Simulink.
- Although the taps are simulated in the form of current sources, the convergence of power flow is not compromised. Simulation results in Section 6.2 indicate that the proposed model presents identical convergence speed with the model of [1], which implicitly considers the taps inside the Y_{BUS} matrix.

The rest of the paper is structured as follows: Section 2 explains the difference between the impedance value of an autotransformer and a two-winding transformer. Section 3 presents the proposed SVR model, while Section 4 explains how it is integrated in the Z-Bus power flow. Section 5 validates the proposed SVR model against Simulink and OpenDSS. Finally, Section 6 tests the performance of the proposed SVR model, while Section 7 concludes the paper.

2. Impedance of autotransformers

Before we proceed with the analysis of the proposed SVR model, it is important to clarify the difference between a two separate winding transformer and an autotransformer. Fig. 1 depicts an ideal two-winding transformer and an ideal autotransformer. The impedances of the transformers are denoted as Z_{2wT} and Z_{auto} and they include the total leakage impedance of the primary and the secondary winding referred to the secondary winding. The primary voltage (V_1), the secondary voltage (V_2) and the number of turns of the primary windings (N_1) are identical for both transformers.

Fig. 1. Two-winding transformer (left) and autotransformer (right).

Voltages and turn numbers for the two types of transformers can be determined according to (1) and (2).

$$\frac{V_2}{V_1} = \frac{N_{2wT}}{N_1} \Rightarrow N_{2wT} = \frac{V_2}{V_1} \cdot N_1 \quad (1)$$

$$\frac{V_2}{V_1} = \frac{N_{auto} + N_1}{N_1} \Rightarrow N_{auto} = \frac{V_2}{V_1} \cdot N_1 - N_1 \quad (2)$$

It can be observed that the number of turns of secondary windings (N_{2wT} and N_{auto}) differs for the two transformer types. Furthermore, assuming that the two transformers have an equal magnetic reluctance, the corresponding impedance ratio for the two transformer types is given by (3).

$$\frac{Z_{auto}}{Z_{2wT}} = \left(\frac{N_{auto}}{N_{2wT}} \right)^2 \quad (3)$$

By combining (1)-(3), (4) is derived, which gives the impedance ratio of the two types of transformer, as a function of the output/input voltage ratio (V_2/V_1).

$$\frac{Z_{auto}}{Z_{2wT}} = \left(\frac{\frac{V_2}{V_1} - 1}{\frac{V_2}{V_1}} \right)^2 \quad (4)$$

Fig. 2 depicts the impedance ratio of the two transformer types with respect to the output/input voltage ratio. The figure is obtained using (4) for an output/input voltage ratio between 0.9 and 1.1, which is a typical voltage range for SVRs. It can be observed that the autotransformer presents significantly lower impedance than the two-winding transformer. As a result of the low impedance of the autotransformer, the Z_{BUS} power flow diverges when the compensation technique is applied to the SVR modeling [13].

3. Proposed SVR model

Fig. 3 shows an SVR of Type A in closed-delta connection. The SVR is connected between buses p and s . Z_{auto} represents the autotransformer impedance of each phase. To overcome the divergence issues resulted from the low impedance of Z_{auto} , an additional fictitious bus m is added in the 2-Bus circuit of Fig. 3, forming the 3-Bus circuit depicted at the top of Fig. 4. Moreover, an impedance (Z_{add}) is added in series with Z_{auto} so that $Z_{pmi} = Z_{auto} + Z_{add}$ for $i = \{a, b, c\}$. To cancel out the influence of the impedance Z_{add} , an impedance of opposite value ($-Z_{add}$) is also added in series so that $Z_{msi} = -Z_{add}$. The additional impedances Z_{add} and $-Z_{add}$ do not affect the power flow results since they are connected in series with opposite signs, thus they cancel each other. Nevertheless, they significantly enhance the power flow convergence, enabling the compensation technique to be applied in the SVR modeling.

Fig. 2. Impedance ratio with respect to the output/input voltage ratio.

Fig. 3. Conventional 2-Bus circuit of type A SVR in closed-delta formation.

Fig. 4. Proposed 3-Bus circuits for SVRs of type A. From top to bottom: a) Closed-delta, b) Open-delta, c) Wye configuration.

By applying simple circuit analysis in Fig. 4, (5a) and (5b) are derived:

$$\begin{bmatrix} I_{pm} \\ I_{mp} \end{bmatrix} = \begin{bmatrix} Y_{pm} \cdot (I_d + K) & -Y_{pm} \\ -Y_{pm} \cdot (I_d + K) & Y_{pm} \end{bmatrix} \cdot \begin{bmatrix} V_p \\ V_m \end{bmatrix} + \begin{bmatrix} I_N \\ 0 \end{bmatrix} \quad (5a)$$

$$I_N = A \cdot Y_{pm} \cdot (-V_m + (I_d + K) \cdot V_p) \quad (5b)$$

where the matrices A, K, Y_{pm} are defined in Tables 1 and 2 for all types and configurations of SVRs. I_d is a 3x3 identity matrix. Eq. (5a) is used to calculate the currents (I_{pm}, I_{mp}) and voltages (V_p, V_m) between the nodes $p-m$, while (5b) is employed to calculate the current (I_N) flowing through the primary windings (N_j). Note that (5a) and (5b) are generic and can be applied to any SVR by simply modifying the parameters A, K, Y_{pm} based on the type (A or B) and configuration (closed-delta, open-delta, wye), as shown in Tables 1 and 2. The winding ratios ($\frac{n_1}{N_1}, \frac{n_2}{N_2}, \frac{n_3}{N_3}$) in Table 1 are related to the tap ratios (Tap_j) as follows [2]: $\frac{n_j}{N_j} = 0.00625 \cdot Tap_j$ for $j = \{1, 2, 3\}$, assuming that $Tap_j = \{-16, \dots, 0, \dots, +16\}$ and $-0.1 < \frac{n_j}{N_j} < 0.1$.

The square matrix in (5a) includes the matrix K , which is not constant due to the tap variations. Therefore, it is moved

outside the square matrix and (6a) is obtained, where the current sources I_p, I_m are given in (6b).

$$\begin{bmatrix} I_{pm} \\ I_{mp} \end{bmatrix} = \begin{bmatrix} Y_{pm} & -Y_{pm} \\ -Y_{pm} & Y_{pm} \end{bmatrix} \cdot \begin{bmatrix} V_p \\ V_m \end{bmatrix} + \begin{bmatrix} I_p \\ I_m \end{bmatrix} \quad (6a)$$

$$\begin{bmatrix} I_p \\ I_m \end{bmatrix} = \begin{bmatrix} A \cdot Y_{pm} \cdot (-V_m + (I_d + K) \cdot V_p) + Y_{pm} \cdot K \cdot V_p \\ -Y_{pm} \cdot K \cdot V_p \end{bmatrix} \quad (6b)$$

Finally, the voltages and currents between the nodes $m-s$ are expressed in (7), where the matrix Y_{ms} is given in Table 2.

$$\begin{bmatrix} I_{ms} \\ I_{sm} \end{bmatrix} = \begin{bmatrix} Y_{ms} & -Y_{ms} \\ -Y_{ms} & Y_{ms} \end{bmatrix} \cdot \begin{bmatrix} V_m \\ V_s \end{bmatrix} \quad (7)$$

Eqs. (6) and (7) can be comprehensively expressed in the form of an equivalent circuit as shown in Fig. 5. The parameters of the equivalent circuit for both types of SVR are given in Tables 1, 2, and 3. The square blocks of Fig. 5 consisting of Y_{pm}, Y_{ms} are constant and are included in the Y_{BUS} matrix. The tap variables are comprised in the current sources, outside the Y_{BUS} matrix.

As shown in Table 3, the current sources depend on the matrices Y_{pm}, Y_{ms} . To ensure the convergence of the power flow, the values of these matrices should be sufficiently small so that the current sources do not take an extremely large value. That is achieved by selecting a sufficiently large value of Z_{add} . Essentially, the role of Z_{add} is to enhance the convergence by artificially increasing the value of Z_{auto} .

Fig. 5. Equivalent 3-Bus circuit of the proposed SVR model.

Table 1

Matrices K and A for several configurations and types of SVR

SVR Type	Matrix	Open-Delta	Closed Delta	Wye
A or B	K	$\begin{bmatrix} \frac{n_1}{N_1} & 0 & -\frac{n_1}{N_1} \\ 0 & \frac{n_2}{N_2} & -\frac{n_2}{N_2} \\ 0 & 0 & 0 \end{bmatrix}$	$\begin{bmatrix} \frac{n_1}{N_1} & -\frac{n_1}{N_1} & 0 \\ 0 & \frac{n_2}{N_2} & -\frac{n_2}{N_2} \\ -\frac{n_3}{N_3} & 0 & \frac{n_3}{N_3} \end{bmatrix}$	$\begin{bmatrix} \frac{n_1}{N_1} & 0 & 0 \\ 0 & \frac{n_2}{N_2} & 0 \\ 0 & 0 & \frac{n_3}{N_3} \end{bmatrix}$
		$\begin{bmatrix} \frac{n_1}{N_1} & 0 & 0 \\ 0 & \frac{n_2}{N_2} & 0 \\ -\frac{n_1}{N_1} & -\frac{n_2}{N_2} & 0 \end{bmatrix}$	$\begin{bmatrix} \frac{n_1}{N_1} & 0 & -\frac{n_3}{N_3} \\ -\frac{n_1}{N_1} & \frac{n_2}{N_2} & 0 \\ 0 & -\frac{n_2}{N_2} & \frac{n_3}{N_3} \end{bmatrix}$	$\begin{bmatrix} \frac{n_1}{N_1} & 0 & 0 \\ 0 & \frac{n_2}{N_2} & 0 \\ 0 & 0 & \frac{n_3}{N_3} \end{bmatrix}$

Table 2

Y matrices for several configurations and types of SVR

Type	Matrix	Open-Delta	Closed-Delta	Wye
A	Y_{pm}	$\begin{bmatrix} Z_{auto} + Z_{add} & 0 & 0 \\ 0 & Z_{auto} + Z_{add} & 0 \\ 0 & 0 & Z_{add} \end{bmatrix}^{-1}$	$\begin{bmatrix} Z_{auto} + Z_{add} & 0 & 0 \\ 0 & Z_{auto} + Z_{add} & 0 \\ 0 & 0 & Z_{auto} + Z_{add} \end{bmatrix}^{-1}$	$\begin{bmatrix} Z_{auto} + Z_{add} & 0 & 0 \\ 0 & Z_{auto} + Z_{add} & 0 \\ 0 & 0 & Z_{auto} + Z_{add} \end{bmatrix}^{-1}$
B	Y_{ms}	$\begin{bmatrix} -Z_{add} & 0 & 0 \\ 0 & -Z_{add} & 0 \\ 0 & 0 & -Z_{add} \end{bmatrix}^{-1}$	$\begin{bmatrix} -Z_{add} & 0 & 0 \\ 0 & -Z_{add} & 0 \\ 0 & 0 & -Z_{add} \end{bmatrix}^{-1}$	$\begin{bmatrix} -Z_{add} & 0 & 0 \\ 0 & -Z_{add} & 0 \\ 0 & 0 & -Z_{add} \end{bmatrix}^{-1}$

Table 3

Current sources for the two types of SVR

SVR Type	I_p	I_m	I_s
A	$A \cdot Y_{pm} \cdot (-V_m + (I_d + K) \cdot V_p) + Y_{pm} \cdot K \cdot V_p$	$-Y_{pm} \cdot K \cdot V_p$	0
B	0	$Y_{ms} \cdot K \cdot V_s$	$A \cdot Y_{ms} \cdot (V_m - (I_d - K) \cdot V_s) - Y_{ms} \cdot K \cdot V_s$

Table 4

Validation of the proposed model against Simulink for the type A SVR

	Open-Delta			Closed-Delta			Wye		
	$ V_{4ab} $	$ V_{4bc} $	$ V_{4ca} $	$ V_{4ab} $	$ V_{4bc} $	$ V_{4ca} $	$ V_{4an} $	$ V_{4bn} $	$ V_{4cn} $
Simulink	13183.73427	12936.56756	13430.15426	13804.36230	13261.03079	13474.00390	7835.31967	7385.21215	7417.952216
Proposed	13183.75038	12936.57385	13430.15983	13804.36244	13261.03156	13474.00456	7835.31980	7385.21264	7417.942290
OpenDSS	13183.75023	12936.56993	13430.16003	13804.36231	13261.03192	13474.00233	7835.31908	7385.21250	7417.941969

Table 5

Validation of the proposed model against Simulink for the type B SVR

	Open-Delta			Closed-Delta			Wye		
	$ V_{4ab} $	$ V_{4bc} $	$ V_{4ca} $	$ V_{4ab} $	$ V_{4bc} $	$ V_{4ca} $	$ V_{4an} $	$ V_{4bn} $	$ V_{4cn} $
Simulink	13272.17655	12969.62611	13567.70840	13974.97510	13290.82893	13590.54690	7915.22523	7403.58178	7436.69034
Proposed	13272.17802	12969.62880	13567.70988	13974.97740	13290.82899	13590.54697	7915.22509	7403.58377	7436.68188
OpenDSS	13272.17697	12969.62745	13567.71039	13974.97788	13290.82897	13590.55012	7915.22361	7403.58423	7436.68374

4. Implementation of the proposed SVR model in a 4-Bus network: An example

In this section, the implementation of the proposed model is practically explained in the 4-Bus network of Fig. 6a. A closed delta SVR of type A is connected between the nodes 2-3. Z_{auto} is the SVR impedance, while Z_{12i} and Z_{34i} for $i = \{a, b, c\}$ are the line impedances connecting the buses 1-2 and 3-4, respectively. The conventional SVR configuration is shown in Fig. 6a, while the proposed SVR model is depicted in Fig. 6b. As shown, the proposed SVR model has an additional fictitious bus 5. Note that no load is connected to this fictitious bus. Buses 2, 5 and 3 correspond to buses p , m and s of Fig. 5, respectively. The impedance $Z_{25i} = Z_{auto} + Z_{add}$, while $Z_{53i} = -Z_{add}$ for $i = \{a, b, c\}$, as explained in Section 3. The networks of Figs. 6a and 6b are identical since $Z_{25i} + Z_{53i} = Z_{auto}$.

The network of Fig. 6b is described by (8), as follows:

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \end{bmatrix} = \begin{bmatrix} -Y_{12} & Y_{12} & 0 & 0 & 0 \\ Y_{12} & -Y_{12} - Y_{25} & 0 & 0 & Y_{25} \\ 0 & 0 & -Y_{53} - Y_{34} & Y_{34} & Y_{53} \\ 0 & 0 & Y_{34} & -Y_{34} & 0 \\ 0 & Y_{25} & Y_{53} & 0 & -Y_{25} - Y_{53} \end{bmatrix} \cdot \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{bmatrix} \quad (8)$$

The square matrix of (8) includes the 3x3 admittance matrices of the lines between the buses 1-2 (Y_{12}) and 3-4 (Y_{34}) as well as the 3x3 matrices Y_{25} and Y_{53} calculated according to Table 2. The voltage vectors of (8) for each bus $k = \{1, 2, 3, 4, 5\}$ are given by $V_k = [V_{ka}, V_{kb}, V_{kc}]^T$. The current vectors of (8) are given in (9). Each vector $[I_{Lra}, I_{Lrb}, I_{Lrc}]^T$ for $r = \{1, 2, 3, 4\}$ denotes the load currents of node r , while $[I_{ya}, I_{yb}, I_{yc}]^T$ for $y = \{2, 5, 3\}$ denote the compensating currents calculated by Table 3 and include the tap variables of SVRs. More specifically,

$[I_{2a}, I_{2b}, I_{2c}]^T$ corresponds to I_p , $[I_{5a}, I_{5b}, I_{5c}]^T$ corresponds to I_m , while $[I_{3a}, I_{3b}, I_{3c}]^T$ corresponds to I_s .

$$\begin{aligned} I_1 &= [I_{L1a}, I_{L1b}, I_{L1c}]^T, \\ I_2 &= [I_{L2a}, I_{L2b}, I_{L2c}]^T + [I_{2a}, I_{2b}, I_{2c}]^T, \\ I_3 &= [I_{L3a}, I_{L3b}, I_{L3c}]^T + [I_{3a}, I_{3b}, I_{3c}]^T, \\ I_4 &= [I_{L4a}, I_{L4b}, I_{L4c}]^T, \\ I_5 &= [I_{5a}, I_{5b}, I_{5c}]^T \end{aligned} \quad (9)$$

The equation system (8) is then solved with the implicit Z_{BUS} method, as described in [5] and [6]. Selecting a sufficiently large value of Z_{add} , the compensating currents in (9) are adequately small to ensure the convergence of the power flow.

5. Validation of the proposed SVR model

5.1 IEEE 4-Bus network with 1 SVR

The proposed SVR model is applied in the Z_{BUS} power flow method of [5] and the results are validated against Simulink and OpenDSS in the IEEE 4-Bus network [17]. Some clarifications about the applied parameters are provided below:

- The unbalanced loads of [17] are used in this paper. In Open-Delta and Closed-Delta configuration the loads are phase-to-phase connected, while in wye configuration they are phase-to-neutral.
- The SVR is placed in the position of the transformer, between the buses 2-3 [17]. The impedance of the SVR (Z_{auto}) is calculated based on the data of the single-phase two-winding transformer given in [17], which has the following parameters: $V_{base} = 7.2kV$, $S_{base} = 2MVA$, $z = 0.01 + 0.06j$ (pu). Hence, in physical units $Z_{2WT} = 0.26 + 1.55j$ Ohm. According to the analysis of section 2, $Z_{auto} \leq 0.01 \cdot Z_{2WT}$, thus $Z_{auto} \leq 0.0026 + 0.0155j$ Ohm. It is noted, that although the SVR impedance varies with the tap settings of SVR, we assume it is constant. The inaccuracy

introduced by this assumption is negligible, due to the very low value of Z_{auto} .

- The taps applied in the simulation are as follows: $(Tap_1, Tap_2, Tap_3) = (16, 8, 8)$. Note that in open delta configuration Tap_3 does not exist.

The results of the proposed model, Simulink and OpenDSS are contrasted in Table 4 for the SVR of type A, and in Table 5 for the SVR of type B. Indicatively, only the phase-to-phase (or phase-to-neutral) voltages of the 4th node are depicted here. The remaining nodes present similar accuracy. As shown, the results of the proposed approach are in full agreement with those of Simulink and OpenDSS confirming the accuracy of the proposed model.

Fig. 6. From top to bottom: a) 4-Bus network with the conventional SVR configuration between the buses 2-3 and b) 4-Bus network with the proposed SVR modeling.

5.2 8-Bus network with 3 SVRs

Fig. 7. Unbalanced 8-Bus MV network consisting of 4 constant impedance loads and 3 SVRs.

The proposed SVR model is further validated in the 8-Bus network of Fig. 7, consisting of 3 SVRs and 4 unbalanced constant impedance loads. It is a 4-wire network with the following assumptions: 1) every bus is considered perfectly grounded, 2) the mutual impedance between the neutral and phase conductors is zero. The parameters of the network are quoted in Table 6, while the loads are given in Table 7. The taps of SVRs for the simulated configurations are presented in Table 8.

The proposed approach is compared against Simulink and the results are presented in Table 9. Indicatively, only the voltage magnitude of the three phases of bus 8 are depicted, nevertheless, the remaining buses present similar accuracy. In Table 9, the results of the proposed approach are presented in regular font, the results of Simulink in bold,

while the results of OpenDSS in red color. As shown, although the network consists of 3 SVRs, the proposed model produces almost identical steady-state power flow results with Simulink and OpenDSS confirming its accuracy.

Table 6

Parameters of 8-Bus network

Distance of the lines	5 km
Phase-to-neutral Voltage of slack bus	7200 V
Frequency of the network	50 Hz
Resistance of the lines (per phase)	0.4 Ω /km
Self-reactance of the lines (per phase)	0.3 Ω /km
Mutual-reactance between phase conductors	0.1 Ω /km
Impedance of SVRs	0 Ohm

Table 7

Loads of 8-Bus network

Load Bus 3	$Z_{La} = 250 \Omega$ in parallel with $j1000 \Omega$ $Z_{Lb} = 250 \Omega$ in parallel with $j1000 \Omega$ $Z_{Lc} = 250 \Omega$ in parallel with $j1000 \Omega$
Load Bus 5	$Z_{La} = 250 \Omega$ in parallel with $j1000 \Omega$ $Z_{Lb} = 125 \Omega$ in parallel with $j500 \Omega$ $Z_{Lc} = 250 \Omega$ in parallel with $j1000 \Omega$
Load Bus 7	$Z_{La} = 150 \Omega$ in parallel with $j600 \Omega$ $Z_{Lb} = 100 \Omega$ in parallel with $j400 \Omega$ $Z_{Lc} = 150 \Omega$ in parallel with $j600 \Omega$
Load Bus 8	$Z_{La} = 250 \Omega$ in parallel with $j1000 \Omega$ $Z_{Lb} = 250 \Omega$ in parallel with $j1000 \Omega$ $Z_{Lc} = 250 \Omega$ in parallel with $j1000 \Omega$

Table 8

Taps of SVRs (Tap_1, Tap_2, Tap_3) for the simulated configurations

	SVR 1	SVR 2	SVR 3
Wye Type A	(8, 10, 8)	(8, 10, 8)	(8, 10, 8)
Open Delta Type A	(8, 8, -)	(8, 8, -)	(8, 8, -)
Close Delta Type A	(8, 10, 8)	(8, 10, 8)	(8, 10, 8)
Wye Type B	(8, 10, 8)	(8, 10, 8)	(8, 10, 8)
Open Delta Type B	(8, 8, -)	(8, 8, -)	(8, 8, -)
Close Delta Type B	(8, 10, 8)	(8, 10, 8)	(8, 10, 8)

Table 9

Phase-to-neutral voltages calculated with the proposed method, Simulink and OpenDSS for the 8-Bus network using several SVR configurations

	Phase A	Phase B	Phase C
Wye Type A	7331.1433 7331.1831 7331.0209	7244.2791 7244.3462 7244.2303	7450.4267 7450.4712 7450.3029
Open Delta Type A	7784.6505 7784.6936 7784.6967	7576.6246 7576.7013 7576.5696	6468.4454 6468.4729 6468.5091
Close Delta Type A	7799.5715 7799.5704 7799.4528	7845.3272 7845.3521 7845.2551	7880.3313 7880.3782 7880.1900
Wye Type B	7377.7522 7377.7209 7377.6269	7312.6066 7312.6144 7312.5579	7500.9205 7500.9656 7500.7956
Open Delta Type B	7858.3033 7858.3470 7858.1504	7649.9001 7649.9796 7649.7734	6463.4446 6463.4717 6463.4885
Close Delta Type B	7874.3123 7874.3141 7874.3046	7960.3695 7960.3946 7960.4086	7948.5619 7948.6069 7948.5285

6. Performance of the proposed model

The performance of the proposed SVR model is tested in the IEEE 8500-Node network. The topology of IEEE 8500-network is shown in Fig. 8. It includes originally 4 SVRs and 4 capacitor banks. For the sake of simplicity, all capacitor banks are considered OFF. SVR 1 is connected in wye configuration, SVR 2 in open delta configuration, while SVRs 3 and 4 are connected in closed delta configuration. SVR 1, SVR 2, SVR 3 and SVR 4 are connected between the buses 1-2, 405-406, 1057-1058 and 1311-1312, respectively. To get a sense about the position of each bus inside the network, their distance from the substation is presented in Fig. 9. More details about the data of the network e.g lines, loads are provided in [17]. All buses of the network are considered perfectly grounded.

Fig 8. The IEEE 8500-node network. It consists of 4 capacitor banks and 4 SVRs. The outputs of the SVRs are connected to the following buses: SVR 1→Bus 2, SVR 2→Bus 406, SVR 3→Bus 1058, SVR 4→Bus 1312.

Fig 9. Distance of the buses of the IEEE 8500-node network from the substation [6, supplementary material].

6.1 Convergence properties of the proposed SVR model

The convergence characteristics of the proposed model are presented here, with respect to the values of the additional impedance Z_{add} introduced in Section 3. Fig 10 depicts indicatively the phase A-to-neutral voltage at the output of the 1st SVR throughout the iterative process of power flow, for several values of Z_{add} . Although in Fig. 10 Z_{add} takes only inductive values, similar results are derived with resistive values of similar magnitude. It is clarified that a flat start was considered for all the nodes of the network. Based on the figure, the following observations are derived:

- For low Z_{add} values (see Fig. 10a) the Z-Bus power flow diverges. This is expectable due to the large values of Y_{pm}, Y_{ms} (see Table 2), which in turn increase unacceptably the current sources of Fig. 5 (see Table 3).
- The algorithm presents fast convergence for all $Z_{add} \geq 0.5j$, as shown in Fig. 10b. Thus, Z_{add} can be arbitrarily selected over a very wide range of values.
- The algorithm converges to the same solution for all $Z_{add} \geq 0.5j$. This is logical since an impedance $-Z_{add}$ is connected in series with Z_{add} , canceling completely the influence of Z_{add} .

6.2 Comparison of the proposed SVR model against the conventional 2-Bus model of [1]

The performance of the proposed SVR model is further validated against the model presented in [1] using the IEEE 8500-node test network. Moreover, a comparison between the two models with respect to the convergence speed is carried out.

The phase-to-neutral voltage profiles of the network, using the proposed model and the model of [1] for simulating the SVRs, is shown in Fig. 11. The tap variables of the three phases (Tap_1, Tap_2, Tap_3) for the 4 SVRs are assumed as follows: SVR 1→ (14, 12, 10), SVR 2→ (14, 12, -), SVR 3→ (14, 12, 10), SVR 4→ (14, 12, 10). It is noted that the Tap_1, Tap_2, Tap_3 regulate the winding number of n_1, n_2, n_3 , respectively, according to Fig. 4. As shown in Fig. 11, the proposed SVR model produces an identical voltage profile with the model of [1], confirming again the validity of the proposed model in a large-scale network.

The convergence of the 4 SVRs throughout the iterative power flow process is depicted in Figs. 12-15 for varying taps. More specifically, the tap variables are changing every 30 iterations according to Table 10. At the first iteration, a flat start was considered. The value of Z_{add} (see Section 3) of all SVRs is arbitrarily selected equal to $Z_{add} = 5j$. As expected, the two models converge to exactly the same solutions with the same convergence speed. Therefore, it is confirmed that the adoption of equivalent current sources for expressing the tap variables instead of including them into the Y_{BUS} matrix, does not affect the convergence of the power flow, if a suitable value of Z_{add} is selected.

A huge difference exists in the computation time between the proposed and the model of [1], as result of the refactorization of the Y_{BUS} matrix from the model of [1] after each tap change. More specifically, when the proposed SVR model is applied, the total computation time of the power flow process of Figs. 12-15 is 45s (namely 90 iterations x 0.5s/iterations). It is pointed out that the initial Y_{BUS} factorization is not counted in the computation time since it is usually executed offline. On the opposite, when the SVR model of [1] is applied, the total computation time is 177s. Please note that the computation time of each matrix factorization is 66s measured in Matlab. The additional computation time of ref. [1] is caused from the Y_{BUS} factorizations that are required to be executed at 31th and 61th iterations as a result of the tap variations. It is reminded that the two-bus equivalent model of [1] expresses the tap variables inside the Y_{BUS} matrix, thus, every tap change requires the execution of Y_{BUS} factorization. A summary of

the computation time of the proposed model and the model of [1] is given in Table 11.

Fig. 10. Phase-to-neutral voltage of phase A at the output of the 1st SVR, during the iterative power flow process. From top to bottom: a) low Z_{add} values, b) large Z_{add} values

Table 10

Tap settings of the SVRs throughout the iterative process

Iteration range	SVR 1	SVR 2	SVR 3	SVR 4
(0-30)	(16, 16, 16)	(16, 16, -)	(16, 16, 16)	(16, 16, 16)
(31-60)	(9, 7, 6)	(9, 7, -)	(9, 7, 6)	(9, 7, 6)
(61-90)	(14, 12, 10)	(14, 12, -)	(14, 12, 10)	(14, 12, 10)

Table 11

Total computation time

	Proposed	Ref. [1]
Computation time of power flow iterations	45s (90 x 0.5s)	45s (90 x 0.5s)
Computation time of Y_{BUS} factorization at 31 th and 61 th iteration	0s	132s (2 x 66s)
Total computation time	45s	177s

Fig. 11. Voltage Profile of the IEEE 8500-node network, using the proposed and the model of [1] to simulate the SVRs.

Fig. 12. Convergence process of SVR 1, when the taps change every 30 iterations, according to Table 10.

Fig. 13. Convergence process of SVR 2, when the taps change every 30 iterations, according to Table 10.

Fig. 14. Convergence process of SVR 3, when the taps change every 30 iterations, according to Table 10.

Fig. 15. Convergence process of SVR 4, when the taps change every 30 iterations, according to Table 10.

7. Conclusion

This paper presents a novel 3-Bus equivalent circuit for modeling three-phase SVRs for the Z_{BUS} power flow. The model is applicable in all SVR configurations. Its advantage is that the tap variables are expressed in the form of current sources outside the Y_{BUS} matrix, avoiding its re-factorization or inversion after each tap change. The proposed model has been compared against the conventional SVR model, (expressed as a 2-bus equivalent circuit) offering significant speed up in applications, where continuous tap variations are required. The proposed SVR model can constitute an important simulation tool in several DMS applications such as state estimation, OPF, VVC, OFR, voltage stability, heuristic optimization, in which the power flow is executed multiple times in a specific time with continuously varying tap settings.

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