Understanding the Input Signal Frequency Effects on the Resistive Window of Memristors

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Abstract— As theoretically predicted by Prof. Chua, the input signal frequency has a major impact on the electrical behavior of memristors. According with one of the so-called fingerprints of such devices, the resistive window, *i.e.* the difference between the low and high resistance states, shrinks as the frequency increases for a given input signal amplitude. Physically, this effect stems from the incapability of ions/vacancies to follow the external electrical stimulus. In terms of the electrical behavior, the collapse of the resistive window can be ascribed to the shift of the set/reset voltages toward higher values. Moreover, for a given frequency, the resistance window increases with the signal amplitude. In this letter, we show that both phenomena are the two sides of the same coin and that can be consistently explained after considering the snapback effect and a balance model equation for the device memory state.

Index Terms—memristor, resistive switching, frequency.

I. INTRODUCTION

ACCORDING to [1] and [2], a memristive device exhibits three major fingerprints: *i)* a pinched hysteresis loop in the current-voltage (I - V) plane, *ii)* the decrease of the hysteresis lobe area as the input signal frequency increases, and *iii)* the shrinking of the pinched hysteresis loop to a single-valued function when the frequency tends to infinite. In terms of the resistive switching (RS) mechanism, the latter two points can be understood as the mutual approach of the low (LRS) and high (HRS) resistance states as the frequency increases. Not only the signal frequency takes part in this problem but also its amplitude needs to be considered. As is well known, for a fixed frequency, the magnitude of the hysteretic current-voltage (I - V) loop increases as the signal amplitude increases (see Fig. 1(a)). In practice, the transitions occur at two voltage levels often referred to as the set (V_S) and reset (V_R) voltages which are regarded as fixed values [3]. Similarly, the I - V loop increases as the signal frequency decreases (see Fig. 1(b)) and for a very high frequency, the I - V curve collapses to a purely resistive behavior. The ratio between the LRS and HRS currents measured at a low fixed bias is referred to as the resistive window of the device and

Fig. 1. Schematic effect of (a) the input signal amplitude V_i and (b) the input signal frequency f on the memristor I - V characteristic. Experimental I - V curves for (c) increasing positive voltage amplitude from 0.4V to 1.1V (10 cycles each condition) and for (d) increasing ramp rate from 1V/s to 1MV/s (100 cycles each condition).

when properly normalized to unity as its memory state window. Then, one can talk about the collapse of the memory window when the input signal amplitude is decreased and the frequency increased [3]-[5]. It is clear that both aspects of the phenomenon have the same root, *i.e.* the ion/vacancy displacements within the insulating layer and the formation and rupture of an atomic-size conducting bridge in between the electrodes [6]-[8]. Physically, the collapse of the memory window can be attributed to the incapability of ions/vacancies to follow the input signal [9],[10]. Electrically, the effect is linked to the shift of the transition voltages, V_{TS} and V_{TR} , toward higher values. These issues have been thoroughly investigated in the past for constant and ramped voltage input signals [11]-[14] but a theoretical approach able to deal with arbitrary input signals is still an almost unexplored terrain.

In this letter, the effects of the input signal frequency and amplitude on the hysteretic I - V curves of memristive devices are investigated. The memory window collapse is demonstrated for HfO_2 -based MIM structures. On the basis of Chua's theory, a simple phenomenological memristor model formed by two coupled equations is proposed. The model takes into account the snapback effect in the I - V characteristic and assumes a dynamic balance-type equation for the memory state of the device. We show that the proposed approach provides a consistent framework for understanding the role played by the signal frequency and amplitude applied to memristors.

This work was supported by the Spanish Ministry of Science, and Innovation and the FEDER program through projects TEC2017-84321-C4-1-R and TEC2017-84321-C4-4-R. M. Maestro-Izquierdo, J. Suñé and E. Miranda are with the Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona, 08193 Cerdanyola del Vallès, Spain (e-mail corresponding author: marcos.maestro@uab.cat). M. B. Gonzalez and F. Campabadal are with the Institut de Microelectrònica de Barcelona, IMB-CNM, CSIC, 08193 Cerdanyola del Vallès, Spain.

II. DEVICES AND EXPERIMENTAL DETAILS

The devices used in this work are TiN(200nm)/Ti(10nm)/HfO₂(10nm)/W(200nm) structures with area 5×5μm². The input signal was applied to the top electrode with the bottom electrode grounded. Details about the device fabrication and electroforming processes can be found in [12], [13]. Two kinds of ramped voltage experiments were carried out varying specific parameters in each case. In the first experiment (see Fig. 1(c)), the maximum positive voltage amplitude was ranged from 0.4V to 1.1V ($RR \sim 0.3V/s$) while the maximum negative amplitude was fixed to -1.5V ($RR \sim 0.4V/s$) in order to induce the complete reset of the device after each cycle. RR is the ramp rate. In the second experiment (see Fig. 1(d)), RR was varied from 1V/s to 10⁶V/s keeping the positive and negative maximum voltage amplitudes fixed to 1.1V and -1.4V, respectively. As illustrated in Figs. 2(a) and 3(a), the median of the I - V curves shown in Figs. 1(c) and 1(d) were corrected for the snapback and snapforward effects ($V-I \cdot R_S$) using a series resistance R_S [15]–[17]. Figure 2(b) shows the dependence of V_{TR} on R_S for the different applied signals. The crossover point indicates the optimum value for R_S . Regardless of the signal amplitude, the transition voltages are approximately the same ($V_{TS} \sim V_{TR} \approx 0.5V$) for $R_S \approx 450\Omega$. Figure 2(c) shows the progressive increase of the memory window with the signal amplitude. In case of the frequency variation, $V_{TS,TR}$ are no longer constant (see Fig. 3(a)) and the cycle-to-cycle variability (C2C) must be taken into account. Figure 3(b) shows the weibits for the individual V_{TS} and V_{TR} values. Remarkably, both data sets can be fitted using the Burr's XII (also called clustering) distribution [18]:

$$F(V) = 1 - \left(1 + \frac{1}{\alpha_{S,R}} \left(\frac{V}{V_{TS,TR}} \right)^{\beta_{S,R}} \right)^{-\alpha_{S,R}} \quad (1)$$

where F is the cumulative distribution function, $\alpha_{S,R}$ the clustering, $\beta_{S,R}$ the shape, and $V_{TS,TR}$ the scale (transition voltages) parameters for set and reset, respectively. The obtained fitting parameters values are $\beta_S = 75$ with $0.35 < \alpha_S < 2.0$ and $\beta_R = 65$ with $0.45 < \alpha_R < 1.3$. While β takes into account the intrinsic C2C variability, α is related to the extrinsic one (different initial conditions for HRS and LRS). Notice that for $\alpha \rightarrow \infty$, (1) yields the Weibull distribution. Figures 3(c) and 3(d) show, respectively, that $V_{TS,TR}$ and R_S linearly increase with $\ln(RR)$. While the first result is a well-known experimental observation [19], [20], the second one points out that R_S is similarly affected by RR . This is not surprising since both behaviors are ultimately ruled by the same mechanism, *i.e.* the ion/vacancy displacements [21]. This indicates that R_S or at least part of R_S is associated with the filamentary structure itself [16] and should not be regarded as a completely external artifact [15]. Finally, Fig. 3(e) shows the collapse of the resistive window with RR as predicted by Chua. Notice the asymmetric reduction of the resistive window largely caused by the R_S effect on the LRS current. As it will be discussed next, both effects shown in Figs. 2 and 3 can be interpreted as the two sides of the same coin.

III. MODEL DESCRIPTION AND DISCUSSION

In this Section, a simple phenomenological model which

Fig. 2. (a) Intrinsic I - V curves (median) and (b) reset transition voltage as a function of R_S . (c) LRS and HRS experimental currents measured at -0.1V as a function of the positive signal amplitude.

Fig. 3. (a) Intrinsic I - V curves (median) for different input signal ramp rates (1V/s to 10MV/s). (b) Weibit plot for the experimental V_{TS} (solid symbols) and V_{TR} (open symbols) voltages and their corresponding fitting curves (solid lines) using (1). (c) Scale factors V_{TS}, V_{TR} , (d) series resistance R_S and (e) LRS and HRS currents measured at -0.1V as a function of the ramp rate RR .

contains all the ingredients necessary to understand the collapse of the resistive window is presented. The first equation, which is related to the electron transport and which accounts for the snapback/snapforward effect discussed above, is expressed as:

$$I(V) = G_C(g) \cdot V_C = G_C(g) \cdot [V - I(V) \cdot R_S] \quad (2)$$

where $G_C(g) = g_{\min} \cdot (-\frac{1}{2} - g) + g_{\max} \cdot (-\frac{1}{2} + g)$ is the constriction conductance, $-\frac{1}{2} \leq g \leq \frac{1}{2}$ the memory state, V_C the voltage drop across this constriction, V the applied voltage, and $g_{\min}$ and $g_{\max}$ fitting parameters for the minimum and maximum conductances, respectively. From (2), the I - V curve reads:

$$I(V) = \frac{G_C(g)}{1 + G_C(g) \cdot R_S} V \quad (3)$$

(3) expresses that the behavior of the I - V characteristic is dictated by two frequency-dependent factors, G_C and R_S . The second equation deals with the memory state of the device [22] and is expressed in terms of the low voltage-normalized conductance g as a symmetric balance model:

$$\frac{dg}{dt} = \frac{\frac{1}{2} - g}{\tau_S(V_C)} - \frac{\frac{1}{2} + g}{\tau_R(V_C)} \quad (4)$$

where $\tau_{S,R}$ are characteristic times associated with the set and

Fig. 4. (a) Equivalent circuit model for equation (4), where the memory state, g , is represented by the current flowing through the RL circuit. Memory state for a sinusoidal signal with increasing amplitude ($f=1\text{Hz}$) (b) and frequency ($V_{AMP}=1\text{V}$) (c). Typical simulated intrinsic I - V curves (d) for different ramped voltage amplitudes and (e) for different RR . (f) Evolution of the memory window, Δg , as a function of f and V_{AMP} .

reset transitions. Assuming ion/vacancy hopping transport [23], [24]:

$$\tau_{S,R}(V_C) = \tau_{OS,OR} \cdot \exp\left(-\frac{|V_C|}{V_{OS,OR}}\right) \quad (5)$$

where $\tau_{OS,OR}$ and $V_{OS,OR}$ are fitting parameters of the model. Remarkably, (4) can be represented by the equivalent circuit model shown in Fig. 4(a), where g is the current flowing through the circuit. For the sake of simplicity, in what follows, identical $\tau_{S,R}$ parameters will be considered for both positive and negative biases. Figures 4(b) and 4(c) show the hysteretic behavior of g for sinusoidal signals with different amplitude and frequency. Notice how the resulting hysteresis or memory loops agree with the experimental results reported in Section II. More in detail, Figs. 4(d) and 4(e) illustrate simulated I - V curves using (3) and (4).

Importantly, to our knowledge, analytic results for a time-varying signal in (4) can only be found for the case of a linearly increasing or decreasing positive and negative ramps. Again, for the sake of simplicity, let's consider only the set region of the device. Solving (4) for $V_C = RR \cdot t$, yields the double exponential expression:

$$g(t) = \left(g_0 - \frac{1}{2}\right) \exp\left\{-\frac{V_{OS}}{RR \cdot \tau_{OS}} \left[\exp\left(\frac{RR \cdot t}{V_{OS}}\right) - 1\right]\right\} + \frac{1}{2} \quad (6)$$

where $g_0 = g(t=0)$ is the initial memory condition. Considering the inflection point of (6), $d^2g/dV_C^2 = 0$, as the reference transition voltage, we obtain:

$$V_{TS} = V_{OS} \ln(RR) + V_{OS} \ln\left(\frac{\tau_{OS}}{V_{OS}}\right) \quad (7)$$

which provides the linear relationship shown in Fig. 3(c). For our devices (HfO_2), $V_{OS} = 1.3 \cdot 10^{-2} \text{V}$ and $\tau_{OS} = 2.97 \cdot 10^9 \text{s}$ are obtained. Moreover, for a cycled ramped voltage signal with maximum amplitude V_{AMP} and frequency f , $V_C = 4 \cdot V_{AMP} \cdot f \cdot t$, so

that from (6) we can look for the initial condition g_0 required for a stationary loop as $g(1/4f) = 0$. This simple exercise provides the amplitude of the memory window Δg as a function of V_{AMP} and f (see Fig. 4(f)):

$$\Delta g = 2g_0 = \exp\left\{\frac{V_{OS}}{4 \cdot V_{AMP} \cdot f \cdot \tau_{OS}} \left[\exp\left(\frac{V_{AMP}}{V_{OS}}\right) - 1\right]\right\} - 1 \quad (8)$$

which, again, is in total agreement with the expected phenomenology for memristive devices.

IV. CONCLUSIONS

In this letter, the dependence of the memory state (resistance) window on the input signal amplitude and frequency was investigated. It was shown that the behavior of the I - V characteristic of HfO_2 -based memristors can be understood as the combined action of two frequency-dependent factors, *i.e.* a series resistance effect and a phase lag effect in the diffusive movement of ions/vacancies.

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