Memristive State Equation for Bipolar Resistive Switching Devices Based on a Dynamic Balance Model and its Equivalent Circuit Representation

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Abstract

A memory state equation consistent with several experimental observations is presented and discussed within the framework of Chua's memristive systems theory. The proposed equation describes the evolution of the memory state corresponding to a bipolar resistive switching device subjected to a variety of electrical stimulus.

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***Abstract*— A memory state equation consistent with several experimental observations is presented and discussed within the framework of Chua's memristive systems theory. The proposed equation describes the evolution of the memory state corresponding to a bipolar resistive switching device subjected to a variety of electrical stimulus. It is shown that our approach is consistent with: *i*) the characteristic switching time associated with the ions/vacancies displacement within dielectric films, *ii*) the SET/RESET voltage dependence on the voltage sweep ramp rate, *iii*) the hysteretic nature of the memory state as a function of time and voltage for arbitrary input signals, *iv*) the generation of self-similar hysteron loops for different initial conditions, and *v*) the collapse of the memory window with the increment of the input signal frequency. It is also shown that the proposed equation admits a circuital representation suitable for circuit simulations.**

***Index Terms*—memristor, resistive switching, memory**

I. Introduction

A central issue in L. Chua's memristive devices theory is the definition of the memory state (λ-t) represented by a first order time differential equation [1]. This equation in combination with an expression for the current-voltage (I-V) characteristic describes the hysteretic behavior observed in many oxide-based resistive switching (RS) devices [2,3]. The memory equation (ME) relates to the nonvolatile system's conduction properties and is physically associated in the case of CBRAMs/OxRAMs with the metal ions/oxygen vacancies displacement (heavy particles flow) within the dielectric film caused by the application of an external electrical stimulus [4]. The I-V relationship describes the specific electron transport mechanism (light particles flow) considered in the conducting filament (CF). In general, the picture resembles cars (electrons) passing across a drawbridge (ions/vacancies) with variable load capacity (λ). Since the first proposal of a memristive ME by Strukov *et al.* [5] many others followed [6-8]. The introduction of a window function in the ME acting as a boundary condition for λ represented a breakthrough in the modeling of the SET/RESET transitions but the approach was demonstrated to be not exempted of serious mathematical drawbacks [9,10]. Interestingly, even for nonlinear electron transport, the memory state λ is a measure of the device conductance in the low-voltage region which contains all the information relevant to whole I-V curve [11,12]. However, beyond the many efforts carried out in the last decade, there is still no consensus on which ME better represents a wide spectrum of RS behaviors. Here, we explore up to what extend the ME can be simplified without sacrificing the constraints imposed by experiments. Of course, as happens with any other model, the elaboration of an analytic approach dismisses a large number of particularities which cannot be covered by a basic general framework. We show that the proposed model is consistent with several experimental observations for a variety of input signals including constant, ramped, pulsed and sinusoidal. To the best of our knowledge, this thorough analysis was not carried out before and demonstrates that simplicity, dimensional considerations, and symmetry arguments are essential ingredients for seting up a well-posed physical and mathematical model for RS devices.

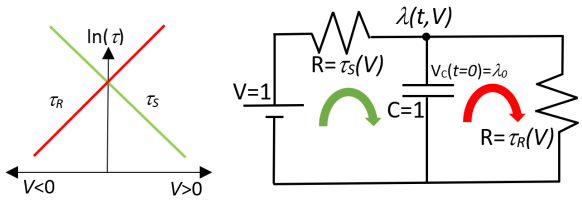

Fig.1: a) Schematic model for the SET (green) and RESET (red) characteristic switching times given by (2). b) Equivalent circuit model for the balance differential equation (1). λ is the memory state (voltage) and λ_0 its initial value.

The central points of this new development are: first, we eliminate the so-called hysteron structure for the memory state as presented in [11,12]. Here, the proposed ME generates the hysteretic memory map by itself without *ad hoc* definitions. Second, we demonstrate through an in-depth analysis of its derivative that the proposed ME equation coinciliates both the static and dynamic switching conditions [2], and third, we show that the proposed ME not only has a compact recursive solution for the whole memory loop but also that it complies with Chua's observation regarding the collapse of the memory window with the signal frequency [1]. In addition, we show that the reported ME admits a simple equivalent circuit representation. This is of utmost importance for circuit simulations in which the timestep parameter is under the control of the simulator itself and not in hands of the user.

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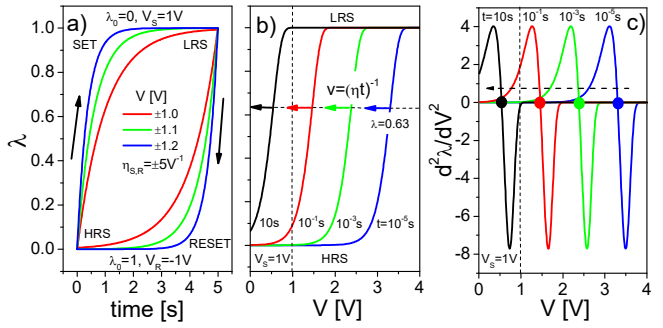

Fig.2: a) Potentiation and depression characteristics for constant voltage input, b) Evolution of the positive ridge function, c) Inflection point of $\lambda(V)$.

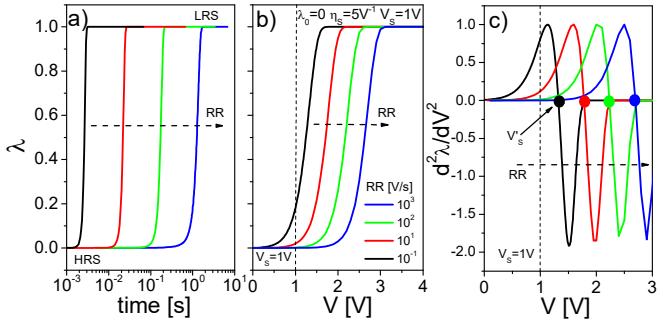

Fig.3: a) Effect of *RR* on the positive ridge function as a function of time, b) SET voltage shift, c) Evolution of the inflection point of $\lambda(V)$ (normalized).

II. Memory State Equation and Circuital Approach

The simplest first order time differential equation for λ satisfying dynamic balance, dimensional homogeneity, and long-term self-saturating behavior with end values 1 (LRS: low resistance state) and 0 (HRS: high resistance state) for opposite biases reads:

$$\frac{d\lambda}{dt} = \frac{1-\lambda}{\tau_S(\lambda,V)} - \frac{\lambda}{\tau_R(\lambda,V)} \tag{1}$$

where $\tau_{S,R}$ [s] are characteristic times associated with the SET (V>0) and RESET (V<0) transients. We assume for $\tau_{S,R}$ a voltage dependence of the form (see Fig.1.a):

$$\tau_{S,R}(V) = exp\left[-\eta_{S,R}\left(V - V_{S,R}\right)\right] \tag{2}$$

where $\eta_{S,R}$ [V^{-1}] and $V_{S,R}$ [V] are the transition rates (η_S>0, η_R<0) and the reference switching voltages (V_S>0, V_R<0), respectively. Any dependence of $\tau_{S,R}$ on λ in (2) requires the use of a circuit simulator. Notice that (2) is a convenient approximation since $\tau_{S,R}(V=0)=\infty$ would be ideally expected (infinite retention time) [13]. In any case, for typical parameter values, the balance equation (1) yields $d\lambda/dt(V=0)\approx 0$ as required for the equilibrium state. (1) has also been used in the past but in connection with physical parameters of the CF [14-17], not as a general memory state variable. Before solving (1) for some cases of particular interest, it is worth pointing out that its mathematical structure is that of an RC circuit with V-dependent resistors (see Fig.1.b). At the end, this will allow us to solve λ for arbitrary input signals. λ corresponds to the voltage drop across the capacitor C=1F (this is not a physical capacitor) with initial voltage λ_0. This representation replaces the V-controlled memory subcircuits considered in many memristor models [10].

III. Model Results and Analysis

Let us focus now on some relevant analytic results for the SET transition (V>0). Corresponding results for RESET (V<0) can be obtained *mutatis mutandis*.

i) Memory state evolution under constant voltage input signal

Neglecting the second term in the right-hand side of (1) and considering a constant voltage V>0 applied across the device, we find:

$$\lambda(t,V) = (\lambda_0 - 1)exp\{-t/\tau_S(V)\} + 1 \tag{3}$$

which has attractor 1 as $t\to\infty$ regardless of λ_0 and τ_S. As shown in Fig.2.a, (3) and its counterpart for V<0 (not shown here), describe the typical potentiation/depression effect in a synaptic cell [18]. If we identify the SET time τ_S' with the inflection point of (3) as a function of V, $d^2\lambda/dV^2$=0, we obtain:

$$\tau_S'(V) = exp[-\eta_S(V - V_S)] = \tau_0 exp(-V/V_0) \tag{4}$$

which coincides with the original expression (2) corresponding to the voltage-acceleration law for metal ions/oxygen vacancies displacement [19-23]. As illustrated in Figs.2.b and 2.c, this can be alternatively visualized as the time required by the point $\lambda=(\lambda_0-1)exp(-1)+1$ (λ=0.63 for λ_0=0) in the travelling ridge function to reach the SET voltage condition (vertical dashed line). Within this picture, the inflection point moves towards the left with non-uniform velocity $v=(\eta t)^{-1}$ [Vs^{-1}]. $\tau_0=exp(\eta_S V_S)$ [s] and $V_0=1/\eta_S$ [V] in (4) are constants of the model and can be found experimentally [24].

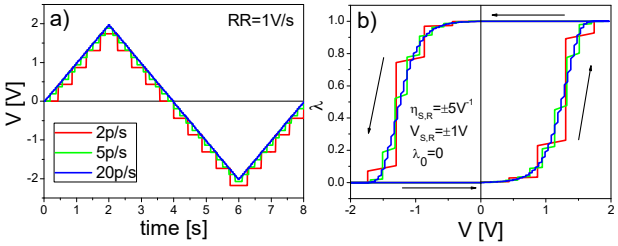

Fig.4: a) Pulsed signals with different number of pulses per second, b) Hysteron structure generated as a function of the applied bias using (7).

ii) Memory state evolution under a linear voltage sweep

Now, if we let $V=RR\cdot t$, with RR>0 [Vs^{-1}] the ramp rate, (1) can be integrated in terms of V>0 (see Figs. 3.a and 3.b):

$$\lambda(V) = (\lambda_0 - 1)exp\left\{-\frac{V_0}{\tau_0 RR}\left[exp\left(\frac{V}{V_0}\right) - 1\right]\right\} + 1 \tag{5}$$

As in *i*), the SET voltage V_S' corresponds to the condition $d^2\lambda/dV^2$=0 (Fig. 3.c), yielding:

$$V_S' = V_0 \ln(RR) + V_0 ln\left(\frac{\tau_0}{V_0}\right) \tag{6}$$

which expresses the well-known V_S-ln(RR) linear relationship [4,25-28]. Remarkably, (6) provides the link between the dynamical and static switching condition case given by (4).

iii) *Hysteretic behavior for arbitrary input signals*

In the case of an arbitrary input signal $V(t)$ (positive or negative, continuous or discontinuous, derivable or not), (3) can be discretized following the recursive scheme:

$$\lambda_{t+1} = [\lambda_t - H(V_t)]exp\{-\Delta t/\tau_{S,R}(V_t)\} + H(V_t) \qquad (7)$$

where Δt is the timestep considered between the states t and t+1, V_t the voltage applied during this time, and $H(x)$ the Heaviside function. Notice that (7) is suitable for dealing with excitations formed by train of pulses with varying amplitude and different pulse rates as illustrated in Figs. 4.a and 4.b. In the continuous limit, (7) naturally generates the sigmoidal hysteron structure λ-V (positive and negative ridge functions) introduced in [11,29,30]. In the present approach, this mathematical structure is no longer required.

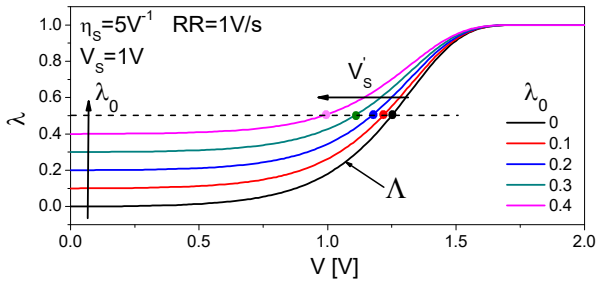

Fig.5: Major and minor positive ridge functions. Symbols are the SET voltages as a function of the initial condition λ_0.

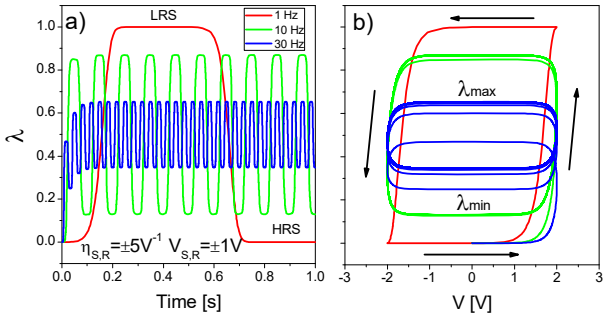

Fig.6: a) Evolution of λ for different input frequencies, b) Collapse of the memory window for a sinusoidal signal with fixed amplitude A=2V.

iv) *Self-similar loops and role played by the initial condition*

As showed in [31], major (maximum voltage excursion) and minor (bounded voltage excursions) memory loops exhibit self-similar properties. The positive ridge function for the major loop Λ is obtained from (5) considering λ_0=0:

$$\Lambda(V) = 1 - exp\left\{-\frac{V_0}{\tau_0 RR}\left[exp\left(\frac{V}{V_0}\right) - 1\right]\right\} \qquad (8)$$

Minor λ loops with arbitrary initial conditions (see Fig.5) can be expressed as affine transformations of Λ since:

$$\lambda(V) = (1 - \lambda_0)\Lambda(V) + \lambda_0 \qquad (9)$$

In other words, this means that the properties found for the major loop propagate to the minor loops after appropriate scaling. If we adopt a definition for the SET condition based on the current magnitude (λ=0.5 for instance) instead of on the voltage, Fig. 5 reveals that V'_S reduces as λ_0 increases. This indicates that more leaky devices switch on first [32].

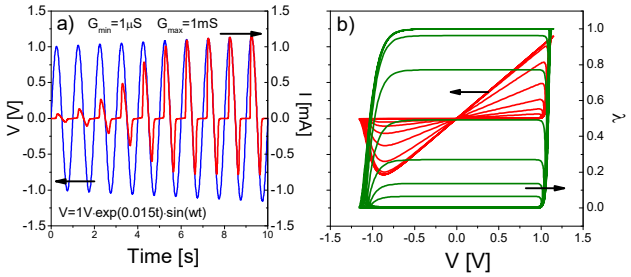

Fig.7: a) Effect of an increasing sinusoidal voltage (blue line) on the current (red) as a function of time. b) Corresponding evolution of the memory state (green) and generation of intermediate states in the I-V characteristic (red).

v) *Memory window vs input signal frequency*

A natural consequence of (6) is the collapse of the memory window (difference between λ_{max} and λ_{min} in the attractor curve) as the input signal frequency increases [1,33,34]. Figure 6 illustrates the effect of a sinusoidal voltage with constant amplitude A and frequency ω on the hysteretic behavior of λ. These results were obtained using the circuit shown in Fig.1.b. From (6), it is clear that for any signal of amplitude A, ideally, one can always find a sufficiently large RR such that $V_S' > A$. This corresponds to a partial SET condition which limits the maximum excursion of λ. Physically, the collapse of the memory window is often attributed to the inability of ions/vacancies to follow the input signal [35,36]. This connection is theoretically demonstrated here using an experimentally validated voltage-acceleration law for the hopping time of the heavy particles, eq. (4).

IV. Simulation of the I-V Characteristic

This final Section illustrates how the memory state λ is linked to a specific electron transport model. For the sake of simplicity, a linear I-V characteristic was chosen [5], but more complex behaviors are acceptable [12]. In this case:

$$I = [(1 - \lambda)G_{min} + \lambda G_{max}]V \qquad (10)$$

where G_{min} and G_{max} [S] are the minimum and maximum conductance values, respectively, achievable without inducing irreversible damage to the device. These parameters are required to calibrate the model with the experimental HRS and LRS curves. Typical simulations results for I-t and I-V showing intermediate conduction states are depicted in Figs. 7.a and 7.b.

V. Conclusions

In this letter, a dynamic balance model for the memory equation of memristive devices exhibiting the bipolar resistive switching mode is proposed. The model complies with several experimental observations related to the switching voltages and times. Because of its simple mathematical structure, the model can be described in terms of an equivalent circuit with voltage-dependent components. This property makes the proposed approach very useful for circuit simulation environments.

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