Modeling and Analysis of Sub-Millimeter-Wave Graphene Switches for On-Wafer Coplanar Transmission Lines

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Abstract

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Modeling and Analysis of Sub-Millimeter-Wave Graphene Switches for On-Wafer Coplanar Transmission Lines

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***Index Terms*—Graphene, terahertz, millimeter-waves, switches, modeling, transmission lines**

I. Introduction

Millimeter-wave (mmWave) and terahertz (THz) frequencies (100 GHz-3 THz) have been widely exploited for a variety of applications including high-throughput communications, sensing, and imaging, due to their small wavelength and ample bandwidth [1]-[8]. In such applications, reconfiguration, especially through switching, is crucial in enabling radio-frequency (RF) signal processing including carrier modulation/encoding or beam steering in antenna arrays [9]-[15]. At mmWave/THz frequencies, switches can provide many practical solutions without residing to the complexity of more traditional devices, including mixers or phase shifters. For example, a switch can be integrated on an antenna to enable direct signal control and provide 1- or 2-bit quantized phase modulation [9]-[15]. These configurations are mainly categorized as either coded phased arrays (e.g. 1-bit digital phased arrays [9][10]) or reflective surfaces (e.g. reflectarrays [11]-[15]). Such reconfigurable apertures carry out frequency independent beamforming, while retaining low DC power consumption and RF losses compared to traditional phased array systems [16]. Moreover, these reconfigurable multi-element antenna arrays, which are expected to dominate in at higher frequencies, are less prone to phase quantization errors compared to smaller ones [17]. Switches can typically achieve simpler modulation schemes (e.g. 1-bit phase or amplitude modulation); however, spectral efficiency is not necessarily a requirement at mmWave/THz bands, where bandwidth can be orders of magnitude larger than lower RF.

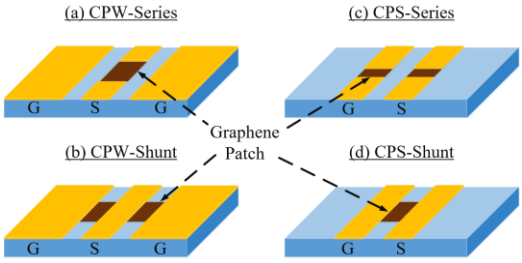

Fig. 1 The proposed CPW and CPS graphene loaded transmission line configurations.

State-of-the-art switches are based on CMOS, SiGe, GaAs, and InP technologies [18]-[28], and provide insertion loss (IL) less than 3 dB with switching ratios (R) up to 15 dB at 300 GHz. However, the downsides of such switch devices are 1) their limited cutoff frequencies (typically less than 300-500 GHz) and 2) the fabrication cost increases dramatically when integrated into large arrays with thousands of elements because of the chip real-estate cost [29]. Specifically, the performance of the aforementioned switches is limited by the parasitics and mobility constraints exhibited in mmWave/THz frequencies (at room temperatures) [30]. To compensate for these limitations, more advanced technology nodes are required, thus increasing the fabrication cost significantly. For example, mmWave/THz reconfigurable reflectarrays with an aperture of 20 mm × 20 mm can host more than 1,600 antenna elements at 300 GHz ($\lambda/2$ sampling). To implement such an array with state-of-the-art methods requires at least 1,600 switches (one per antenna), which can be manually assembled as chips on the aperture (to reduce the cost) or have an entire wafer of 400 mm^2 with all the

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switches integrated. Therefore, scaling current technology becomes a cost and fabrication challenge for mmWave/THz multi-element arrays.

Alternatively, switching can be achieved with the use of tunable thin-film (2D or 2.5D) materials; the electromagnetic properties of which (e.g. sheet resistance or permittivity/permeability) can be tuned over a large bandwidth with the use of an external mechanism (e.g. external field biasing or heating). Such materials include ferrite [31], liquid crystals [32], molybdenum disulfide (MoS_2) [33], black phosphorus (BlPh) [34], vanadium dioxide (VO_2) [35]-[37], and graphene (GR) [38]-[49]. In the literature, MoS_2 and BlPh switches are currently limited to lower frequencies (<100 GHz) due to their high intrinsic impedances that demand for thin and long active device shapes to avoid excess losses; however, these configurations are highly affected by parasitics that become pronounced in high frequencies [33][34]. In addition, to the best of our knowledge, the fabrication of large-scale apertures with integrated switches demands for high-fabrication-yields, currently challenging with the use of these materials due to the growth and transfer processes [33][34]. Alternatively, VO_2 switches have been proposed in mmWave/THz bands with good performance (low insertion loss and high switching ratio) [35][36]; VO_2 conductivity is thermally regulated and has been mostly exploited in power limiting switching topologies. Nevertheless, VO_2 switching is sensitive to ambient temperature changes [37], a limiting factor for reliable compact multi-element designs that exhibit strong heat dissipation. In addition, the heaters of VO_2 switches require at least 20-50 mW per element [35], thus power consumption is expected to skyrocket in multielement configurations with hundreds or even thousands of integrated switches. Although thin-film materials are probably in their infant in terms of usage in mmWave/THz applications. Yet, there are indications that such tunable materials can provide key advantages over more traditional semiconductor technologies, including 1) wideband and higher cut-off frequency performance [37]-[43], 2) low-cost large-area fabrication [39][40], and 3) compatibility with standard substrate materials and nanofabrication tools [39].

In this study, we focus on graphene loaded (GL) coplanar transmission line (TL) switches, as illustrated in Fig. 1. Graphene is a 2D material that exhibits sheet resistance tunability over a great bandwidth (DC-1.5 THz) with the use of external biasing similarly to field-effect-transistors [38]-[49]. Additionally, the implementation of large-scale graphene reconfigurable apertures has been recently enabled with the development of a high-yield nanofabrication process that offers more than 92% yield over a large area [39][40]. Even though graphene has a relatively low switching ratio R_{biased}*=300 Ω/□* and $R_{unbiased}$*=1,500 Ω/□* [41]-[44], these sheet resistances are considerably lower than MoS_2 and BlPh, leading to designs with fewer constraints regarding the channel/active device size, therefore fewer parasitic effects at mmWave/THz bands. Several studies that propose graphene-loaded topologies include attenuators, switches, and reconfigurable power dividers [45]-[49]. These works include both experimental designs and/or theoretical studies for series or shunt configurations; however, an insight on the expected performance based on the configuration (series versus shunt topology) and the design parameters (e.g. characteristic impedance−Z_0 and graphene size) is missing. Specifically, the achievable ON/OFF ratio and insertion loss, when graphene is embedded in a switching topology, can differ from the sheet impedance ratio. For example, in [45], measurements up to 110 GHz of a shunt coplanar waveguide (CPW) graphene switch are presented, demonstrating the switching performance does not exceed 2 dB (*IL≈10 dB*). Conversely, in [47], a tunable graphene-based series microstrip attenuator is measured up to 20 GHz achieving switching ratio of 3-5 dB (*IL≈5 dB*). Thus, which is the maximum switching performance for graphene-based switches and under what limitations?

The goal of this work is to methodically study GL TL switches and reveal the dependence of their performance on design parameters, including transmission line characteristic impedance, graphene patch geometry, scaling effects, and topology (series versus shunt). A partial study with respect to the aforementioned parameters is carried out in [46], where the performance of a series graphene switch is studied only for variable graphene patch widths. On the other hand, existing studies use equivalent models for graphene devices [47]-[49]. Namely, in [47] an equivalent model is used to extract the graphene sheet impedance values from the measured S-parameters of a microstrip attenuator. Moreover, in [48], an equivalent model approach is exploited to identify the losses in GL TLs, by carrying out full-wave simulations and then using the *ABCD* parameters to extract the complex TL characteristics (complex-propagation constant and -characteristic impedance) for different frequencies. Finally, in [49] a one-port GL device is proposed and an equivalent model is used to extract the graphene sheet impedance values without investigating the effects of patch geometry on device performance. Nevertheless, no study examines in depth the switching performance with respect to the affecting parameters, especially for the various coplanar transmission line topologies presented in this work.

Herein, we model graphene using measured sheet impedance values (R_{biased}*=300 Ω/□* and $R_{unbiased}$*=1,500 Ω/□* [41]-[44]) instead of theoretical models to include phenomena that affect the sheet impedance switching performance (e.g. lattice defects, grain size, etc.). As such, we identify the GL TL geometry that offers the best switching performance with limited graphene biased/unbiased ratio. Herein, we focus our effort on GL coplanar waveguides and striplines (CPW and CPS) switches, since these TLs are frequently used in mmWave/THz integrated circuits (ICs) [50]-[53]. As such, we expand the theoretical models of the CPW and CPS TLs by incorporating the graphene sheet resistance. Furthermore, to identify the optimum switch topology using full-wave simulators based on multiple parameters is computationally intensive, especially for high-frequency circuits; therefore, the use of accurate equivalent models is a valuable tool for the design of multi-element configurations. Some prior results of this work are presented in [44]; however, that study is strictly limited to a brief discussion on general TL models (neither CPW nor CPS) and does not include the scaling effects and the parasitics of the devices. In

this work, we extend the analysis including the dependence of the switching performance on device scaling, characteristic impedance, and graphene shape, incorporated in CPW and CPS TLs in the presence of parasitics. Moreover, our models incorporate graphene as a distributed sheet impedance in Ω/□; hence, they can be exploited for other loaded topologies that use materials characterized by sheet impedance (e.g. VO_2, MoS_2 etc.). Additionally, the proposed models can be used for rapid optimization processes or in conjunction with machine learning algorithms, where the generation of many design points is required. For example, machine learning algorithms are leveraged to optimize the antenna topology under certain constraints (e.g. gain, VSWR, return loss, etc.) as shown in [54]; these algorithms could now be extended for graphene-actuated reconfigurable antennas with embedded switches, which could be modelled as proposed herein.

The rest of the paper is organized as follows: In section II, we analyze the GL TLs using lumped models. Then, in section III, we investigate the performance of GL CPW switches based on various parameters and identify the optimum topology in terms of the switch geometrical features including device scaling, graphene squares, and transmission line characteristic impedance. Afterward, in section IV, we further the analysis of GL CPS switches. Finally, in section V, we discuss the estimated performance of the coplanar switch configurations for 2D materials with a wider tuning range of the impedance sheet.

II. Lumped-Element Modeling of Graphene Switches

In this section, we demonstrate the performance dependence of graphene-loaded transmission line switches based on graphene shape, characteristic impedance, and topology (series versus shunt). The equivalent circuits of the series and shunt graphene switches are depicted in Fig. 2a and their respective scattering parameters [55] are given by

$$S_{11}^{series} = \frac{Z_{gr,sheet}/N}{2Z_o + Z_{gr,sheet}/N} = S_{22}^{series}$$
$$S_{21}^{series} = \frac{2Z_o}{2Z_o + Z_{gr,sheet}/N} = S_{12}^{series} \quad (1)$$

$$S_{11}^{shunt} = \frac{-Z_o}{2Z_{gr,sheet}/N + Z_o} = S_{22}^{shunt}$$
$$S_{21}^{shunt} = \frac{2\,Z_{gr,sheet}/N}{2Z_{gr,sheet}/N + Z_o} = S_{12}^{shunt} \quad (2)$$

where, $Z_{gr,sheet}$ is the sheet impedance of graphene in $\Omega/\square$ (R_{biased}=300 $\Omega/\square$ and $R_{unbiased}$=1,500 $\Omega/\square$ [44]) and N is the number of graphene squares oriented in a line vertical to the current flow ($N_{series}=w/l$ and $N_{shunt}=l/w$). Considering that graphene has a uniform current distribution due to small electrical size, the number of squares defines the total lumped impedance of the graphene; for example, if graphene is 5 squares, then R_{biased}=60 Ω and $R_{unbiased}$=300 Ω. Moreover, in (1) and (2) the S-parameters depend only in the number of squares N (ratio of w over l); thus, we do not account for any scaling effects, which are thoroughly presented in the following sections.

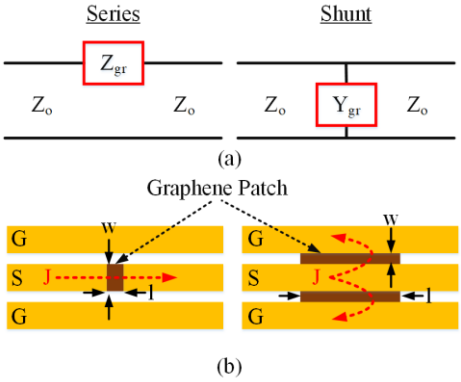

Fig. 2 (a) Graphene switches as lumped models (series and shunt) without parasitics and (b) the equivalent CPW topology paradigm (top view).

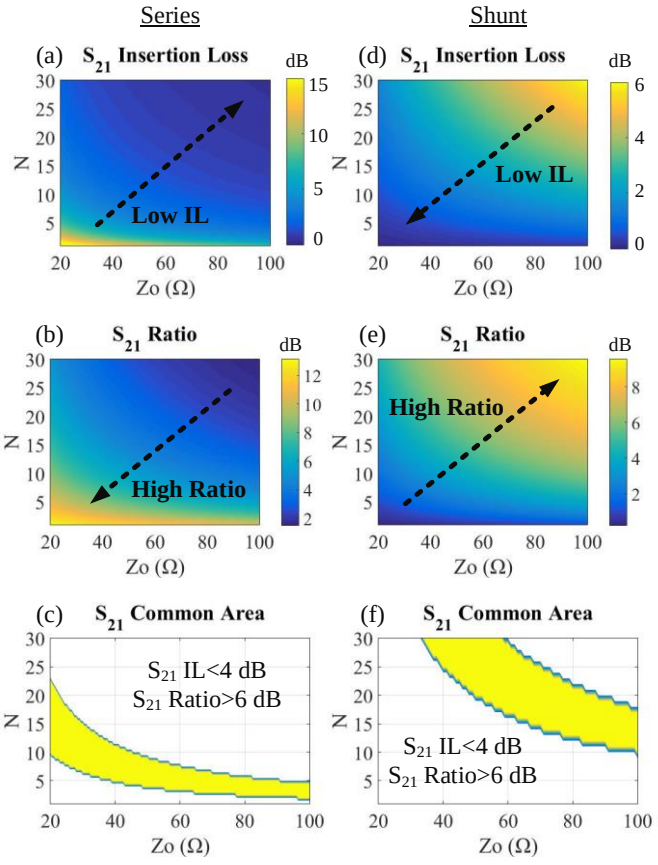

Fig. 3 The series/shunt switch topology (lumped): (a)/(d) Insertion loss, (b)/(e) ON/OFF ratio, and (c)/(f) the common area for given specifications.

The series (shunt) topology is in ON (OFF) state when graphene is biased and exhibits low impedance, thus leading to high (low) S_{21}. On the opposite, the series (shunt) switch is OFF (ON) when graphene is unbiased-(high impedance) and the S_{21} is low (high). The two switching performance metrics of interest are: i) insertion loss (S_{21}) for the ON state and ii) the S_{21} ratio between the ON and OFF states. Typically, improving the former reduces the latter and vice-versa. Therefore, switch design becomes a compromise between insertion loss and

ON/OFF ratio.

The inverse proportionality between the switching ratio and the IL is also evident when simulating the topologies for variable N and Z_0, as depicted in Figs. 3a-b,d-e. For specific switch operation (e.g. $IL<4$ *dB* and $R>6$ *dB*), we can identify the range of $\{N, Z_0\}$ that satisfies these conditions (see Figs. 3c&f).

We notice that both topologies can exhibit similar performance for the same graphene sheet impedance ratio (5 in this case). For example, if $Z_0=60\ \Omega$ and $IL=3$ *dB*, both configurations can exhibit a maximum ON/OFF ratio of 7 dB (for different squares). However, as shown in the latter sections, the comparison is not always accurate, since the lumped modelling does not include any scaling effects that limit the performance due to the presence of parasitics. The effects of these parasitics are pronounced in higher-frequencies, since they offer a better path for the currents that flow through the switch, thus mitigating the performance.

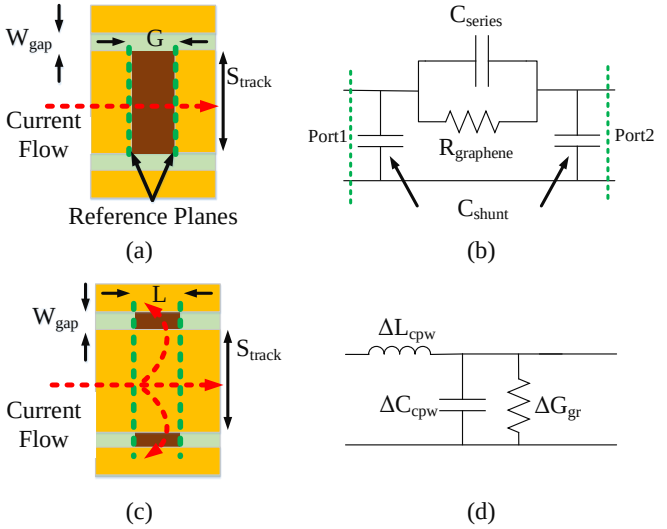

Fig. 4 The CPW (a) series and (c) shunt switch configurations (top-view) and in (b) and (d) the respective equivalent circuits.

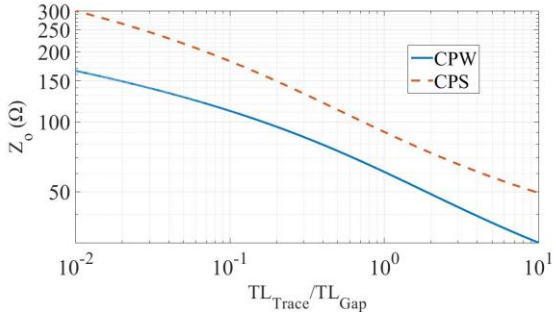

Fig. 5 The CPW and CPS characteristic impedance versus the TL trace over gap ratio [52].

III. Graphene Loaded CPW Switches

In this section, we expand the study of Section-II on the graphene switch performance, by including the scaling factor of the device for series and shunt topologies. The scaling factor affects the device parasitics (neglected in Section-II) and thus further investigation on the performance is needed with respect to the characteristic impedance, the number of graphene squares, and scaling factor. To carry out this study, we assume that the switches are implemented in a CPW topology, as depicted in Fig. 4.

A. Series CPW Topology

The series GL-CPW switch is modelled with an equivalent Π-network, as shown in Fig. 4b. The parasitic capacitances of the configuration depend on the geometrical features of the discontinuity [50]. Graphene sheet is modelled using a lumped resistor (Fig. 4b). The *ABCD* parameters of the series GL-CPW switch are [55]

$$ABCD = \begin{bmatrix} 1+\dfrac{Y_p}{Y_s} & \dfrac{1}{Y_p} \\ 2Y_p+\dfrac{Y_p^2}{Y_s} & 1+\dfrac{Y_p}{Y_s} \end{bmatrix} \quad (3)$$

where,

$$Y_s = \frac{X_s + R_{gr}}{X_s R_{gr}}, \quad Y_p = \frac{1}{X_p} \quad (4)$$

and,

$$X_s = 1/i\omega C_{series}, \quad X_p = 1/i\omega C_{shunt}, \quad and \ R_{gr} = Z_{gr,sheet}/N \quad (5)$$

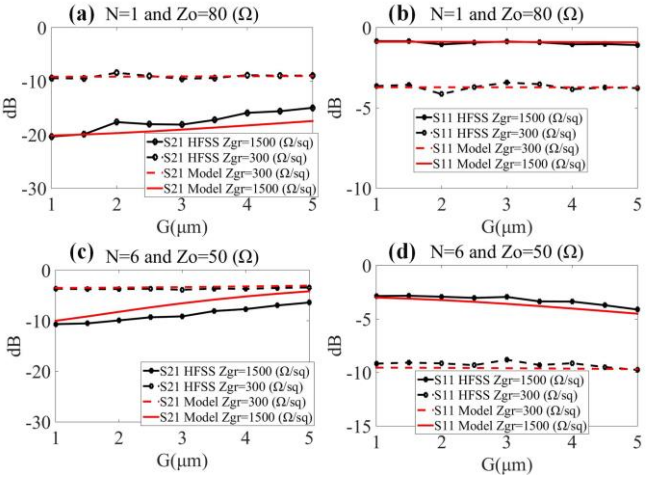

Fig. 6 The S_{21} and S_{11} comparison between the proposed series GL-CPW switch model and full-wave simulations for various configurations.

To evaluate the accuracy of our model, we carry out full-wave simulations using a commercial finite element method (FEM) solver [56]. In these simulations, we fix the number of graphene squares (N) and CPW Z_0 (we keep a fixed ratio of S_{track}/W_{gap} as shown in Fig. 5), and vary the device length/scaling factor (G). From the obtained results presented in Fig. 6, we observe that the model has good performance for various gap size (G) values. The discrepancy observed in Fig. 6c for high G values is due to the model inaccuracies of the parasitic capacitance obtained from [50]. Namely, the effect of fringing fields is neglected in the models of [50], thus they become inaccurate for greater G values. Moreover, if we followed the simplistic approach of Section II, the S-parameters (thus IL and ON/OFF ratio) of the devices would be constant

regardless of the scaling factor G, since (1)-(2) depend only on N and Z_0.

The simulation results are de-embedded using a thru-reflect-line (TRL) calibration [57], eliminating any mismatch effects of the FEM solver's ports. As such, for each of the G values, we simulated four configurations (3 TRL standards and 1 series GL-CPW switch). These simulations are carried out at 300 GHz and the substrate is high resistivity silicon (ε_r=11.9) (as for the rest of the paper), leading to dense meshes that increase the total simulation time. Namely, to obtain the S-matrix for each G-step of Fig. 6, approximately 3 minutes are needed (on a system with an Intel Xeon 6-core processor and 64 GB RAM). Therefore, if a design demands optimization based on N, Z_0, and G, with a fine step, the total full-wave simulation time becomes a bottleneck. Thus, the proposed models are an invaluable tool for the design of GL switches.

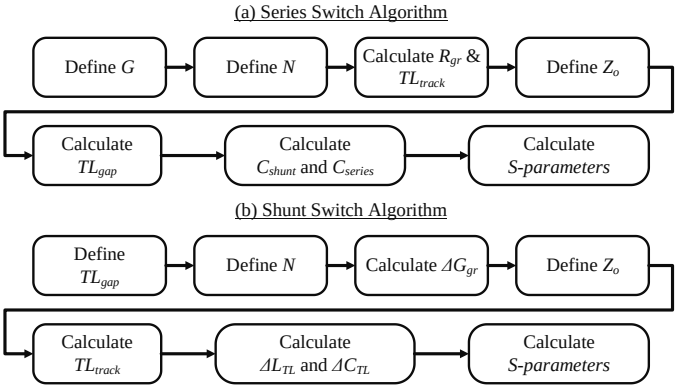

Fig. 7 The algorithms (a) series and (b) shunt, used to analyze the multi-dimensional problems based on the scaling factors, graphene squares, and Z_0.

The results of Fig. 6 are a small subset of the available topologies based on Z_0, N, and G parameters. Hence, to identify the performance based on all the incorporated parameters; we need to carry out a scan for all the available combinations {G, N, Z_0}. Explicitly, we use the algorithm given in Fig. 7a to calculate the S-parameters of the series GL-CPW switch. Z_0 (Fig. 5) is scanned between 20 and 120 Ω (S_{track}/W_{gap} ratio from 0.05 to 12), leading to low radiation losses and practically-sized features [52]. The obtained results are a 5-dimensional matrix (assuming the devices are reciprocal) that contains all the S-parameters for each available combination of {G, N, Z_0}, one for every switch state (ON/OFF). To observe the results, we first examine the IL and switching ratio of the series switch. For example, in Fig. 8a, the surfaces of constant IL (S_{21} ON) values are plotted; each point on these surfaces provides a combination of {G, N, Z_0}. Similarly, in Fig. 8b, surfaces of constant S_{21} ON/OFF ratio values determine the respective combination of {G, N, Z_0}. We notice that increasing the number of graphene squares N, decreases the IL but also decreases the switching ratio. Similar trends are noticed for the other two parameters G and Z_0, indicating that there is large design flexibility to achieve the desired specifications.

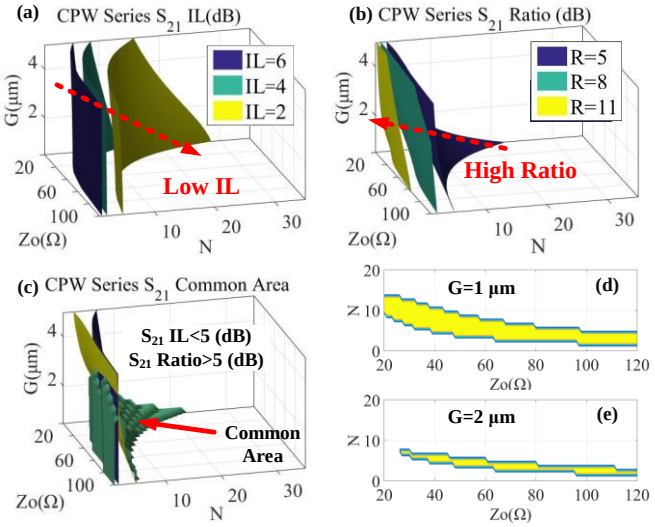

Fig. 8 The S_{21} parameters of the series GL-CPW switch: (a) insertion loss, (b) ON/OFF ratio, (c) common locus (volumetric) for given criteria, and (d)-(e) the slices of the volumetric locus for different G values.

In Fig. 8c, we depict the common area of {G, N, Z_0} that follow the exemplary specifications of $IL<5$ dB and switching ratio greater than 5 dB. These results suggest that the series GL-CPW switch depends on the gap size/scaling factor (G). Namely, in Fig. 8d-e, we depict slices, for different G values, of the common area from Fig. 8c. As expected, scaling the device size to smaller gap values decreases the parasitic effects, therefore, increasing the common area.

Examining the multi-dimensional data can be challenging to the designer and prioritizing specific parameters can help arrive faster in the desired switching topology. For example, by defining a desired/acceptable IL we can obtain the parameter space that satisfies the performance goal. As such, in Fig. 9 we present the ON/OFF ratio with respect to {G, N, Z_0} for fixed IL values, observing a tradeoff between the IL and ON/OFF ratio. These maps are very useful since the designer can identify the desired ON/OFF ratio for given IL and obtain the geometrical characteristics of the design. Additionally, using the proposed models we obtain more than 600,000 S-matrices for all the {G, N, Z_0} combinations, all these are calculated in less than 15 minutes using the proposed equivalent model. However, the same time using full-wave simulations would result in several months of run time.

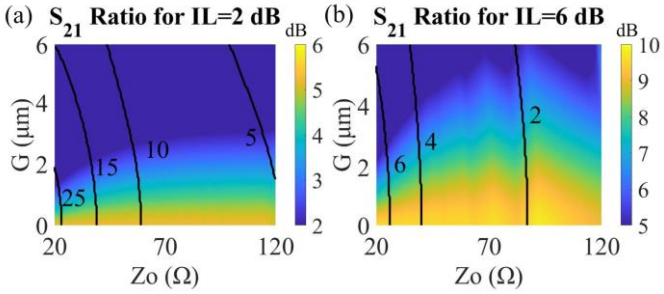

Fig. 9 The series GL-CPW switch 2D maps of ON/OFF ratio for fixed IL. With black contour, the number of squares is noted.

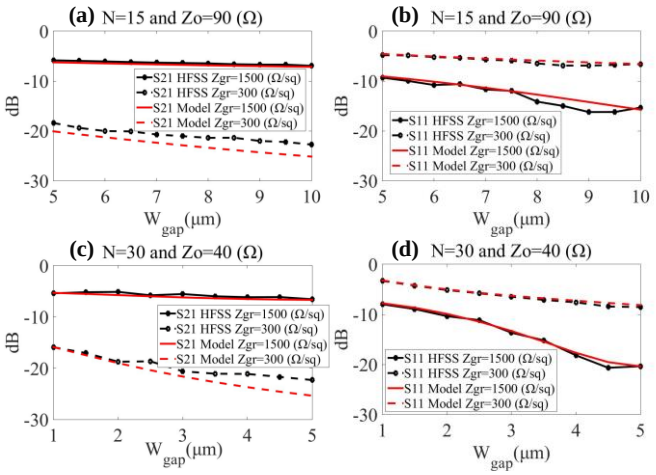

Fig. 10 The S_{21} and S_{11} comparison between the proposed shunt GL-CPW switch model and full-wave simulations for various configurations.

In the following sub-section, the case study of the shunt GL-CPW switches is presented and a comparison between the series and the shunt topology is carried out in terms of switching performance.

B. *Shunt CPW Topology*

In this section, we present the model for the shunt GL-CPW switch shown in Fig. 4c. In this design, we incorporate graphene in the gaps of the CPW line and model the switch as a distributed transmission line. Graphene is modelled as a distributed admittance of $\Delta G_{gr}=2NL/Z_{gr,sheet}$. The propagation constant and Z_0 of the GL-CPW are given by [48]

$$\gamma_{gr} = \sqrt{\left(j\omega\Delta L\right)\left(\Delta G_{gr} + j\omega\Delta C\right)}$$
$$Z_{o,gr} = \sqrt{\left(j\omega\Delta L\right)/\left(\Delta G_{gr} + j\omega\Delta C\right)} \quad (6)$$

where ΔL and ΔC are the distributed CPW components obtained by [52]. Thus, the *ABCD* parameters of the GL-CPW switch are [55]

$$ABCD = \begin{bmatrix} \boldsymbol{\cosh(\gamma L)} & \boldsymbol{Z_{o,gr}\sinh(\gamma L)} \\ \dfrac{\boldsymbol{\sinh(\gamma L)}}{\boldsymbol{Z_{o,gr}}} & \boldsymbol{\cosh(\gamma L)} \end{bmatrix} \quad (7)$$

To validate the accuracy of the proposed model, we compare the analytical model results with full-wave simulations, as shown in Fig. 10. Similarly, to the series case, we keep N and Z_0 fixed and vary W_{gap} (scaling factor) of the CPW, observing a good agreement between our model and full-wave simulations.

Following the algorithm given in Fig. 7b, the S-matrices for all the available $\{W_{gap}, N, Z_0\}$ combinations are obtained, and in Fig. 11 the 3D isosurfaces of the S_{21} are presented. Conversely, to the series case, the IL has an opposite trend with respect to N. The common region of the S_{21} is given in Fig. 11c, and is significantly larger for the shunt GL-CPW switch compared to the series topology.

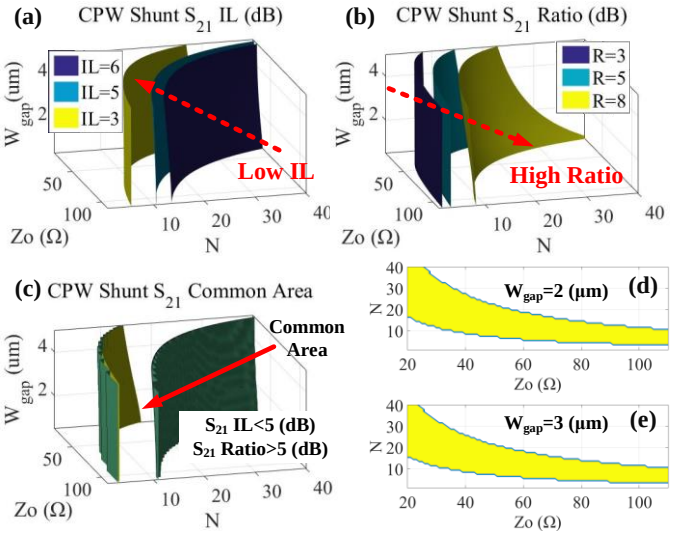

Fig. 11 The S_{21} parameters of the shunt GL-CPW switch: (a) insertion loss, (b) ON/OFF ratio, (c) common locus (volumetric) for given criteria, and (d)-(e) the slices of the common for different W_{gap} values.

In Fig. 11d-e the slices of the common areas (Fig. 11c) for different W_{gap} values are given. Contrary to the series case (Fig. 8d-e), the common area is not significantly limited by parasitics (series and shunt capacitances of Fig. 4b), hence offering greater flexibility for the design of GL switches. In addition, in Fig. 12 the S_{21} ON/OFF ratio for fixed IL values is given with respect to $\{W_{gap}, N, Z_0\}$. The results indicate that the switching performance improves with the larger scale of the devices, conversely to the series topology. Overall, the shunt topology offers better performance when considering fabrication limitations. For example, for *IL=6 dB*, the maximum achieved ratio is 19 dB for the shunt case, while for the series is less than 10 dB. Hence, using our model we establish that the shunt switch design is preferable over the series in terms of IL and ON/OFF ratio.

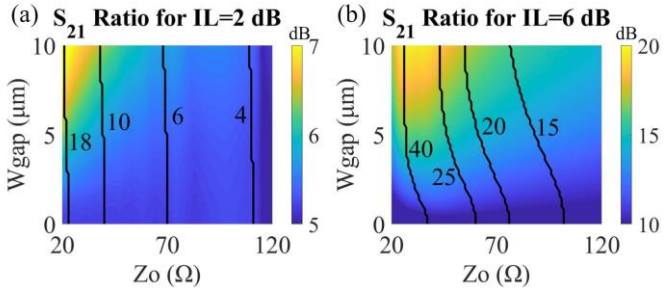

Fig. 12 The shunt GL-CPW switch 2D maps of ON/OFF ratio for fixed IL. With black contour, the number of squares is noted.

All the results of this section are obtained using the proposed equivalent model and suggest that the shunt topology outperforms the series. Nevertheless, we mention the following regarding the proposed designs: 1) The series case has better performance for smaller gap (G) sizes (<1 μm), which requires advanced/costly nanolithography processes (e.g. electron beam lithography−EBL) for fabrication. On the other hand, the performance of the shunt increases proportionally to the scaling factor, thus alleviating the cost of complex fabrication processes. However, as the CPW TL W_{gap} size increases, radiation and higher-order mode losses increase. As shown in Fig. 10, the proposed model has good agreement with the full-

wave simulations that include all these losses, but for electrically larger designs, radiation losses and higher-order modes (not accounted for herein) are expected to limit the switching performance.

IV. Graphene Loaded CPS Switches

Another type of TL that are used in planar ICs is coplanar stripline, especially for cases where a higher Z_0 is preferred (see Fig. 5). In this section, we expand the theoretical modelling proposed in Section III, for the case of series/shunt GL-CPS switches. Similarly, to the CPW topology, we characterize the switching performance based on the scaling factor, characteristic impedance, and graphene shape (squares).

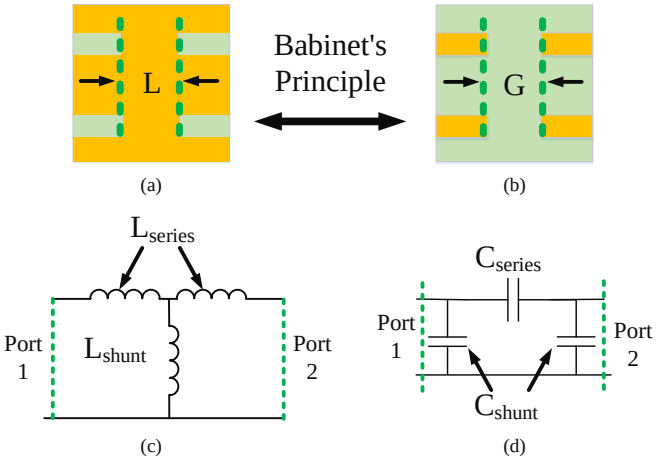

Fig. 13 (a) The CPW short discontinuity and (c) the equivalent circuit. Contrary, using Babinet's principle (b) the CPS gap discontinuity and (d) the equivalent circuit.

A. Series CPS Topology

To formulate the series GL-CPS switch, we first need to derive the equivalent circuit in the absence of graphene (parasitics), namely the series gap discontinuity. Unlike the CPW gap discontinuity, the CPS gap discontinuity's equivalent circuit models are not available in the existing literature in closed-form. Nevertheless, we can extract the equivalent models using Babinet's principle. The equivalent circuit of a shorted CPW is a T-network comprised of three inductors [50], as depicted in Fig. 13a&c. This topology is complementary to the CPS gap discontinuity (Fig. 13 b&d); hence using Babinet's principle the equivalent circuit of the CPS gap discontinuity is modelled with a Π-network comprised of three capacitors. The expressions of the parasitic capacitances are obtained by [58]

$$C_{shunt} = \frac{\varepsilon_{eff}}{(120\pi)^2} L_{series} \qquad C_{series} = \frac{\varepsilon_{eff}}{(120\pi)^2} L_{shunt} \tag{8}$$

where, $\varepsilon_{eff}=(\varepsilon_r+1)/2$, ε_r is the dielectric constant of the substrate, and L_{shunt}/L_{series} are the inductances of the CPW short discontinuity given in [50], in closed form. The graphene patches placed in the gaps of the series GL-CPS switch are modelled with a resistor ($R_{graphene}$), as shown in Fig. 14. The proposed model shows very good agreement when compared with full-wave simulations for various switch parameters, as depicted in Fig. 15.

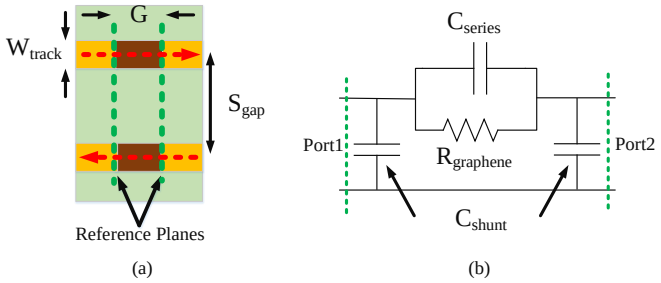

Fig. 14 (a) The series GL-CPS switch configuration (top-view) and (b) the equivalent circuit.

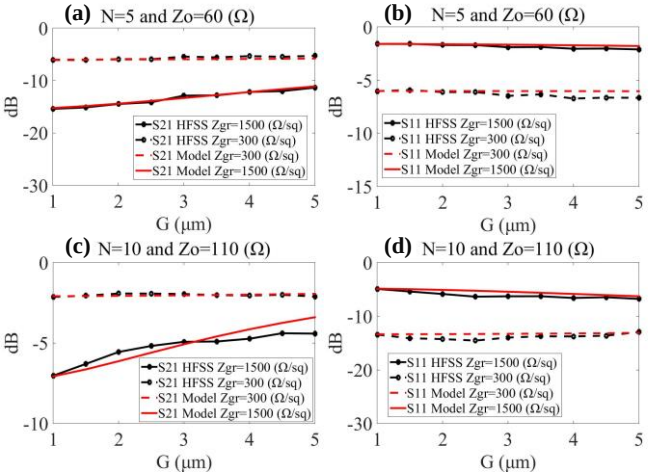

Fig. 15 The S_{21} and S_{11} comparison between the proposed series GL-CPS switch model and full-wave simulations for various configurations.

The switching performance with respect to the various parameters {G, N, Z_0} follows similar trends to the results presented for the series GL-CPW switch (see Fig. 8), thus are not included in the manuscript.

In Fig. 16, the S_{21} ON/OFF ratios are presented for two values of insertion loss. When compared to the same switch parameters of the series CPW topology (see Fig. 9), the series CPS S_{21} ratio falls off slower for larger G values and can have a potential advantage when gap minimum-dimensions are limited.

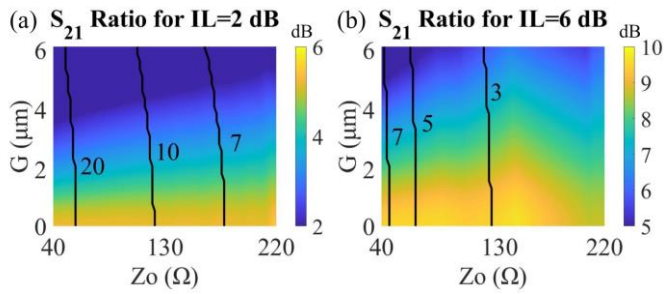

Fig. 16 The series GL-CPS switch 2D maps of ON/OFF ratio for fixed IL. With black contour, the number of squares is noted.

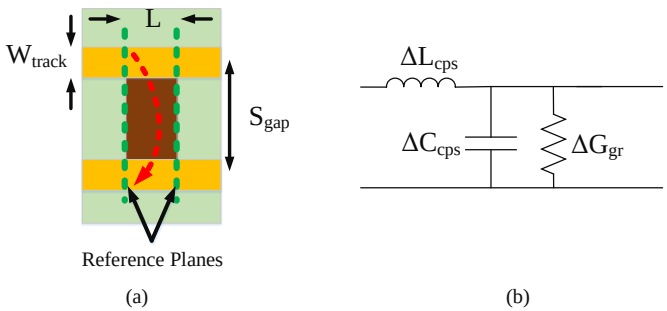

Fig. 17 (a) The shunt GL-CPS switch configuration (top-view) and (b) the equivalent circuit.

B. Shunt CPS Topology

For the shunt GL-CPS switch topology, we consider that graphene is placed in the gap between the signal and the ground traces, as is illustrated in Fig. 17a. The expressions for the distributed components are given in (6). In this case, we consider that the graphene distributed admittance is given by $\Delta G_{gr}=NL/Z_{gr,sheet}$. The *ABCD* parameters are obtained using (7). The comparison between the full-wave simulations and the proposed model are depicted in Fig. 18, where a very good agreement is observed.

Similarly, to the series case, the switching performance trends with respect to the configuration parameters $\{W_{gap}, N, Z_0\}$, are similar to the shunt CPW switch (see Fig. 11), thus are not included in the manuscript. Finally, in Fig. 19 the S_{21} ON/OFF ratios are given for various ILs. From these graphs, we observe that the shunt CPS switch has very similar performance with the respective CPW switch.

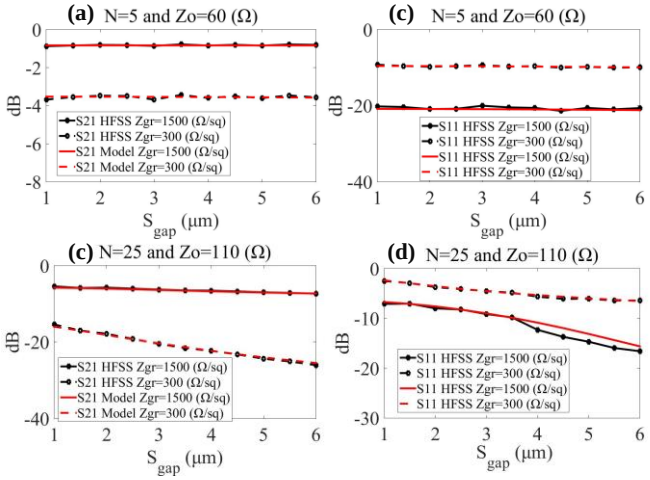

Fig. 18 The S_{21} and S_{11} comparison between the proposed shunt GL-CPS switch model and full-wave simulations for various configurations.

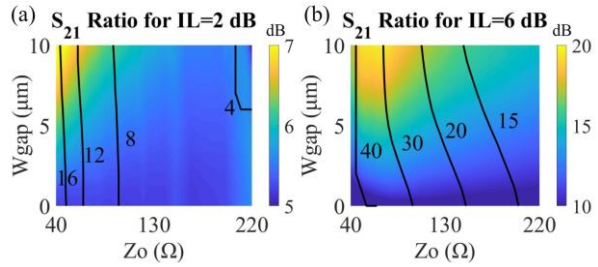

Fig. 19 The shunt GL-CPS switch 2D maps of ON/OFF ratio for fixed IL. With black contour, the number of squares is noted.

V. Discussion

The theoretical models proposed in this work are used to reveal the performance of GL switches based on coplanar waveguide topologies. The presented results reveal the trends between the different series/shunt topologies with respect to geometrical parameters. From the obtained results, we conclude that the shunt switches are dominant over the series in terms of switching performance (IL and ON/OFF ratio). However, this model can be easily adjusted to other materials and/or graphene ratios. Specifically, graphene is expected to have a sheet impedance biased/unbiased ratio between 5-10 [41]-[49]. In this work, we chose 5 based on our previous experiments in the 220-330 GHz band [44]. However, if the fabrication process is optimized, the impedance ratio will increase. In addition, instead of monolayer graphene, the thin film could be comprised of graphene flakes that exhibit a higher ratio [47]. For example, if we consider a ratio of 10 ($R_{biased}=150\ \Omega/\square$ and $R_{unbiased}=1500\ \Omega/\square$), the switching performance increases significantly both for the series and the shunt case, as shown in Fig. 20 (CPW topology). Namely, for the series GL-CPW switch, if the impedance ratio is 5, and we consider an *IL=2 dB*, $Z_0=50\ \Omega$, and $G=5\ \mu m$, the maximum switching ON/OFF ratio is 6 dB, while for an impedance ratio of 10, the respective ON/OFF switching ratio is 12 dB. To compare with existing configurations, at 275 GHz, VO_2 switches can achieve an ON/OFF ratio of 9 dB for an insertion loss of 2 dB [36].

Furthermore, in this work, the used graphene impedance values include the parasitic effects from the biasing structures (gates). Specifically, in our case study, we assume that graphene is biased with ion-gel gates, a polymer with losses of approximately less than 0.4 dB/100 μm at 300 GHz [41]-[44]. Hence, our models, account for the total performance of the graphene switches, since the parasitic gating losses are taken into consideration. One limitation of this gating approach is the switching speed that we do not analyze herein since it exceeds the scope of this work. However, according to the existing literature, the switching speed of ion-gel gated graphene can reach a few MHz [42][43]. Finally, this approach can also be used for the design of reflection-based switches. In such topologies, the performance metrics are the return loss (*RL*) and ON/OFF ratio of reflection coefficients (S_{11}), which are expected to have opposite trends to the results presented herein, though similar performance in terms of *RL* and ON/OFF ratio.

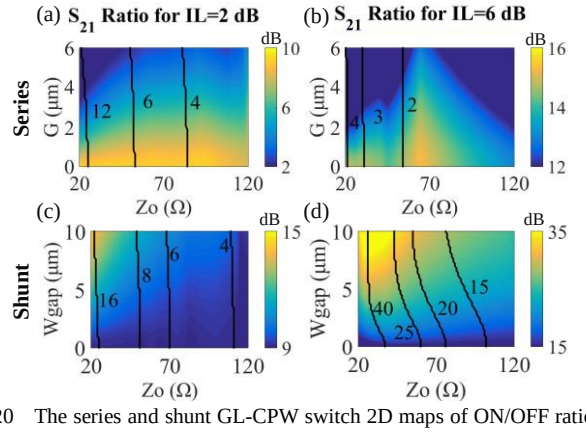

Fig. 20 The series and shunt GL-CPW switch 2D maps of ON/OFF ratio for fixed IL. These results are obtained for an impedance ratio of 10, instead of 5 as rest of the paper. The black contour indicates the number of squares (N).

VI. Conclusion

Herein, we presented an in-depth analysis of graphene loaded switches for coplanar waveguide topologies (CPW and CPS). The study is carried out using equivalent models both for the series and shunt configurations with respect to various parameters including scaling, characteristic impedance, and graphene size. We validate the results of the proposed equivalent models using a FEM solver achieving good agreement between model and full-wave simulations. Afterward, we use the proposed models to obtain the S-matrices and identify the trends between the IL and ON/OFF ratios both for series and shunt GL- CPW and CPS switches. Alongside the theoretical models of the switches, the series CPS discontinuity equivalent circuit is presented for the first time using Babinet's principle. From the acquired data, we concluded that the shunt topology outmatches the series in terms of switching performance (both IL and ON/OFF ratio), both for the CPW and CPS topologies. This study would be impossible without the use of the proposed equivalent models, since, we calculated more than 2,400,000 S-matrices for the CPW and CPS cases, a herculean task using 3D full-wave solvers. The proposed methodology can be extended for other types of transmission lines (e.g. slotlines). Furthermore, other thin-film materials that are modelled by sheet impedance/conductance (e.g. VO_2, MoS_2, BlPh etc.) can be analyzed with the proposed approach.

Acknowledgements

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