Inductor Saturation Compensation in Three-Phase Three-Wire Voltage-Source Converters via Inverse System Dynamics-II

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Abstract

Current waveform quality and current control bandwidth are the figures of merit for current controllers in three-phase threewire (3P3W) voltage-source converter (VSC) systems. When saturable inductors are employed as converter side inductors due to cost, size, and energy conversion efficiency benefits in 3P3W VSCs with conventional synchronous frame current control (CSCC); substantial drawbacks arise by means of these figures of merit. In the preceding part of this study, an inverse dynamic model based compensation (IDMBC) method has been proposed to deal with these drawbacks. Complementarily, this paper presents a thorough analytical investigation of the control system characteristics of CSCC and IDMBC methods that affect the current waveform quality and current control bandwidth. The analyses are verified via dynamic response and waveform quality simulations and experiments that employ saturable inductors reaching $1/9^{th}$ of the zero-current inductance at full current. The results obtained demonstrate the suitability of the IDMBC method for 3P3W VSCs employing saturable inductors.

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Index Terms—Bandwidth, current control, disturbance rejection, dynamic response, harmonic distortion, inductor saturation, robust control, three-phase, three-wire, voltage-source converter, waveform quality.

I. INTRODUCTION

NDUCTORS are key constituents of voltage-source converters (VSCs) by taking part as element(s) of load (grid) interface filters. In all filter topologies [1], the converter side is interfaced by inductors experiencing rectangular-shaped PWM voltage and associated current. Accordingly, the converter side inductors have a high impact on the cost, size, weight, and efficiency of the overall VSC system [2], [3]. By means of these criteria, the utilization of saturable inductors brings significant improvement [4]–[10]. The utilization of saturable inductors in three-phase three-wire (3P3W) VSC systems (shown in Fig. 1 realized as well-known two-level topology) can spread these benefits due to the wide range and volume energy conversion applications of these systems. On the other hand, such utilization in 3P3W VSC systems with industry-standard conventional synchronous frame current control (CSCC) employing PI compensators introduces unignorable current waveform quality and bandwidth shrinkage issues as reported in the preceding part of this study [7].

Probably, the current waveform quality issue is the more detrimental one introduced by the utilization of saturable inductors in 3P3W VSCs with CSCC. Besides the prohibitive effects such as additional losses, electromagnetic interference, and converter derating; certain grid codes such as IEEE 1547, VDE-AR-N 4105, and BDEW restrain the total current



Fig. 1. Three-phase three-wire two-level voltage-source converter topology.

harmonic distortion (THD_i) and individual current harmonics injected to the grid [1], [11]–[13].

The current harmonics associated with the utilization of saturable inductors in VSCs with CSCC have various sources. The first and dominant source is the mismatch between the nonlinear physical system and the linear controller [14], [15]. In the second, disturbances caused by the converter nonlinearity, imperfectly compensated dead-time, and measurement errors contribute to current harmonics not only in VSCs employing saturable inductors but also in VSCs with linear inductors [16]-[18]. The third source of the harmonics is the imperfectly decoupled cross-coupling terms [19], [20]. Such imperfect decoupling may occur in linear inductor based 3P3W VSCs with CSCC due to estimated inductance and actual inductance mismatch. Lessening such effect of the mismatch, in [21], a complex vector-based approach is presented. On the other hand, in the case of the VSC systems with saturable inductors employing CSCC, the cross-coupling decoupling matrix is indeterminate as the inductance of each phase is time-varying [7].

Current control bandwidth shrinkage due to the utilization of saturable inductors in VSCs with CSCC is the other and relatively scarcely investigated issue in the literature. Being the measure of how well an input sinusoid is tracked up to the frequency where the gain does not drop below -3 dB [22], the bandwidth is highly correlated with the dynamic response performance for linear closed-loop systems. In [21], such correlation is demonstrated for 3P3W VSCs exhibiting linear system characteristics via frequency response functions. On the other hand, for VSCs employing saturable inductors, the dynamic response can still be utilized as an indicator of the system bandwidth as a function of time; wherein [8], [23], such a utilization has already been performed and verified for single-phase VSCs with saturable inductors. In this study, a similar approach is adapted to analyze 3P3W VSC systems employing saturable inductors.

In the first part of this study [7], an inverse dynamic model based compensation (IDMBC) method is presented to overcome the waveform quality and control bandwidth shrinkage issues of the CSCC method. In accordance with the preceding part, this paper analytically investigates and compares the CSCC and IDMBC methods by means of control system characteristics that affect the waveform quality and the current control bandwidth; and verifies these characteristics and comparisons by means of simulations and experiments. For both methods, the investigation is performed through a two-phase manner representation. For the reproducibility of the results, the s-domain functions related to the analyses are given in an explicit manner.

The paper is organized as follows. In Section II, the CSCC and IDMBC methods are summarized in a two-phase manner and associated analytical convention of the methods for the progressing sections is provided. In Section III, the control system characteristics of the methods are elaborated by means of command to output, disturbance rejection, and cross-coupling decoupling. In Section IV, simulation results regarding the investigated control characteristics are provided via dynamic response, cross-coupling behaviour, and waveform quality. Similarly, in Section V, experimental results for the same system parameters that of the simulations are provided. These simulation and experimental results show the superiority of the proposed IDMBC method over the CSCC method and the viability of the IDMBC method at deep saturation levels via saturating the converter-side inductors down to 1/9th of the zero-current inductance. While the investigation and the verification are performed for the two-level 3P3W VSC topology in the paper, the method can be applied to other multilevel, multiphase VSC configurations also.

II. THE CSCC AND IDMBC METHODS

For the analyses conducted in the subsequent sections, two-phase modelling of CSCC and IDMBC current control methods are summarized in this section. In Figs. 2(a) and (b), these current control models are provided in a block diagram representation respectively.

For both of CSCC and IDMBC methods, the load is an L-R type with saturable inductors, hence is nonlinear. The disturbance signal interfered output voltage $\mathbf{v}_{\sigma} = [v_{ab} \ v_{bc}]^T$ is the control input to this load with $\mathbf{i}_{\sigma} = [i_a \ i_b]^T$ is the output current, and $\mathbf{L}_{\sigma} = \begin{bmatrix} L_a & -L_b \\ L_c & L_b + L_c \end{bmatrix}$ and $\mathbf{R}_{\sigma} = \begin{bmatrix} R_a & -R_b \\ R_c & R_b + R_c \end{bmatrix}$ are the two-phase nonlinear system inductance and resistance matrices respectively as described in [7].

Considering that an ideal 3P3W VSC is a unity gain amplifier (shown in Figs. 2(a) and (b) as 2×2 identity matrices), and assuming the disturbance decoupling is accurately performed and the estimated system parameters are identical to the actual parameters ($\hat{\mathbf{L}}_{\sigma} = \mathbf{L}_{\sigma}$, $\hat{\mathbf{R}}_{\sigma} = \mathbf{R}_{\sigma}$), the CSCC and IDMBC methods have the stationary frame dynamic equations respectively as

$$\mathbf{v}_{\sigma}^{*} = \mathbf{L}_{\sigma} \frac{d}{dt} \mathbf{i}_{\sigma} + \mathbf{R}_{\sigma} \mathbf{i}_{\sigma}$$
(1)

$$\mathbf{w}_{\sigma} = \mathbf{L}_{\mathbf{M}} \frac{d}{dt} \mathbf{i}_{\sigma} \tag{2}$$

where $\mathbf{L}_{\mathbf{M}} = \begin{bmatrix} L_{min} & 0 \\ 0 & L_{min} \end{bmatrix}$ in which L_{min} is the minimum inductance value to be able to perform designs within the maximum available current control bandwidth.

For the purpose of increasing stability, active damping techniques can be incorporated into the systems described by (1) and (2). However, such an approach has a slight effect on the relative performances of the current controllers and complicates the oncoming analyses. Similarly, the zero-sequence voltage injection ideally does not have any effect on the performance of the current controllers. Hence such injection is involved neither in the block diagram representations in Fig. 2 nor in the analyses.

The stationary frame CSCC system equation (eq. (1)) is dependent on the nonlinear (and time varying) system parameters (\mathbf{L}_{σ}), whereas that of IDMBC method (eq. (2)) is a linear one. The control inputs of (1) and (2) (\mathbf{v}_{σ}^{*} and \mathbf{w}_{σ} respectively) are both generated in synchronous frame and transformed to stationary frame. The synchronous frame to/from stationary frame transformations are performed differently for CSCC and IDMBC methods as shown in Fig. 2 via different transformation matrices $\mathbf{T}(\theta) = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \cos(\theta - 2\pi/3) & -\sin(\theta - 2\pi/3) \end{bmatrix}$ and $\mathbf{H}(\theta) = \mathbf{T}(\theta) - \mathbf{T}(\theta - 2\pi/3)$ as discussed in the preceding part of this study [7].

The error compensation is performed via PI compensators in the synchronous frame and is the same for the CSCC and IDMBC methods. The PI compensator coefficients are set to obtain predefined design bandwidth ω_{BW} for each axis by setting $K_p = \omega_{BW} L_{min}$ and $K_p = \omega_{BW} \hat{R}$ [24]. For the CSCC method, it is reasonable to employ the minimum inductance value in the setting of the K_p value to prevent time-varying system bandwidth from exceeding maximum available system bandwidth restrained by either of the carrier frequency, sampling method, measurement quality, or the processor speed. For the IDMBC method, on the other hand, as the nonlinear plant is linearized to behave as a fictitious linear inductor system with a constant inductance value of L_{min} , this minimum inductance value is employed to set K_p . Besides, other PI setting approaches such as [25], [26] can also be preferred with the consideration of bandwidth run-over.

Similar to the PI compensation, the cross-coupling decoupling is performed the same for the CSCC and IDMBC methods in the synchronous frame. The minimum inductance value is utilized in the establishment of the cross-coupling decoupling matrix as

$$\hat{\mathbf{W}}_{\mathbf{cc}} = \begin{bmatrix} 0 & -\omega L_{min} \\ \omega L_{min} & 0 \end{bmatrix}$$
(3)

where ω is the fundamental frequency. The reasoning behind the use of L_{min} for CSCC method is the fictitious linear inductor behaviour of the linearized system with an inductance of L_{min} . In the case of the CSCC method, the same crosscoupling decoupling matrix is employed to establish a fair



Fig. 2. 3P3W VSC nonlinear closed-loop current control systems in two-phase column vector block diagram representation. (a) Conventional synchronous frame current control (CSCC) method. (b) Inverse dynamic model based compensation (IDMBC) method.

comparison basis as it is indeterminate when the inductances of the three-phase current control system change with time.

III. CONTROL SYSTEM CHARACTERISTICS

In this section, the control system characteristics of the CSCC and IDMBC methods are elaborated. The investigation consists of command to output, disturbance to output, and cross-coupling characterizations.

The command to output frequency response characteristics are investigated in synchronous frame as the synchronous frame currents are dc quantities and their dynamic responses provide clear verification of the performance of the control methods as shown in the following sections via simulations and experiments. In the case of the disturbance to output frequency response investigation, the analyses are performed in the stationary frame as the physical disturbance source and the output currents are both in the stationary frame.

In the analyses, the VSC system is assumed to operate at the steady-state where the inductance variation is dominated by the fundamental frequency large-signal and small magnitude command/disturbance applied. Accordingly, the performance of the controllers is interpreted via frequency responses and a high correlation between the interpretations, simulations, and experiments is observed.



Fig. 3. Generic control block diagrams for 3P3W VSC systems for analyzing the frequency response characteristics of the current controllers. (a) The generic block diagram in synchronous frame for the investigation of command to output characteristics. (b) The generic block diagram in stationary frame for the investigation of disturbance to output characteristics.

In Fig. 3, the generic current control system block diagram representations are shown for the command to output and the disturbance to output frequency response analyses. Fig. 3(a)

represents the overall control system for the CSCC and the IDMBC methods in synchronous frame for the command to output analyses. In the figure, $\mathbf{G}_{\mathbf{P}-\mathbf{dq}}(\theta, s)$ is the physical plant transfer function matrix whereas $\mathbf{G}_{\mathbf{H}-\mathbf{dq}}(\theta, s)$ is the overall unified form of the other system blocks in the overall current regulation system in the synchronous frame. For this analysis, the disturbance signal in the synchronous frame given by (4) is set to zero.

$$\mathbf{d}_{\mathbf{dq}} = \mathbf{\hat{v}}_{\mathbf{D}-\mathbf{dq}} - \mathbf{v}_{\mathbf{D}-\mathbf{dq}} \tag{4}$$

where $\hat{\mathbf{v}}_{\mathbf{D}-\mathbf{dq}}$ and $\mathbf{v}_{\mathbf{D}-\mathbf{dq}}$ are the synchronous frame representations of the estimated and actual disturbances respectively.

The disturbance to output frequency response characteristics are investigated in the stationary frame based on Fig. 3(b). In the figure, the current command \mathbf{i}_{dq}^* is set to zero hence not shown. The stationary frame disturbance signal is taken as an input to the system wherein $\mathbf{G}_{\mathbf{P}}(\theta, s)$ is the physical plant transfer function matrix whereas $\mathbf{G}_{\mathbf{H}}(\theta, s)$ is the overall unified form of the other system blocks in the overall current regulation system in the stationary frame. The following paragraphs further clarify the obtained frequency response characteristics.

A. Command to Output Characteristics

Considering the two phase modelling in the preceding paper and Fig. 2, equation (5) represents the nonlinear physical system for CSCC and IDMBC methods as

$$\mathbf{v}_{\sigma}^{*} + \mathbf{d}_{\sigma} = \mathbf{L}_{\sigma} \frac{d}{dt} \mathbf{i}_{\sigma} + \mathbf{R}_{\sigma} \mathbf{i}_{\sigma}.$$
 (5)

where $\mathbf{d}_{\sigma} = \hat{\mathbf{v}}_{\mathbf{D}} - \mathbf{v}_{\mathbf{D}}$. While this nonlinear physical system representation is common to the CSCC and the IDMBC methods, the command voltage \mathbf{v}_{σ}^* is generated differently for each method. The representation in (5) with the stationary frame variables can be expressed in the synchronous frame for CSCC and IDMBC methods respectively as

$$\mathbf{H}(\theta)\mathbf{v}_{\mathbf{dq}} = \mathbf{L}_{\sigma}\frac{d}{dt}(\mathbf{T}(\theta)\mathbf{i}_{\mathbf{dq}}) + \mathbf{R}_{\sigma}\mathbf{T}(\theta)\mathbf{i}_{\mathbf{dq}}$$
(6)

$$\frac{\hat{\mathbf{L}}_{\sigma}}{L_{min}}\mathbf{T}(\theta)\mathbf{v}_{dq} + \frac{\hat{\mathbf{R}}_{\sigma}}{L_{min}}\int_{0}^{t}\mathbf{T}(\theta)\mathbf{v}_{dq}d\tau$$

$$= \mathbf{L}_{\sigma}\frac{d}{dt}(\mathbf{T}(\theta)\mathbf{i}_{dq}) + \mathbf{R}_{\sigma}\mathbf{T}(\theta)\mathbf{i}_{dq}$$
(7)

by setting the disturbance signal to zero for command to output frequency response characterization. The synchronous frame control voltage v_{dq} in (6) and (7) is the sum of the output of the PI compensation of the current error and the cross-coupling decoupling term which is given by

$$\mathbf{v}_{\mathbf{dq}} = K_p \{ \mathbf{i}_{\mathbf{dq}}^* - \mathbf{i}_{\mathbf{dq}} \} + K_i \int_0^t \{ \mathbf{i}_{\mathbf{dq}}^* - \mathbf{i}_{\mathbf{dq}} \} d\tau + \mathbf{\hat{W}}_{\mathbf{cc}} \mathbf{i}_{\mathbf{dq}}.$$
 (8)

Inserting (8) into (7) and (6) and expanding the derivative term one can obtain the closed-loop current control dynamics for CSCC and IDMBC methods in s-domain respectively as

$$\begin{aligned} \mathbf{H}(\theta) \big\{ \mathbf{K}_{\mathbf{c}}(s) \{ \mathbf{i}_{\mathbf{dq}}^{*}(s) - \mathbf{i}_{\mathbf{dq}}(s) \} + \hat{\mathbf{W}}_{\mathbf{cc}} \mathbf{i}_{\mathbf{dq}}(s) \big\} \\ &= \big\{ \mathbf{L}_{\sigma} \mathbf{X}(\theta, s) + \mathbf{R}_{\sigma} \mathbf{T}(\theta) \big\} \mathbf{i}_{\mathbf{dq}}(s) \end{aligned} \tag{9}$$

$$\left\{\frac{\hat{\mathbf{L}}_{\sigma}}{L_{min}}\mathbf{X}(\theta,s) + \frac{\hat{\mathbf{R}}_{\sigma}}{L_{min}}\mathbf{T}(\theta)\right\}\left\{\mathbf{K}_{\mathbf{c}}(s)\left\{\mathbf{i}_{\mathbf{dq}}^{*}(s) - \mathbf{i}_{\mathbf{dq}}(s)\right\} + \hat{\mathbf{W}}_{\mathbf{cc}}\mathbf{i}_{\mathbf{dq}}(s)\right\} = \left\{\mathbf{L}_{\sigma}\mathbf{Y}(\theta,s) + \mathbf{R}_{\sigma}\mathbf{X}(\theta,s)\right\}\mathbf{i}_{\mathbf{dq}}(s)$$
(10)

where $\mathbf{K}_{\mathbf{c}}(s) = \begin{bmatrix} K_p + K_i/s & 0 \\ 0 & K_p + K_i/s \end{bmatrix}$ is the s-domain representation of PI compensator. Further, $\mathbf{X}(\theta, s) = \omega \mathbf{P}(\theta) + s\mathbf{T}(\theta)$ and $\mathbf{Y}(\theta, s) = -\omega^2 \mathbf{T}(\theta) + 2\omega s \mathbf{P}(\theta) + s^2 \mathbf{T}(\theta)$ are the s-domain representations of first order and second order time derivatives of the operator $\mathbf{T}(\theta)(\cdot)$ respectively in which $\mathbf{P}(\theta) = \mathbf{T}(\theta + \pi/2)$. The closed-loop current control dynamics of (9) and (10) can be rearranged in the form given by

$$\mathbf{i}_{\mathbf{dq}}(s) = \mathbf{G}_{\mathbf{OL}-\mathbf{dq}}(\theta, s) \{ \mathbf{i}_{\mathbf{dq}}^*(s) - \mathbf{i}_{\mathbf{dq}}(s) \}$$
(11)

where $\mathbf{G}_{\mathbf{OL}-\mathbf{dq}}(\theta, s)$, error to output synchronous frame open-loop transfer function matrix, corresponds to the multiplication of $\mathbf{G}_{\mathbf{H}-\mathbf{dq}}(\theta, s)\mathbf{G}_{\mathbf{P}-\mathbf{dq}}(\theta, s)$ shown in Fig. 3. These matrices for CSCC and IDMBC methods are obtained as

$$\mathbf{G_{OL-dq}^{CSCC}}(\theta, s) = \left\{ \mathbf{L}_{\sigma} \mathbf{X}(\theta, s) + \mathbf{R}_{\sigma} \mathbf{T}(\theta) - \mathbf{H}(\theta) \mathbf{\hat{W}_{cc}} \right\}^{-1} \mathbf{H}(\theta) \mathbf{K}_{c}(s)$$
(12)

$$\mathbf{G_{OL-dq}^{IDMBC}}(\theta, s) = \left\{ \mathbf{L}_{\sigma} \mathbf{Y}(\theta, s) + \mathbf{R}_{\sigma} \mathbf{X}(\theta, s) - \left\{ \frac{\hat{\mathbf{L}}_{\sigma}}{L_{min}} \mathbf{X}(\theta, s) + \frac{\hat{\mathbf{R}}_{\sigma}}{L_{min}} \mathbf{T}(\theta) \right\} \hat{\mathbf{W}}_{cc} \right\}^{-1} \quad (13)$$
$$\times \left\{ \frac{\hat{\mathbf{L}}_{\sigma}}{L_{min}} \mathbf{X}(\theta, s) + \frac{\hat{\mathbf{R}}_{\sigma}}{L_{min}} \mathbf{T}(\theta) \right\} \mathbf{K}_{c}(s).$$

The frequency response characteristics of CSCC given in (12) describe spatially varying (θ dependent) behaviour in which the variation frequency is assumed to be much smaller than the investigated system dynamics ($\omega \ll \omega_{BW}$). On the other hand, the frequency response characteristics of IDMBC method in (13) are spatially invariant as intended [7] when the estimated system parameters are identical to the actual

system parameters ($\hat{\mathbf{L}}_{\sigma} = \mathbf{L}_{\sigma}, \, \hat{\mathbf{R}}_{\sigma} = \mathbf{R}_{\sigma}$). When the system is linear (the inductance is constant), the command to output characteristics of CSCC and IDMBC methods also become the same and spatially invariant. Accordingly in Fig. 4, the d-axis to d-axis and q-axis to q-axis magnitude and phase characteristics of CSCC and IDMBC methods are illustrated for a linear symmetrical 3P3W L-R current control system with $L = 500 \ \mu\text{H}$, $R = 0.5 \ \Omega$, and $K_p = 1.57$, $K_i = 1570$ to yield $\omega_{BW} = 2\pi 500$ rad/s [24]. As shown in Fig. 4(a) and (b), the d- and q-axis system bandwidths of CSCC and IDMBC methods are the same as the preset design bandwidth ω_{BW} , regardless of the phase angle. Similarly, the phase characteristics of the d-axis to d-axis and q-axis to q-axis open-loop frequency responses of the two methods are the same and constant (-90°) yielding a phase margin (PM) of 90°. The magnitude and phase characteristics of the d- and q-axis show two decoupled single-phase linear L-R control system behaviour as intended.



Fig. 4. d-axis to d-axis and q-axis to q-axis open loop magnitude and phase characteristics of the frequency responses of CSCC and IDMBC methods for symmetrical 3P3W linear VSC system. (a) d-axis to d-axis magnitude response. (b) q-axis to q-axis magnitude response. (c) d-axis to d-axis phase response. (d) q-axis to q-axis phase response. These plots are θ independent due to linear and symmetrical operation. For the IDMBC method with nonlinear inductors, the characteristics are the same as if the system is a linear one due to linearization in the large [7].

In Fig. 5, the case for a nonlinear inductor is elaborated for the CSCC method. In the case, the inductance of each phase decreases from 0.45 mH to 500 μ H with zero to full load current (10 A) having an ESR of 0.5 Ω . The K_p and K_i values are selected the same as the linear case ($K_p = 1.57$, $K_i = 1570$) to yield $\omega_{BW} = 2\pi500$ rad/s. It should be noted that the K_p value is calculated in proportion to the minimum inductance L_{min} to avoid bandwidth run-over. Considering the d-axis to d-axis and q-axis to q-axis magnitude plots in Fig. 5 (a) and (b) for $\theta = 0$ and $\theta = \pi/3$ under fullload operation, the d-axis bandwidth (ω_{BW-dd}) and q-axis bandwidth (ω_{BW-qq}) are observed to be much smaller than the design bandwidth ω_{BW} which is called bandwidth shrinkage [8], [23] and elaborated in [7]. Moreover, the phase responses in Fig. 5(c) and (d) show the PM of d- and q-axis decrease



Fig. 5. d-axis to d-axis and q-axis to q-axis open loop magnitude and phase characteristics of the frequency responses of CSCC method for nonlinear inductor case. (a) d-axis to d-axis magnitude response. (b) q-axis to q-axis magnitude response. (c) d-axis to d-axis phase response. (d) q-axis to q-axis phase response. The characteristics of the IDMBC method for the nonlinear inductor case are given in Fig. 4.

down to 62 degrees decreasing the robustness of the stability of the closed-loop current control system [22].

In the case of the IDMBC method with nonlinear inductors, the magnitude and phase responses are obtained as the same shown in Fig. 4 due to the linearization of the nonlinear plant in the large via inverse system dynamics.

B. Disturbance Rejection Characteristics

In 3P3W VSCs, the disturbance voltage is mainly composed of the load voltage (or grid voltage) and the VSC generated disturbance voltage which can be described in two-phase representation by

$$\mathbf{v}_{\mathbf{D}} = \mathbf{v}_{\mathbf{g}-\sigma} + \mathbf{v}_{\mathbf{id}-\sigma} \tag{14}$$

where $\mathbf{v}_{\mathbf{g}-\sigma}$ is load voltage and $\mathbf{v}_{\mathbf{id}-\sigma}$ is inverter generated disturbance due to dead-time, measurement errors, and switch nonidealities [27]. In (14), the two-phase load voltage can described as $\mathbf{v}_{\mathbf{g}-\sigma} = [(v_{an} - v_{bn}) (v_{bn} - v_{cn})]^T$ in terms of the phase to neutral point load voltages as shown in Fig. 1. The inverter generated component of $\mathbf{v}_{\mathbf{D}}$ can be expressed in a similar manner as $\mathbf{v}_{\mathbf{id}-\sigma} = [(v_{id-a} - v_{id-b}) (v_{id-b} - v_{id-c})]^T$ wherein v_{id-a}, v_{id-b} , and v_{id-c} denote the inverter generated disturbance voltage of leg A, B, and C respectively. The same convention applies for the estimated disturbance voltage $\hat{\mathbf{v}}_{\mathbf{D}}$.

To decouple the distorting effects of the disturbance voltage, it is conventionally performed that the estimated disturbance voltage is added to the control system as shown in Fig. 2. However, perfect decoupling can not be achieved due to measurement and estimation errors. Due to this imperfect decoupling, depending on the measurement quality and estimation success, more or less disturbance voltage interferes to the dynamic system as described by (5) so that the current control systems in Fig. 2 can be interpreted as shown in Fig. 3(b) in the stationary frame with the current command set to zero $(i_{dq}^* = 0)$. With such a setting for disturbance rejection characterization, the current control methods the stationary frame represented the dynamic system in (5) can be described in s-domain as

$$\mathbf{i}_{\sigma}(s) = \mathbf{F}_{\mathbf{D}}(\theta, s) \mathbf{d}_{\sigma}(s) \tag{15}$$

where $\mathbf{F}_{\mathbf{D}}(\theta, s)$ stands for the disturbance to output transfer function. Considering Fig. 2 and expanding the command voltage \mathbf{v}_{σ}^* in (5) according to the control architectures, the disturbance to output transfer functions for CSCC and IDMBC methods can be obtained respectively as

$$\mathbf{F}_{\mathbf{D}}^{\mathbf{CSCC}}(\theta, s) = \left\{ s\mathbf{L}_{\sigma} + \mathbf{R}_{\sigma} - \mathbf{H}(\theta) \{ \hat{\mathbf{W}}_{\mathbf{cc}} - \mathbf{K}_{\mathbf{c}}(s) \} \mathbf{T}(\theta)^{-1} \right\}^{-1}$$
(16)

$$\mathbf{F}_{\mathbf{D}}^{\mathbf{IDMBC}}(\theta, s) = \left\{ (s\mathbf{L}_{\sigma} + \mathbf{R}_{\sigma}) - \left\{ \frac{\mathbf{\hat{L}}_{\sigma}}{L_{min}} + \frac{\mathbf{\hat{R}}_{\sigma}}{sL_{min}} \right\} \right\} (17) \times \mathbf{T}(\theta) \left\{ \mathbf{\hat{W}_{cc}} - \mathbf{K_{c}}(s) \right\} \mathbf{T}(\theta)^{-1} \right\}^{-1}.$$



Fig. 6. Disturbance to output transfer function magnitude plots of the CSCC and IDMBC methods for nonlinear inductor case at two different angles. (a) d_{ab} to i_a magnitude response. (b) d_{bc} to i_a magnitude response. (c) d_{ab} to i_b magnitude response. (d) d_{bc} to i_b magnitude response.

The magnitude plots of the disturbance to output transfer functions of CSCC and IDMBC methods for two different angles ($\theta = 0$ and $\theta = \pi/2$) in Fig. 6 indicate distinctive behaviours of the current control methods. In the figure the terms d_{ab} and d_{bc} represent the elements of the disturbance vector $(\mathbf{d}_{\sigma}(s) = [d_{ab}(s) d_{bc}(s)]^T)$. In the figure, the same nonlinear current control system parameters given in the previous subsection are employed to yield the disturbance to output magnitude responses. The obtained magnitude responses in Fig. 6(a)-(d) show that the IDMBC method has better disturbance rejection characteristics than CSCC method especially for low-frequency disturbance signals even for different angles. The difference of the rejection of low-frequency disturbance signals between the methods can be as much as 60 dB while the disturbance rejection characteristics of two methods converge as the frequency of the disturbance increase. Such characteristics of the IDMBC method yield improved current waveform quality due to the reduction of the disturbance effects on the converter current.

C. Cross-Coupling Characteristics

The cross-coupling decoupling performance of the CSCC method in the preceding part of this study [7] has been found deficient as the correspondence $\mathbf{H}(\theta)\hat{\mathbf{W}}_{cc} = \omega \mathbf{L}_{\sigma} \mathbf{P}(\theta)$ is not met when saturable inductors are employed. On the other hand in the IDMBC method, due linearization of the nonlinear system in the large, the system behaves as a constant inductance current control system with unity-gain zero-phase characteristics described by (2). Considering this outcome and Fig. 2(b), the equivalence

$$\mathbf{T}(\theta)\hat{\mathbf{W}}_{\mathbf{cc}} = \omega \mathbf{L}_{\mathbf{M}} \mathbf{P}(\theta) \tag{18}$$

holds for $\hat{\mathbf{L}}_{\sigma} = \mathbf{L}_{\sigma}$. Therefore, contrary to the CSCC method, it is reasonable to expect no cross-coupling problem for the IDMBC method.

IV. SIMULATION RESULTS

In this section, the proposed IDMBC method for 3P3W VSC system simulation results are presented in comparison with that of the CSCC method. The current regulator attributes are investigated by means of dynamic response, cross-coupling behaviour, and steady-state waveform quality. Accordingly, the simulated system configuration by means of hardware and control is provided.

A. Simulated System Configuration

1) Simulated System Hardware: Simulation studies are conducted for the 3P3W VSC setup to prove the viability of the proposed IDMBC control method in comparison with the CSCC method. Two hardware configurations are employed as shown in Fig. 7 for the investigation of the performance of the current controllers. For the dynamic response and crosscoupling behaviour investigation, the VSC+inductor terminals short-circuited configuration shown in Fig. 7(a) is employed to render the sole characteristics without grid voltage interference. On the other hand, the waveform quality is investigated via grid-connected configuration shown in Fig. 7(b).

In Fig. 7(c), the L-i characteristics of saturable inductors employed as converter side inductors are illustrated. These characteristics are obtained from experimental measurements as performed in [8] and used for analyses, simulations, and the implementation of experimental inverse system dynamics. The selected core is deeply saturated so that the inductance is decreased with the increase in the current down to $1/9^{th}$ of the initial value. Such deep saturation levels can be tolerated in 3P3W VSC systems by means of PWM ripple due to balancing effect of the inductors as the phase currents are driven by the VSC line-to-line voltages and the minimum inductance values of any two phases do not overlap in time.

In the grid-connected configuration shown in Fig. 7(b), the filter capacitor is selected to be 2.2 μ F connected in a wye configuration. The grid side inductor is selected to be 2 mH. The LCL filter provides sufficient PWM harmonic attenuation even for the minimum inductance value of the converter side inductor within the design constraints provided [28]. The parameters related to the simulated hardware configuration in this figure is tabulated in Table-I. These parameters are also the same for experimental configuration.



Fig. 7. Equivalent experimental configurations. (a) VSC+inductor terminals short-circuited configuration. (b) Grid-connected configuration. (c) L-i characteristics of the converter side inductors employed throughout the study.

TABLE I SIMULATED AND EXPERIMENTAL PARAMETERS FOR 3P3W VSC SYSTEM

Parameter	Value
dc-link voltage (V _{dc})	350 V
Rated current	10 A _{peak} /phase
Grid voltage	115 V _{RMS} /phase
Fundamental frequency ω	$2\pi 50$ rad/s
Carrier frequency f_c	10 kHz
Modulation method	SVPWM
Sampling period (T_s)	50 µs
Inverter dead-time	3 µs
L_{max}/L_{min} (converter side)	4.45/0.5 mH
L_g (grid side)	2 mH
R (converter side equivalent resistance/phase)	0.5 Ω
C_f (LCL filter capacitor)	2.2 μF (2.2 %)

2) Simulated System Control: The 3P3W VSC system simulations are performed both for CSCC and IDMBC methods with a sufficiently small step size of $0.02 \ \mu s$ for the simulation of nonlinear systems involving saturable inductors having the characteristics of Fig. 7(c). The synchronous frame PI controllers (for the d- and q-axis) in Fig. 2 are tuned to provide a bandwidth of $2\pi 500$ rad/s as if the system is a linear one (having constant converter side inductance of L_{min}) and accordingly the PI gains are tuned as $K_p = \omega_{BW} L_{min}$ and $K_i = \omega_{BW} \hat{R}$ for both methods. The cross-coupling decoupling is performed as the same for both controllers by using L_{min} to form the cross-coupling decoupling matrix \hat{W}_{cc} . Space vector PWM (SVPWM) method is employed to efficiently utilize the dc-link voltage and to have reduced ripple current. Moreover, such utilization of SVPWM method proves the compatibility of zero-sequence voltage injection in 3P3W VSC systems with nonlinear inductors. The zero-sequence signal of SVPWM is generated by selecting the minimum voltage command magnitude of the three phases, multiplying by 0.5 and adding to each of the three-phase voltage command [29]. Simulation results are obtained as the compensator gains are kept the same for each configuration, current control method, and test. With these specifications, dynamic response, cross-coupling behaviour, and waveform quality performances of the current control methods are investigated.

B. Dynamic Response

The dynamic response characteristics of a current regulator are one of the figures of merit to evaluate and compare the controller performances. Further, the dynamic response performance is a direct indicator of the system bandwidth at the operating condition of the converter [8]. The faster the response implies the higher the control bandwidth.



Fig. 8. Simulated d-axis step responses of the CSCC and IDMBC methods at various d-axis dc-bias currents. Note that q-axis current command is set to zero.

To examine the dynamic response characteristics of the current controllers, simulations are performed by providing 1 A step changes on the d-axis current command whereas the q-axis current command is set to zero. In Fig. 8, the d-axis current command and currents are illustrated for CSCC and IDMBC methods. As the q-axis currents are set to zero they are not illustrated in the figure. For the CSCC method, the response (or rise) time to a 1 A step increase is highly dependent on the current bias as discussed in the preceding part of this study [7]. When the current dc-bias is zero, the rise

time is approximately 3-4 ms whereas when the d-axis current dc-bias level is 10 A, the rise time of the CSCC method is around 1 ms. This bandwidth shrinkage phenomenon in 3P3W VSCs with CSCC is similar to the case that of single-phase controlled VSCs under dc excitation [8], [23].

On the other hand, the response time of the IDMBC method is the same for all current bias levels (1 ms) exhibiting that the bandwidth is conserved throughout various operating conditions of the VSC.

C. Cross-Coupling Behaviour

In addition to the dynamic response performance, it is desired for a 3P3W VSC current control system to have independent control of the d- and q-axis currents without any coupling effects on each other. To examine the cross-coupling behaviour of the current controllers, simulations have been performed. Briefly, the current command value for one axis is changed instantly while the actual current of the other axis is observed.



Fig. 9. Experimental d-axis (or q-axis) step responses of the CSCC and IDMBC methods at various d- and q-axis dc-bias currents. (a) $i_d^* = 1 \text{ A} \rightarrow 2 \text{ A} \rightarrow 1 \text{ A}$ while $i_q^* = 0 \text{ A}$. (b) $i_q^* = 1 \text{ A} \rightarrow 2 \text{ A} \rightarrow 1 \text{ A}$ while $i_d^* = 0 \text{ A}$. (c) $i_d^* = 4 \text{ A} \rightarrow 5 \text{ A} \rightarrow 4 \text{ A}$ while $i_q^* = 4 \text{ A}$. (d) $i_q^* = 4 \text{ A} \rightarrow 5 \text{ A} \rightarrow 4 \text{ A}$ while $i_d^* = 4 \text{ A}$.

In Fig. 9, the waveforms regarding the observations are illustrated. For the CSCC method, when the d-axis or q-axis is excited, the current of the other axis responds to the change which is undesirable for a current controller. On the other hand, in the case of the IDMBC method, the two axes seem decoupled from each other almost perfectly as when one axis current is changed the other axis current does not exhibit any considerable change as a desirable feature for a highperformance current controller.

D. Waveform Quality

The waveform quality performances of the CSCC and IDMBC methods are investigated at steady-state by means of simulations in a grid-connected mode shown in Fig. 7(b).

In Figs. 10(a) and (b), the converter side current, voltage command signal, zero-sequence signal, and zero-sequence added voltage command signal (the signal provided to triangle comparator) of phase-A of the CSCC and IDMBC methods are illustrated respectively. With the application of the IDMBC method, the converter side current waveform seems to be improved when compared to the converter side current waveform of the CSCC method even if these waveforms contain PWM current ripple. In Figs. 10(c) and (d), such a conclusion can be reached through the grid currents. As filtered by the LCL filter, almost all PWM caused high-frequency current harmonics are cleared and there remained control-fixable loworder harmonics in the grid current especially in the CSCC method. When the current control technique is changed to the IDMBC, one can observe the current waveform quality improvement with the employment of the IDMBC method. To quantify, the THD_i is reduced from 5.45 % to 1.82 %. Fig. 10(c) and (d) also show that at full load current, the inductance of the converter side inductor decreases almost to $1/9^{th}$ of its zero current value as expected.



Fig. 10. Simulated steady-state converter side current, voltage command signal, zero-sequence signal, and zero-sequence added voltage command signal of phase-a: (a) CSCC method. (b) IDMBC method. The converter side inductance and the grid-current: (c) CSCC method. (d) IDMBC method.



Fig. 11. Simulated harmonic spectra of the phase currents of the CSCC and IDMBC methods around low frequency region.

In Fig. 11, the harmonic spectra of the CSCC and IDMBC methods around the low-frequency region are illustrated.

Based on the spectra, the most dominant harmonics are observed to be 5^{th} and 7^{th} for both methods. When compared the two methods, the same conclusion obtained from the timedomain waveforms can be reached that the IDMBC method outperforms the CSCC method by means of current waveform quality.

V. EXPERIMENTAL RESULTS

In order to observe and compare the dynamic response, cross-coupling behaviour, and steady-state performances of CSCC and IDMBC methods, experiments are conducted. Accordingly, the experimental system configuration by means of hardware and control implementation is provided.

A. Experimental System Configuration

1) Experimental System Hardware: In the hardware implementation for the performance investigation of the current control methods, VSC+inductor terminals short-circuited and grid-connected configurations shown in Fig. 7 are employed as in the case of simulation studies. The power module PM75RL1A120 is utilized in the realization of the VSC power semiconductors. The dynamic response and crosscoupling performances of the methods are investigated via VSC+inductor terminals short-circuited configuration to eliminate the grid interaction. On the other hand, the waveform quality performances of the methods are investigated via gridconnected experiments. The experimental system parameters kept the same as that are tabulated in Table-I. For both configurations in Fig. 7, the dc-link voltage is obtained from the grid via a diode rectifier and a variac. In the grid-connected experiments, the ac-grid voltage is stepped down to 115 V_{RMS}/phase via three single-phase transformers connected in a wye-wye configuration each having a leakage inductance of 0.25 mH. Supplemental linear filter inductors as grid side have been inserted also to form grid side inductors $(L_{g-a}, L_{g-b}, L_{g-c})$ together with the transformer leakage inductance. The converter side saturable inductors are wound to sendust powder material toroid cores [30] yielding the inductance characteristics given in Fig. 7(c). Fig. 12 shows this three-phase grid-connected VSC system hardware.

2) Control Implementation: The control schemes in Fig. 2 are implemented for experimental validation of and performance comparison of the controllers. A 150 MHz floating-point digital signal processor (DSP) is used to realize the control functions in discrete time. The interrupt cycle is selected as 50 μ s to yield a double update for a PWM cycle of 100 μ s (10 kHz). At every interrupt cycle, the controller executes the grid synchronization via a three-phase vector PLL method [31], current control algorithms including anti-windup, software VSC protection, and PWM signal generation. A dead-time of 3 μ s is utilized and its compensation is performed. The backward Euler method is utilized for the discretization of the continuous-time controllers.

All system control parameters are selected the same as in the case of simulations. The L-i characteristics of the converter side inductors are modelled as second-order polynomials to establish an inverse dynamic model of the current-control



Fig. 12. Three-phase three-wire grid-connected VSC setup.

system as in [8]. As the converter side currents are double sampled [24], the d- and q-axis currents obtained via the DSP readings are almost PWM ripple-free.

B. Dynamic Response

In order to observe and compare the dynamic response performances of the CSCC and IDMBC methods, 1 A step changes are applied to the d-axis current reference for both methods, as in the case of simulations. To mitigate the grid voltage disturbance, the test is carried out for the VSC+inductor terminals are short-circuited configuration. The associated dynamic response waveforms are illustrated in Fig. 13. The results presented in this figure are very similar to the one obtained in the simulations (Fig. 8). When the d-axis current is zero, the rise time of the d-axis current is quite long in the CSCC method when compared that of the IDMBC method even if the associated PI controller parameters are the same aiming the same bandwidth. When the d-axis current offset is increased, the rise time of the CSCC method starts to decrease while the dynamic response characteristics of the IDMBC method are the same which is initially designed to be. This is due to the bandwidth shrinkage phenomenon in the CSCC method as described in the preceding part of this study [7].

C. Cross-Coupling Behaviour

The experimental cross-coupling behaviour of the CSCC and IDMBC methods are investigated by applying a step



Fig. 13. Experimental d-axis step responses of the CSCC and IDMBC methods at various d-axis dc-bias currents. Note that q-axis current is set to zero.



Fig. 14. Experimental d-axis (or q-axis) step responses of the CSCC and IDMBC methods at various d- and q-axis dc-bias currents. (a) $i_d^* = 1 \text{ A} \rightarrow 2 \text{ A} \rightarrow 1 \text{ A}$ while $i_q^* = 0 \text{ A}$. (b) $i_q^* = 1 \text{ A} \rightarrow 2 \text{ A} \rightarrow 1 \text{ A}$ while $i_d^* = 0 \text{ A}$. (c) $i_d^* = 4 \text{ A} \rightarrow 5 \text{ A} \rightarrow 4 \text{ A}$ while $i_q^* = 4 \text{ A}$. (d) $i_q^* = 4 \text{ A} \rightarrow 5 \text{ A} \rightarrow 4 \text{ A}$ while $i_d^* = 4 \text{ A}$.

change to the current command of an axis and then observing the actual current of the other axis, as in the case of simulations. In Fig. 14(a), the d-axis current command is increased from 1 A to 2 A while the q-axis command is kept at 0 A. In the figure, for the CSCC method, the q-axis current is not stationary but it deviates from its reference value with the change in the d-axis current indicating the imperfect crosscoupling decoupling. When the d- and q-axis currents are interchanged (Fig. 14(b)), the same phenomenon again appears in a similar way but distinct in sign with a reasoning that the cross-coupling terms have opposite signs. On the other hand, for both Figs. 14(a) and (b), the IDMBC method exhibits superior cross-coupling decoupling performance as expected from analyses and simulations.



Fig. 15. Experimental grid-connected 3P3W VSC waveforms for the CSCC and IDMBC methods at full load, zero displacement angle $(i_d^* = 10 \text{ A}, i_q^* = 0 \text{ A})$, and steady-state. (a) SVPWM output voltage command and converter side current for CSCC method. (b) SVPWM output voltage command and converter side current for IDMBC method. (c) Output filter capacitor voltage and grid current for IDMBC method. (d) Output filter capacitor voltage and grid current for IDMBC method.

In Figs. 14(c) and (d), the dc-bias levels on both axes are set to 4 A. Then the d- and q-axis current commands are increased to and decreased from 5 A (shown in Figs. 14(c) and (d) respectively). In these cases, even the 6^{th} order harmonic blurs the decoupling effect it can be still identified that the decoupling is imperfect when the rising and falling regions of the current waveforms are considered. Similar to the cases of Figs. 14(a) and (b), the cases of Figs. 14(c) and (d) illustrate the superior cross-coupling decoupling performance of the IDMBC method.

D. Waveform Quality

The experimental waveform quality investigation of CSCC and IDMBC current control methods is performed via the grid-connected configuration shown in Fig. 7(b). The system parameters specified in Table-I are utilized in the experiments. The inductor L-i characteristics are the same in Fig. 7(c) and the controller parameters are kept as the same that are used for simulations.

In Fig. 15, the grid-connected 3P3W VSC system significant waveforms are illustrated at full load, zero displacement angle, and steady-state conditions. In Figs. 15(a) and (b), the VSC output voltage (with SVPWM), and converter side phase-a inductor currents are depicted for CSCC and IDMBC methods respectively. In Figs. 15(c) and (d), the capacitor voltage and the grid current are shown in the same order. The grid current waveforms indicate the effectiveness of the IDMBC method, while it can be inferred that the CSCC method can not be used in grid-connected applications for the current system parameters as 5 % THD_i limit is exceeded that is set by the grid connection standards such as IEEE 519.

In Fig. 16 the three-phase grid currents of the methods are illustrated for three grid cycles. The THD_i value for the CSCC method is measured to be 9.6 % and the THD_i value of the IDMBC method is measured to be 2.58 %. The measured



Fig. 16. Experimental grid currents of the CSCC and IDMBC methods at full load for zero displacement angle $(i_d^* = 10 \text{ A}, i_q^* = 0 \text{ A})$. (a) Grid currents of the three phases for CSCC method. (b) Grid currents of the three phases for IDMBC method.

THD_i values in the grid-connected configuration are slightly greater than their simulated counterparts.

In Fig. 17, the harmonic spectra belonging to the grid currents shown in Fig. 15 (and grid currents also shown in Fig. 16) are illustrated. In the spectra, the zero-sequence current harmonics are minimal as there is no return path for these harmonics to flow. For CSCC method, the 5^{th} and the 7^{th} harmonics flow in a considerable amount making the CSCC method prohibitive for grid-connected applications with the current parameters. As discussed, such spectrum can be attributed to imperfect cross-coupling decoupling, measurement errors and delays, low disturbance rejection characteristics, and load nonlinearity. In the case of IDMBC method, the spectrum has acceptably low 5^{th} and 7^{th} harmonic current magnitudes demonstrating the suitability of the method for grid-connected applications.



Fig. 17. Experimental grid-connected system grid side current low frequency region harmonic spectra for the CSCC and IDMBC methods.

VI. CONCLUSION

This paper presented detailed analyses of the control system characteristics of conventional synchronous frame current control (CSCC) and inverse dynamic model based compensation (IDMBC) methods for three-phase three-wire (3P3W) voltage-source converter (VSC) systems employing saturable inductors. The current control methods are evaluated by taking the current waveform quality and current control bandwidth as the performance criteria. Constituting the determinants for these criteria; command to output, disturbance to output, and cross-coupling decoupling characteristics of the methods are investigated on a two-phase representation basis. Simulations and experiments are conducted as well for a 3P3W VSC system employing saturable inductors reaching $1/9^{th}$ of the zero-current inductance at full current to verify the analyses and performance comparisons. It is shown via analyses, simulations, and experiments that the CSCC method suffers both the current waveform quality and current control bandwidth. On the other hand, the IDMBC method exhibits superior performance with uniform current control bandwidth and high steady-state current waveform quality that meets grid codes enabling the utilization of deeply saturable inductors in 3P3W VSC systems.

REFERENCES

- R. N. Beres, X. Wang, M. Liserre, F. Blaabjerg, and C. L. Bak, "A review of passive power filters for three-phase grid-connected voltagesource converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, pp. 54–69, March 2016.
- [2] J. Muhlethaler, M. Schweizer, R. Blattmann, J. W. Kolar, and A. Ecklebe, "Optimal design of LCL harmonic filters for three-phase pfc rectifiers," *IEEE Transactions on Power Electronics*, vol. 28, no. 7, pp. 3114–3125, 2013.
- [3] Y. Jiao and F. C. Lee, "Lcl filter design and inductor ripple analysis for 3-level npc grid interface converter," in 2014 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 1911–1918, 2014.
- [4] Q. Li, D. Jiang, and Y. Zhang, "Analysis and calculation of current ripple considering inductance saturation and its application to variable switching frequency pwm," *IEEE Transactions on Power Electronics*, vol. 34, no. 12, pp. 12262–12273, 2019.
- [5] N. Femia, K. Stoyka, and G. Di Capua, "Impact of inductors saturation on peak-current mode control operation," *IEEE Transactions on Power Electronics*, pp. 1–1, 2020.
- [6] L. Milner and G. A. Rincón-Mora, "Small saturating inductors for more compact switching power supplies," *IEEJ transactions on electrical and electronic engineering*, vol. 7, no. 1, pp. 69–73, 2012.
- [7] Z. Özkan and A. M. Hava, "Inductor saturation compensation in threephase three-wire voltage-source converters via inverse system dynamics-I," *Submitted Manuscript*, 2020.
- [8] Z. Özkan and A. M. Hava, "Inductor saturation compensation with resistive decoupling for single-phase controlled vsc systems," *IEEE Transactions on Power Electronics*, vol. 35, no. 2, pp. 1993–2007, Feb. 2020.
- [9] G. Di Capua, N. Femia, and K. Stoyka, "Validation of inductors sustainable-saturation-operation in switching power supplies design," in 2017 IEEE International Conference on Industrial Technology (ICIT), pp. 242–247, 2017.
- [10] Z. Özkan, High performance current control methods for voltage source converters with saturable inductors. PhD thesis, Middle East Technical University, June 2019.
- [11] "Ieee standard for interconnection and interoperability of distributed energy resources with associated electric power systems interfaces," *IEEE Std 1547-2018 (Revision of IEEE Std 1547-2003)*, pp. 1–138, 2018.
- [12] FNN/VDE, "Power generation systems connected to the low-voltage distribution network-technical minimum requirements for the connection to and parallel operation with low-voltage distribution networks," 2011.
- [13] W. Bartels, F. Ehlers, K. Heidenreich, R. Hüttner, H. Kühn, T. Meyer, T. Kumm, J. Salzmann, H. Schäfer, and K. Weck, "Technical guideline generating plants connected to the medium-voltage network. guildeline for generating plants' connection to and parallel operation with the medium-voltage network," *BDEW Bundesverband der Energieund Wasserwirtshaft e. V.(German Association of Energy and Water Industries)*, 2008.
- [14] L. G. Franquelo, J. Napoles, R. C. P. Guisado, J. I. Leon, and M. A. Aguirre, "A flexible selective harmonic mitigation technique to meet grid codes in three-level pwm converters," *IEEE Transactions on Industrial Electronics*, vol. 54, pp. 3022–3029, Dec 2007.

- [15] F. Wang, J. L. Duarte, M. A. M. Hendrix, and P. F. Ribeiro, "Modeling and analysis of grid harmonic distortion impact of aggregated dg inverters," *IEEE Transactions on Power Electronics*, vol. 26, pp. 786– 797, March 2011.
- [16] M. Kang, S. Lee, and Y. Yoon, "Compensation for inverter nonlinearity considering voltage drops and switching delays of each leg's switches," in 2016 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 1–7, 2016.
- [17] K. Wiedmann, F. Wallrapp, and A. Mertens, "Analysis of inverter nonlinearity effects on sensorless control for permanent magnet machine drives based on high-frequency signal injection," in 2009 13th European Conference on Power Electronics and Applications, pp. 1–10, 2009.
- [18] Y. Park and S. Sul, "Implementation schemes to compensate for inverter nonlinearity based on trapezoidal voltage," *IEEE Transactions on Industry Applications*, vol. 50, no. 2, pp. 1066–1073, 2014.
- [19] S. Zhou, J. Liu, L. Zhou, and H. She, "Cross-coupling and decoupling techniques in the current control of grid-connected voltage source converter," in 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 2821–2827, 2015.
- [20] S. Zhou, J. Liu, L. Zhou, and H. She, "Cross-coupling and decoupling techniques in the current control of grid-connected voltage source converter," in 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 2821–2827, 2015.
- [21] F. Briz, M. W. Degner, and R. D. Lorenz, "Analysis and design of current regulators using complex vectors," *IEEE Transactions on Industry Applications*, vol. 36, no. 3, pp. 817–825, 2000.
- [22] K. Ogata and Y. Yang, *Modern control engineering*. Prentice Hall, 3rd ed., 2002.
- [23] Z. Özkan and A. M. Hava, "Current control of single-phase vsc systems with inductor saturation using inverse dynamic model-based compensation," *IEEE Transactions on Industrial Electronics*, vol. 66, pp. 9268–9277, Dec. 2019.
- [24] S. K. Sul, Control of electric machine drive systems. John Wiley & Sons, 2011.
- [25] W. Taha, A. R. Beig, and I. Boiko, "Design of pi controllers for a gridconnected vsc based on optimal disturbance rejection," in *IECON 2015* - 41st Annual Conference of the IEEE Industrial Electronics Society, pp. 001954–001959, 2015.
- [26] J. Dannehl, C. Wessels, and F. W. Fuchs, "Limitations of voltageoriented pi current control of grid-connected pwm rectifiers with LCL filters," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 2, pp. 380–388, 2009.
- [27] M. P. Kazmierkowski and L. Malesani, "Current control techniques for three-phase voltage-source pwm converters: a survey," *IEEE Transactions on Industrial Electronics*, vol. 45, pp. 691–703, Oct 1998.
- [28] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an LCLfilter-based three-phase active rectifier," *IEEE Transactions on Industry Applications*, vol. 41, no. 5, p. 1281, 2005.
- [29] A. M. Hava and N. O. Cetin, "A generalized scalar pwm approach with easy implementation features for three-phase, three-wire voltage-source inverters," *IEEE Transactions on Power Electronics*, vol. 26, no. 5, pp. 1385–1395, 2010.
- [30] "Inductor core datasheet 0077908a7." [Online] Available: https://www.mag-inc.com/Media/Magnetics/Datasheets/0077908A7.pdf Accessed March 6, 2018.
- [31] V. Kaura and V. Blasko, "Operation of a phase locked loop system under distorted utility conditions," *IEEE Transactions on Industry Applications*, vol. 33, no. 1, pp. 58–63, 1997.