Fundamentals and SPICE Implementation of the Dynamic Memdiode Model for Bipolar Resistive Switching Devices

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Abstract

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***Abstract*— This paper reports the fundamentals and SPICE implementation of the dynamic memdiode model (DMM) for the conduction characteristics of bipolar resistive switching (RS) devices. Following Chua's memristive devices theory, the memdiode model comprises two equations, one for the electron transport based on a heuristic extension of the quantum point-contact model for filamentary conduction in dielectrics and a second equation for the internal memory effect related to the reversible displacement of atomic species within the oxide film. The DMM represents a breakthrough with respect to the previous quasi-static memdiode model (QMM) since it describes the memory state of the device as a rate balance equation incorporating both the snapback and snapforward effects, features of utmost importance for the accurate and realistic simulation of the RS phenomenon. The DMM allows simple setting of the memory state initial condition as well as separate modeling of the set and reset transitions. The model equations are implemented in the LTSpice simulator using an equivalent circuital approach with behavioral components and sources. The practical details of the model implementation and its use are thoroughly discussed.**

***Index Terms*—memristor, resistive switching, memory**

I. Introduction

Selecting an appropriate generic model for an electron device is far from being simple and straightforward. The model should be able to cover not only the basic features but also the distinctive details of the system under study. For circuit simulation-oriented models, this capacity of adaptation must be achieved by means of a reduced number of robust and differentiable equations controlled by a reduced number of parameters, if possible, with physical origin, if not, with some degree of electrical meaning. This is the signature of a compact behavioral approach. Clearly, accurate representation of the electron transport across the device under arbitrary input signals is twofold: first, encourages the design and simulation of more complex circuits and systems and second, allows to identify and arrange the elementary pieces that lead to the variety of observed behaviors. Since the first practical description of a memristive device by HP in 2008 [1], a number of compact models for the current-voltage (*I-V*) characteristic of resistive switching (RS) devices have been proposed [2]. Because of the hysteretic nature of the phenomenon (see Fig.1), the electron transport model requires supplementary information about the previous history of the device. Here is where Prof. Chua's theory of memristive devices comes into play [3]. According to this theory, a physical or electrical variable driven by a first order differential equation determines the current that flows through the structure. In this work, we will not discuss previous approaches since the reader can find excellent review papers on the subject [4-10]. Instead, we will concentrate on our own view of the filamentary conduction problem. The origin of the memdiode model is the double-diode circuit with a single series resistance driven by the Krasnosel'skii-Pokrovskii hysteresis operator [11]. Although a time module can be incorporated into the base model [12], this is in essence a quasi-static model (QMM) because the memory state of the device does not change unless a threshold condition is surpassed. The main advantage of this approach is the elimination of the integration step in favor of the use of the so-called hysteron or memory map. In this work, we report the fundamentals and the SPICE implementation of the dynamic memdiode model (DMM). This is a breakthrough with respect to the previous model since the DMM is based on a balance memory equation which includes both the snapback and snapforward effects. In addition, the model takes into account the non-linearity of the *I-V* characteristic and the roles played by fixed and variable series resistances.

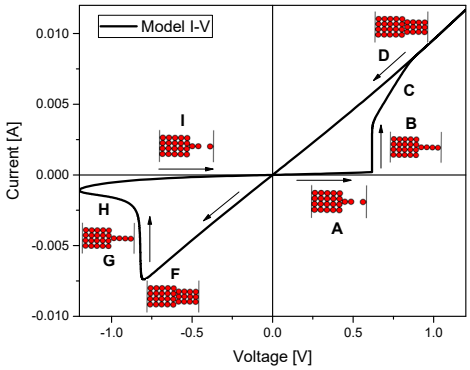

Fig.1: Hysteretic behavior of the filamentary-type *I-V* characteristic. Filament stages: A) formation, high resistance state (HRS), B) completion, C) expansion, D,F) complete expansion, low resistance state (LRS), G) dissolution, I) rupture.

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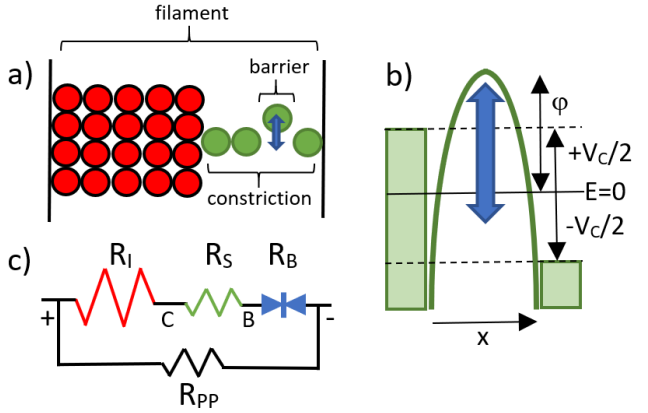

Fig.2: a) Schematic of the filamentary structure: static and dynamic part. b) Schematic of the tunneling barrier/gap. φ is the barrier height. c) Representation of the QPC model using an equivalent circuit approach.

II. Dynamic Memdiode Model (DMM)

In this Section, the two equations that define the DMM are presented and discussed. They are: *i)* the current-voltage (*I-V*) characteristic and *ii)* the memory state equation (λ-*t*). The very basic idea behind this model is that the current flows through a kind of filamentary structure embedded in the oxide layer in which some of its atomic constituents can reversibly move in and out according to the forces exerted by the external field. This in turn alters the overall transmission properties of the structure leading to the system's hysteretic behavior. The model can be appropriately modified so as to cover non-filamentary-type conduction as well.

i) Current-voltage characteristic

According to the quantum point-contact (QPC) model [13-16], the current that flows through a single nanosized filamentary structure (see Fig. 2a) can be calculated using the finite-bias Landauer formula [17]:

$$I(V_C) = \frac{2e}{h}\int_{-\infty}^{+\infty} T(E)[f(E - eV_C/2) - f(E + eV_C/2)]dE \quad (1)$$

where V_C=V-IR_I is the potential drop across the constriction, V the applied voltage, R_I the internal/external series resistance (permanent section of the filament/wire resistance), E the energy, f the Fermi-Dirac function, and T the transmission coefficient for the confinement barrier. e and h are the electron charge and the Planck constant, respectively. (1) can be extended to the case of asymmetric potential drops at the two ends of the constriction using a coefficient different from ½ for the energy window. Assuming an inverted parabolic potential barrier for the constriction's bottleneck (scatterer), $T(E)$ is expressed as:

$$T(E) = \frac{1}{1+exp[-\theta(E-\varphi)]} \quad (2)$$

where θ is the barrier shape factor and φ the barrier height (see Fig. 2b). In the pure tunneling regime (φ>>E) and zero-temperature limit, (1) and (2) yield [18]:

$$I(V_C) \approx \frac{4e}{\theta h} exp(-\theta\varphi) sinh\left(\frac{\theta e V_C}{2}\right) \quad (3)$$

Notice that, if the barrier width collapses ($\theta \to 0$) because of the completion of the filament, (3) results in the standard Landauer formula I=G_0V_C, where G_0=$2e^2/h$ is the quantum conductance unit. The effect of θ on the *I-V* curve is illustrated in Fig. 3a. Combining (3) in the linear regime (V_C<<1) with (2), we obtain:

$$V_C \approx \frac{1}{G_0} exp(\theta\varphi) I = \frac{1}{G_0}\left(\frac{1-T(E=0)}{T(E=0)}\right) I \quad (4)$$

Since in a mesoscopic system, the constriction resistance R_C can be regarded as the sum of the contact (or Landauer) resistance R_L and the scatterer resistance R_B as [17]:

$$R_C = \frac{1}{G_0 T} = \frac{1}{G_0} + \frac{1}{G_0}\left(\frac{1-T}{T}\right) = R_L + R_B\,, \quad (5)$$

we can associate (4) with R_B. However, it is clear from (5) that not only the confinement barrier contributes to the constriction resistance but also the way the constriction is attached to the charge reservoirs (or thermalizing region of the filament) through R_L. As is well known, this is a consequence of the funneling effect of the electron wavefunction caused by the mismatch in the number of available energy states when passing from the reservoir to the constriction and *vice versa*.

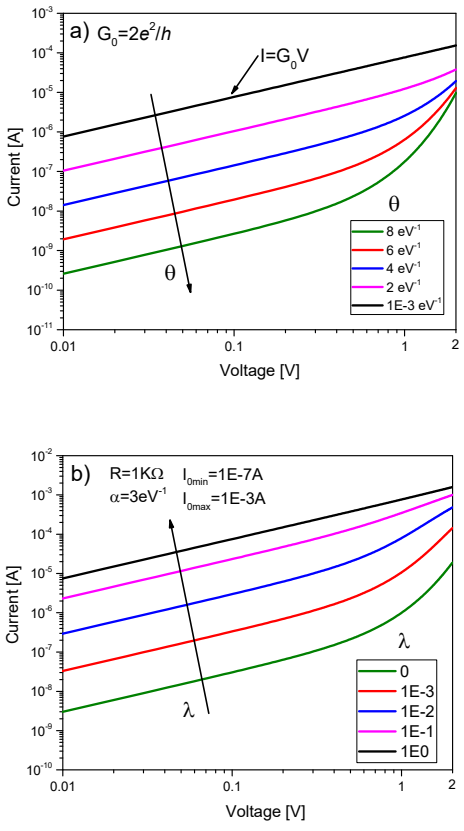

Fig.3: a) Single filament conduction characteristic and effect of the parameter θ. b) Multiple filament conduction characteristic and effect of the parameter λ.

Since, in general, for a wider constriction formed by a bunch of conducting channels neither the number N of elemental filamentary structures involved is known nor their barrier parameters θ_i and φ_i can be accessed individually [19], we extrapolate (3) to that case using the heuristic approximation:

$$I(V_C) = I_0 sinh[\alpha(V_C - R_S I)] \quad (6)$$

which has the same functional asymptotes as the original equation (3) for large I_0 values ($R_S I \approx V_C$) and low applied voltages ($R_S I << V_C$) (see Fig. 3b). While R_S in (6) accounts for the contact resistance, the hyperbolic sine function expresses the barrier resistance (see Fig. 2c). R_{PP} represents the device resistance before the forming event. A central difference between R_S and R_I, is that R_S will be allowed to change (if necessary) according to the memory state of the device (movement of ions/vacancies). Moreover, notice that (6) does not correspond strictly to N times the current flowing through a single filament, otherwise a parallel shift of (3) towards higher current values would be obtained [20]. In addition, (6) complies with the pinched condition $I(V=0)=0$ and, because of its heuristic nature, overcomes the physical limitation on the voltage drop $eV_C/2 \leq \varphi$ imposed by (3). Physically, the moving species in Fig. 2.a represent the hopping of ions/vacancies induced by the external applied field. As schematically illustrated in Fig. 2.b, the opening (RESET) or closing (SET) of the atom chain raises or lowers the top of the confinement barrier for the electron flow [21,22]. According to this picture, ballistic transport would not be required along the whole filament structure but just at the narrowest section of the constriction. For a complete review about conductance quantization effects in RS devices see Refs.[23-31].

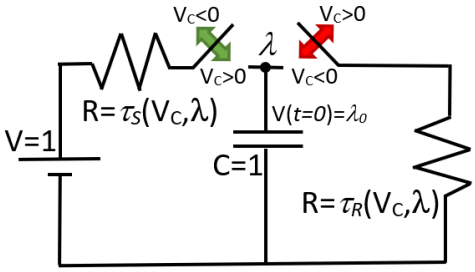

Fig.4: Equivalent circuit model for the memory state equation. The switching times τ_S and τ_R are regarded as variable resistances. The state of the switches depends on the sign of the applied voltage. The memory state λ is the voltage across the capacitor. λ_0 is the initial memory state.

From the electrical viewpoint, (6) can be envisaged as two opposite biased diodes (see Fig. 2c) with a single series resistance [2]. Since these are not real diodes, inverse saturation currents are disregarded. This was the approach followed in our previous works and justifies the origin of the name memdiode [11], *i.e.* a diode with memory. The main point is that (6), as shown in Fig. 3b, self-rectifies the *I-V* curve as the device switches from HRS (linear-exponential) to LRS (linear), which is in agreement with many experimental observations. (6) is implemented in LTSpice XVII from Linear Technologies using two resistors (R_S and R_I) in series with a behavioral voltage-controlled hyperbolic sine current source with amplitude factor given by the expression:

$$I_0(\lambda) = (I_{0max} - I_{0min})\lambda + I_{0min} \quad (7)$$

where $0 \leq \lambda \leq 1$ is the memory state variable, and I_{0min}, I_{0max} are calibration parameters (minimum and maximum currents, respectively). $\lambda=0$ and $\lambda=1$ correspond to HRS and LRS, respectively. The linear relationship between I_0 and λ is a key feature of the model and likely reflects the connection between the memory state and the density of conducting sites or the cross-section area of the filamentary structure [32,33]. The effect of λ on the *I-V* curve is illustrated in Fig. 3b. As λ increases the *I-V* curve becomes more linear as expected for an ohmic-type conducting channel. Notice that, at low biases, the HRS *I-V* is also linear. Importantly, I_{0min} and I_{0max} control the barrier resistance and do not refer directly to the minimum and maximum currents that are allowed to flow across the device. This will be ultimately determined by the whole system's dynamics. For the sake of completeness, α and R_S receive a similar treatment in the LTSpice script to that given to $I_0(\lambda)$. Both parameters can be swept from a minimum to a maximum if required. If not, α and R_S can remain fixed. Next, we discuss the memory state equation and its circuital implementation.

ii) Memory state equation

As reported in [34], a very convenient differential equation for the memory state variable λ that complies with a number of experimental observations in memristive structures is:

$$\frac{d\lambda}{dt} = \frac{1-\lambda}{\tau_S(\lambda,V_C)} - \frac{\lambda}{\tau_R(\lambda,V_C)} \quad (8)$$

where $\tau_{S,R}$ are characteristic times associated with the SET ($V>0$) and RESET ($V<0$) transitions, *i.e.* with the ionic/defect movement within the dielectric film in one or the opposite direction. (8) can be regarded as the normalized version of a birth-death process for a two-state system with transition rates τ_S^{-1} and τ_R^{-1}:

$$X \underset{\tau_R^{-1}}{\overset{\tau_S^{-1}}{\rightleftarrows}} Y \quad (9)$$

in which there are n_1 particles in the state X and n_2 particles in the state Y, with $n_1+n_2=N$ the total number of particles. This comes to represent for example the REDOX process in VCMs [35]. Notice that $\tau_{S,R}$ in (8) are expressed as a function of V_C and λ. In our case, where SET and RESET only occur for biases with opposite signs, (8) can be treated as two separate differential equations, one for $V>0$ and one for $V<0$. This is not mandatory but simplifies the model calibration since the SET and RESET processes become largely disentangled (but not completely). Under this consideration, (8) can be represented by the equivalent circuit schematic depicted in Fig. 4. λ corresponds to the voltage drop across the capacitor C=1F. Notice that the memory state behavior during the RS cycle is nothing but the alternate action of two RC circuits. The charge and discharge characteristic times are governed by the respective resistance values. The green and red arrows in Fig. 4 indicate the position of the switches as a function of the sign of V_C. In practice, the switches are modeled by two behavioral *if* statements in the LTSpice script. Notice that the voltage source in the circuit is always V=1V. This value has no connection with the applied signal and is just a consequence of the differential

equation (8). The initial condition for the memory state is introduced through the initial voltage drop across the capacitor as $V(t=0)=\lambda_0$. In the LTSpice script, λ is represented by the capital letter H (for hysteron). In fact, $\lambda=V(\mathrm{H})$ is the voltage at the H node.

Both in the SET and RESET regions, the corresponding characteristic switching times can depend implicitly or explicitly on λ. This property is used to represent the so-called snapback (SB: positive bias) and snapforward (SF: negative bias) effects in the RS *I-V* loop. These effects are typically present in VCMs [36]. In this work, we introduce explicitly the memory state λ in the characteristic times as:

$$\tau_S(\lambda, V_C) = exp[-\eta_S(V_C - V_S(\lambda))] \quad (10)$$

and

$$\tau_R(\lambda, V_C) = exp[\eta_R \lambda^{\gamma}(V_C - V_R)] \quad (11)$$

where $\eta_{S,R}$ and $V_{S,R}$ are the transition rates ($\eta_S, \eta_R > 0$) and the reference switching voltages ($V_S > 0$, $V_R < 0$), respectively. $\gamma \geq 0$ is referred to as the SF coefficient. The exponential dependences of (10) and (11) on V_C are a consequence of the ions/vacancies dynamics associated with the hopping mechanism [37,38]. Deviations from these exponential laws in the low voltage region have also been reported but are disregarded in this work [39].

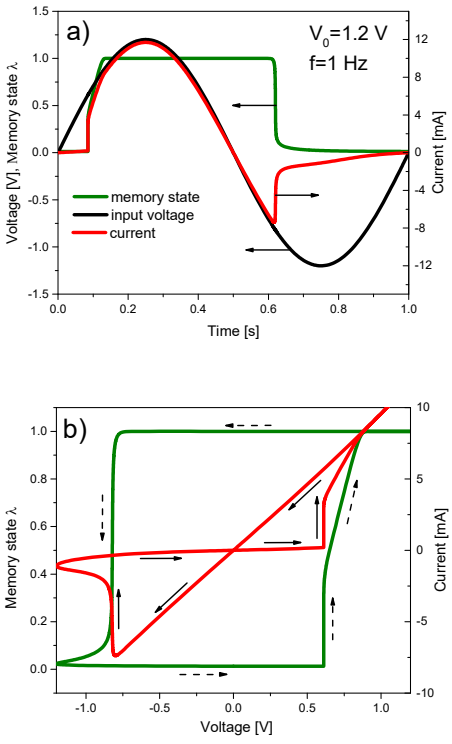

Fig.5: a) Simulation example for the current and memory state as a function of time a sinusoidal signal. b) Evolution of the memory state (hysteron) and current as a function of the applied voltage.

If for any reason, the SB and SF effects do not need to be considered, taking $V_S(\lambda)=V_S$ a constant reference SET voltage and $\lambda^{\gamma}=1$ in (10) and (11), respectively, the switching dynamics becomes exclusively voltage-controlled as originally assumed in [34]. This behavior is typical of ECM cells in which abrupt RESET transitions are observed. Under these latter conditions, (8) has analytic solution both for the constant and ramped voltage input signal cases. In any other case, because of the mathematical complexity involved, (8) must be numerically solved with the help of a differential equation solver (in our case the circuit simulator itself). In the following Section, the practical implementation and consequences of the above mentioned effects on the *I-V* curve are discussed.

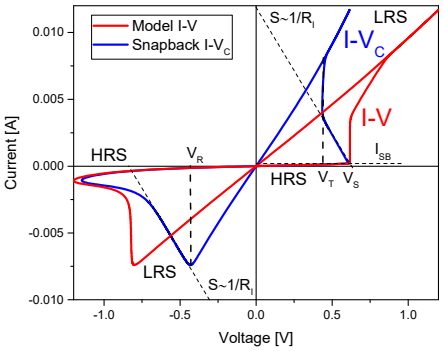

Fig.6: Original *I-V* curve (red line) and its snapback correction $I\text{-}V_C$ (blue line). V_T is the transition voltage, V_R the reset voltage, V_S the set voltage, R_I the internal series resistance, I_{SB} the snapback triggering current.

III. Simulation Results and Discussion

In order to test the ability of the proposed model to deal with realistic simulations, a number of evaluation criteria must be adopted and assessed. In this work, we basically consider Linn's criteria [40] to which we add some very specific features not included in the referred work. These criteria are: *i*) capability of the compact model to reproduce the RS *I-V* characteristics including the SB and SF effects, *ii*) realistic switching dynamics for SET and RESET transitions including the ability of the model to deal with arbitrary input signals (continuous and discontinuous), and *iii*) multi-device connectivity in the form of Complementary Resistive Switching (CRS). These three major issues are discussed in detail next. Before entering into the discussion, it is worth mentioning that because of the complexity of the numerical problem involved, caution should be exercised with the selection of the model parameters values. Although the DMM is robust enough, certain combination of parameters could lead to fatal errors of convergence or to extremely long simulation times. Sometimes the numerical problems disappear by simply changing the maximum simulation timestep (shorter or longer), signal excursion, or numerical method used (trapezoidal, modified trap, Gear). Depending on the required accuracy, simplifying the model equations by eliminating unnecessary details (SB, SF, resistances, limiting functions, etc.) is also a good strategy to follow. The roles played by parameters I_0, α, and R_S in the HRS and LRS *I-V* curves are not analyzed here since they were discussed elsewhere in connection with the QMM [12]. Notice that the QMM is also part of the DMM LTSpice script and can always be used as the starting point of any simulation exercise.

The main difference between both models resides in the how the SET and RESET transitions are modeled. QMM requires a threshold voltage/current to induce the transitions, while DMM does not. The *I-V* expression (6) is common to both models.

i) Snapback and snapforward effects

To begin with, Fig. 5 illustrates typical *I-V* and λ-*V* loops obtained using (6) and (8). The LTSpice script and model parameters for this particular exercise can be found in the Supplementary Information of this paper. While in Fig. 5a, the sinusoidal input voltage, the memory state and the current flowing through the structure are plotted as a function of time, Fig. 5b illustrates the current evolution and the memory map (hysteron) of the device as a function of the applied voltage [41].

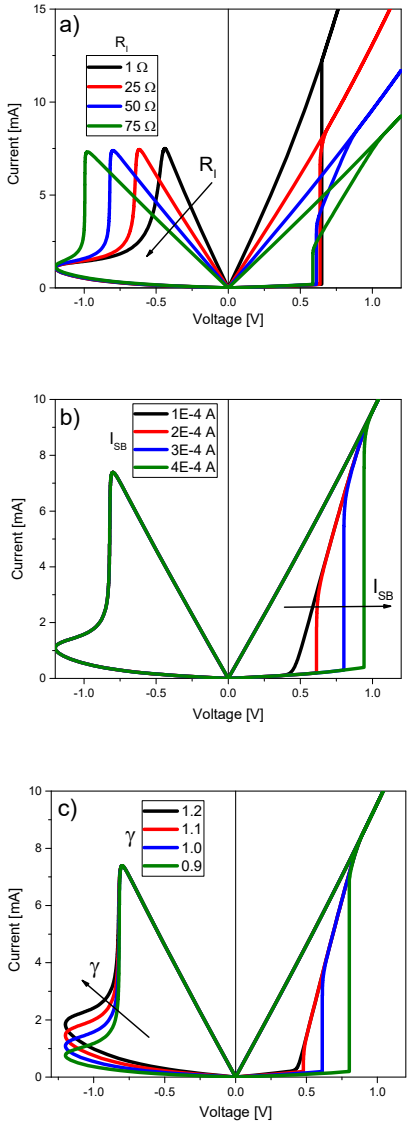

Fig.7: Effect of the DMM parameters on the *I-V* characteristic: a) internal/external series resistance R_I, b) snapback triggering current I_{SB}, and c) snapforward coefficient γ.

More in detail, the SB effect is recognized by the sudden current increase in the SET region (red line in Fig. 6) caused by the reduction of the constriction resistance that occurs when the tunneling gap or confinement barrier vanishes (the CF is completely formed). During this phase the current also grows as a function of V_C but following approximately the load line of the circuit (slope~$1/R_I$), and next at an almost constant voltage called the transition voltage V_T (blue line in Fig. 6) [36]. This second phase corresponds to the accumulation of ions/defects in the constriction (or alternatively to its lateral expansion) with the consequent progressive resistance reduction. This behavior has been reported many times in the literature [42] but has received scarce attention in the compact simulation field. V_T is the minimum voltage required to move the ions/vacancies and its value seems to be not only a characteristic parameter of each material but also a function of measurement variables such as the voltage ramp rate or signal frequency [43].

The SB effect is incorporated into the model equations by modifying the SET reference voltage V_S($>V_T$) in (10) according to the rule:

$$V_S(I) = \begin{cases} V_T & I \geq I_{SB} \\ V_S & I < I_{SB} \end{cases} \qquad (12)$$

where I is the current flowing through the device. (12) is a switching rule based on the current value, but other rules based on the voltage or memory state are also admissible [44]. I_{SB} is a threshold current for the SB effect. (12) is written as an *if* statement for the SET voltage in the LTSpice script and expresses a collapse of the nominal SET voltage V_S to a lower value V_T after reaching the threshold condition I_{SB}. This event generates a sudden current increase compatible with the voltage drop along the load line of the circuit. It is worth mentioning that the SB effect is not always observable since its detection depends on a number of factors linked to the specific features of the device under test and to the measurement conditions. When combined with other parameters (I_{min} and R_{PP}), V_S can also be used to represent the forming step (see Supplementary Information). This may require code edition for a specific conduction mechanism (Schottky, Fowler-Nordheim, etc.) in the fresh device [45].

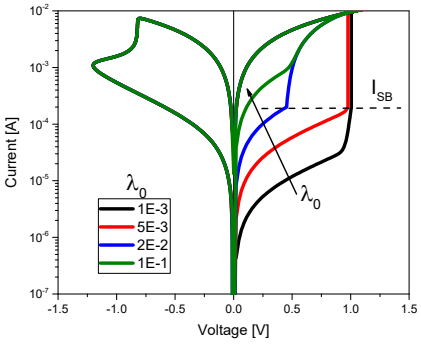

Fig.8: Effect of the initial memory state λ_0 on the *I-V* characteristic.

For the opposite polarity (V<0), after the SF event (current decrease following the circuit load line with slope~$1/R_I$), the main difference appears at the low current region, once the filament is almost dissolved. In this case, since λ approaches

zero as the current drops, the factor λ^{γ} gains weight in equation (11) reducing the RESET characteristic time. The result is remarkable since the current deviates from the load line generating a lobe. In other words, as the current decreases, larger voltages are required to deplete the constriction from conducting atomic species up to the point in which the initial gap or tunneling barrier is completely restored. Alternatively, this can be view as a reduction of the electric field caused by the increase of the tunneling gap width. The referred protuberance is clearly visible in many VCM-type devices but rarely observed in ECM-type structures, which exhibit more abrupt transitions [46,47]. Although V_R is considered an independent model parameter in the LTSpice script, in general V_R=-V_T is found, which is consistent with a field-induced activation of the SET/RESET processes in bipolar RS devices.

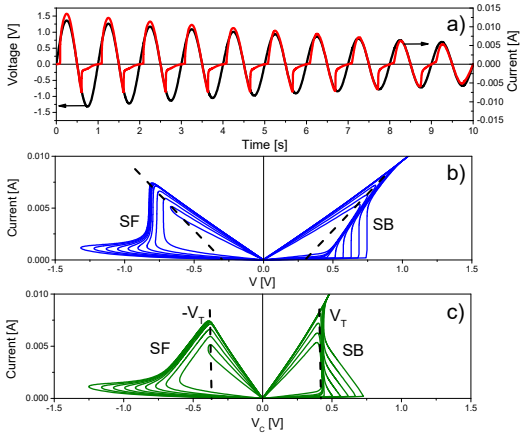

Fig.9: a) Application of a damped sinusoidal voltage on the memdiode *I-t* characteristic, b) *I-V* curve with minor loops, and c) *I-V*$_C$ curve. V_T is the transition voltage.

Figure 7 illustrates the effects of some of the model parameters on the *I-V* curve. The analysis is carried out on the second *I-V* loop, *i.e.* once the transient effects associated with the initial loop or forming process play no role. As shown in Fig. 7a, R_I mainly affects the slope of the LRS *I-V* curve and the apparent RESET voltage. The small shift in the SET voltage is a consequence of the modifications that occurred in the RESET region after the first loop. Remarkable changes are also observed in the *I-V*$_C$ curve (see below). Figure 7b illustrates the effects of the threshold current I_{SB}. As this parameter increases, the completion of the filament takes place at a higher voltage thus reducing the observable effects associated with V_T. No change is detected in the RESET transition since the LRS *I-V* remains unaltered. Figure 7c illustrates the effects of the SF parameter γ. The main effect on the RESET transition is the change of the triggering point of the current lobe. Since the HRS current in the RESET region is also affected by this change, γ also alters the triggering point in the SET region. It is also important to mention that the observation of the SB effect in the simulated curve strongly depends on the memory state initial condition (λ_0). As shown in Fig. 8, depending on the HRS current magnitude, the SB triggering point can differ (because the same current value is reached at different voltages). Once the device reaches LRS, the RESET process becomes independent of the initial condition. Subsequent loops do not carry on information about the initial state of the device.

A remarkably property of the *I-V*$_C$ curve which results from the SB transformation (*V-R·I*) of the original *I-V* curve (see Figs. 9a and 9b) is that in addition to the current increase at a constant voltage V_T occurring in the SET region, the minor *I-V*$_C$ loops also peak at -V_T in the RESET region (see Fig. 9c) for V_R=-V_T. This has been experimentally verified in [48] and indicates that the constriction voltage or alternatively the field and not the current magnitude are responsible for triggering the RESET process. As another example of the switching dynamics that can be achieved with the DMM, Fig. 10 shows the case in which the SB effect is not considered. Notice the hard threshold voltage for the SET condition. The *I-V* curve (red line) shows the intermediate current states (minor loops) for a damped sinusoidal input voltage. These states are generated by the hysteron (λ) shown in green.

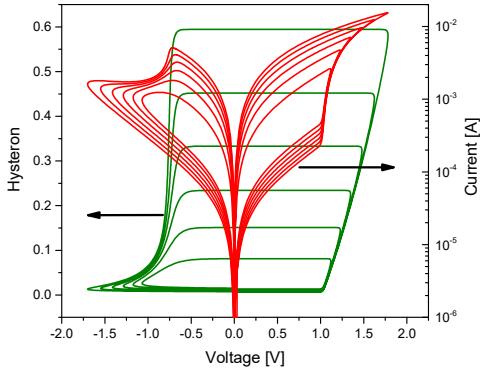

Fig.10: Simulation of intermediate states in the *I-V* characteristic without considering SB effect.

ii) Switching dynamics

As the second criterion for assessing the model behavior, the DMM switching dynamics is discussed next. It is worth emphasizing that the switching properties of the memory equation (8) for constant and ramped voltage signals were reported in [34]. (8) complies with the expected characteristic switching times (SET and RESET) for a constant bias condition (Fig. 11):

$$\tau_{S,R}(V) = \tau_{0S,R} exp\left(\mp V / V_{0S,R}\right) \tag{13}$$

and with the switching voltage value as a function of the applied signal ramp rate (*RR*) and frequency (Fig. 11):

$$V_{S,R} = V_{0S,R} \ln(RR) + V_{0S,R} ln\left(\frac{\tau_{0S,R}}{V_{0S,R}}\right) \tag{14}$$

where $\tau_{0S,R}$ and $V_{0S,R}$ are fitting constants. Although no close-form expression for a sinusoidal input is available, the phenomenology is similar to that expressed by (14).

As shown in Fig. 11, as the applied voltage increases, the maximum recheable current not only increases but also the SET switching time reduces in an exponential manner (see Fig.11's inset). This has been experimentally demonstrated to occur in

many material systems [49]. A similar behavior is obtained for the RESET transition of the device. Figure 12 illustrates the effects of the signal frequency on the *I-V* curve. As the frequency increases, the SET and RESET voltages shift to higher values. This effect is consistent with (14) and has been experimentally observed using ramp rates varying orders of magnitude [50]. Physically, the reason behind this behavior is the voltage-time combined action in the characteristic switching times for the ionic hopping represented by (9) and (10). The current increase observed in the RESET transition (V<0) of Fig. 12 has also been observed as it is a consequence of the increment of the current lobe triggering point [50].

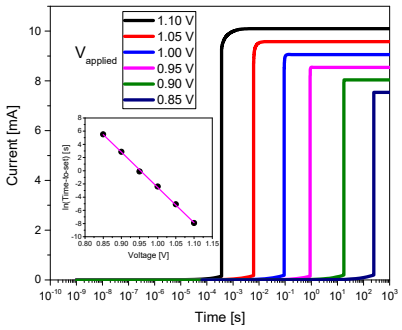

Fig.11: Effect of a constant voltage input signal on the *I-t* characteristic.

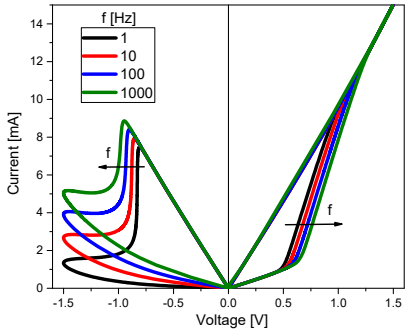

Fig.12: Effect of the signal frequency on the *I-t* characteristic.

Concerning the switching dynamics for discontinuous signals, Fig. 13 illustrates the effects of a sequence of equal amplitude voltage pulses ($V_{applied}$=0.1,0.3,0.4,0.5 V) and period (1 s) on the current magnitude. As shown in Fig. 13a, for a device with an initial memory state λ_0=0 (HRS), the current increases as function of voltage and time. This is the so-called potentiation effect in neuromorphic devices [51]. In addition, for higher voltages, as shown in Fig. 13b, the current not only progressively increases but also switches to LRS after reaching the threshold condition dictated by the SB effect (pulse-induced switching). For negative voltages (see Fig. 13c), the current behaves in a similar fashion. First, the current decreases monotonically but as soon as the RESET condition is met, the current exhibits an abrupt reduction. In this latter case, the device memory state starts at λ_0=1 (LRS).

iii) CRS devices

Complementary Resistive Switching consists in the anti-serial combination of two memristors [52,53]. This is the third criterion selected for evaluation of the DMM. This is an emblematic problem to demonstrate the connection capacity of the devices. CRSs are intended to be used for selector devices in crossbar arrays [43,54]. Different behaviors are experimentally observed depending on the voltage and current window investigated [55-59]. Most of the RS models published to the date are unable to represent all these behaviors.

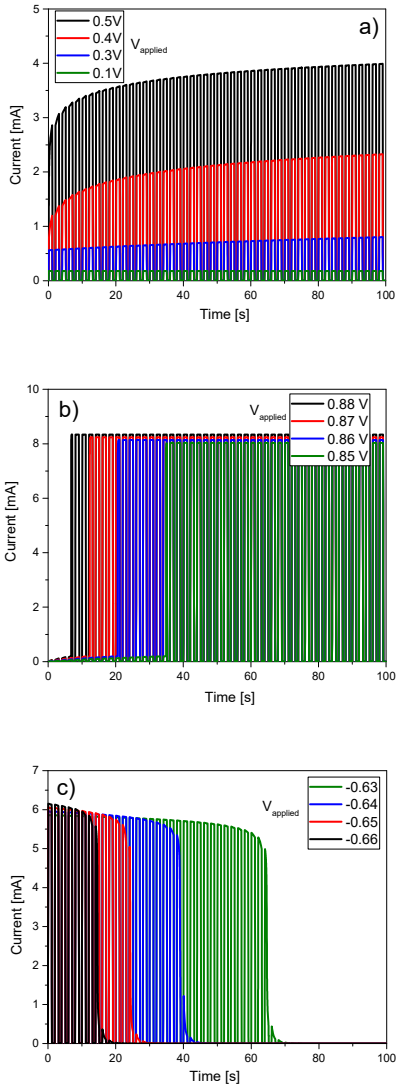

Fig.13: a) Effect of a pulsed signal on the SET *I-t* characteristic, b) similar to a) but with a higher voltage, and c) similar to a) but for a RESET *I-t* curve.

As shown in Fig. 14a, the top device (DMM1) is initially in HRS (λ_0=0) and the bottom device (DMM2) in LRS (λ_0=1). Figure 14 illustrates the combined action of both memdiodes in the stationary loop. The current behavior is characterized by the appearance of two bumps (transmission windows) at opposite voltages. The high current state is reached when both devices are in LRS. Remarkably, different behaviors can be achieved depending on the specific features selected in the simulation model. Figure 13a illustrates three cases or particular interest.

In general, the inclusion of the SB effect yields abrupt HRS/LRS transitions, while the absence of the SB effect leads to smoother transitions. The inclusion of the SF effect with $\lambda' \neq 1$ in (11) results in the appearance of a lobe current in the LRS/HRS transition. In order to understand the complexity of the analyzed problem, Fig. 14b illustrates the potential drop distribution across each device as a function of time for the circuit shown in Fig. 13a when a sinusoidal signal is applied. The figure illustrates the case with SB and without SF effects.

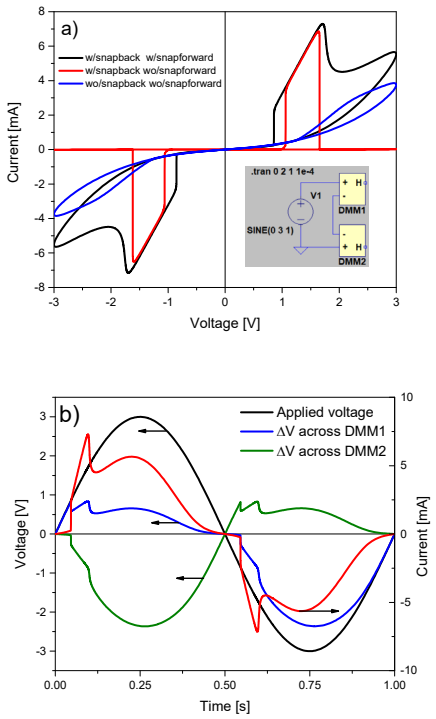

Fig.14: a) *I-V* characteristic for a CRS structure w/o SB and SF. b) Voltage drop distribution as a function of time.

IV. Conclusions

A compact behavioral model for the *I-V* characteristic of bipolar resistive switching devices was presented. The model relies on the combined action of two equations, one for the electron transport and a second one for the memory effect that represents the ion/vacancy displacements. It was shown how the snapback and snapforward effects play a fundamental role during the SET and RESET processes, respectively. The model equations were implemented in the LTSpice simulator but can be easily translated to any other specific simulation language. In summary, the proposed dynamic memdiode model (DMM) is simple, robust and accurate as expected for a fast and reliable simulation involving resistive switching devices.

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Supplementary information

The memdiode model script for LTSpice XVII reported in this Appendix includes not only the DMM but also the QMM. It is important to activate one of the options at a time (DMM or QMM) by inserting asterisks (*) in the corresponding lines. The parameter list, *I-V*, and Auxiliary functions sections are common to both approaches. This does not mean that the obtained curves will be identical. The meaning of the parameters is discussed in the text and in previous papers.

LTSPICE script

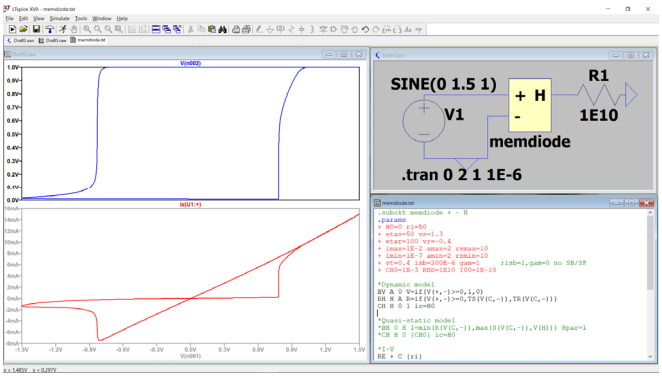
```
.subckt memdiode + - H
*created by E.Miranda & J.Suñé, June 2020
.params
+ H0=0 ri=50
+ etas=50 vs=1.4
+ etar=100 vr=-0.4
+ imax=1E-2 amax=2 rsmax=10
+ imin=1E-7 amin=2 rsmin=10
+ vt=0.4 isb=200E-6 gam=1 gam0=0 ;isb=1/gam=0 no SB/SF
+ CH0=1E-3 RPP=1E10 I00=1E-10
*Dynamic model
BV A 0 V=if(V(+,-)>=0,1,0)
RH H A R=if(V(+,-)>=0,TS(V(C,-)),TR(V(C,-)))
CH H 0 1 ic={H0}
*Quasi-static model
*BH 0 H I=min(R(V(C,-)),max(S(V(C,-)),V(H))) Rpar=1
*CH H 0 {CH0} ic={H0}
*I-V
RE + C {ri}
RS C B R=RS(V(H))
BD B - I=I0(V(H))*sinh(A(V(H))*V(B,-))+I00
RB + - {RPP}
*Auxiliary functions
.func I0(x)=imin+(imax-imin)*limit(0,1,x)
.func A(x)=amin+(amax-amin)*limit(0,1,x)
.func RS(x)=rsmin+(rsmax-rsmin)*limit(0,1,x)
.func VSB(x)=if(x>isb,vt,vs)
.func ISF(x)=if(gam==0,1,pow(limit(0,1,x),gam)-gam0)
.func TS(x)=exp(-etas*(x-VSB(I(BD))))
.func TR(x)= exp(etar*ISF(V(H))*(x-vr))
.func S(x)=1/(1+exp(-etas*(x-VSB(I(BD)))))
.func R(x)=1/(1+exp(-etar*ISF(V(H))*(x-vr)))
.ends
```

Some hints:

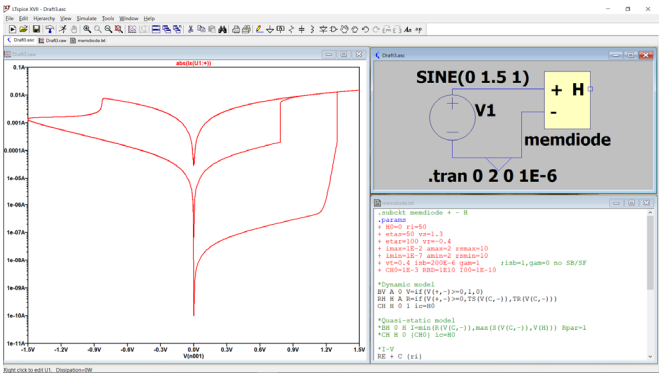
- If not necessary, keep the hysteron output H open. If used to plot the memory state of the device, consider a very large output resistance (1E10Ω) connected to ground.
- Different combinations are allowed: w/wo SB or w/wo SF effects in both models. isb=1 deactivates SB and gam=0 deactivates SF. All the auxiliary functions are active.
- Try to use amax=amin (alpha), rsmax=rsmin (series resistance) and vr=-vt (transition voltage).
- In QMM, CH0 must be in principle selected so as to reach V(H)=1 in the LRS condition. CHO must be chosen according to the input signal frequency. Always check V(H).
- In case of convergence error, try different maximum timesteps, change the amplitude of the input signal or integration method. A *limit* function is used to avoid numerical spikes generated by the memory equation.
- Do not consider the first loop for stationary conditions (independent of H0).
- RPP is a parallel resistance used to simulate the fresh device
- I00 is use for avoiding the pinched condition for graphical use but can be eliminated for computation
- $(\lambda^{\gamma}\text{-}\gamma_0)$ can be replaced by 1-exp[-A*(λ-B)], A≈1,B≈0.1. Alternative expressions can be tested.
- Once you select the required model (QMM or DMM), you can delete all what you are not going to use.

Some examples:

1) Hysteron and *I-V* characteristic

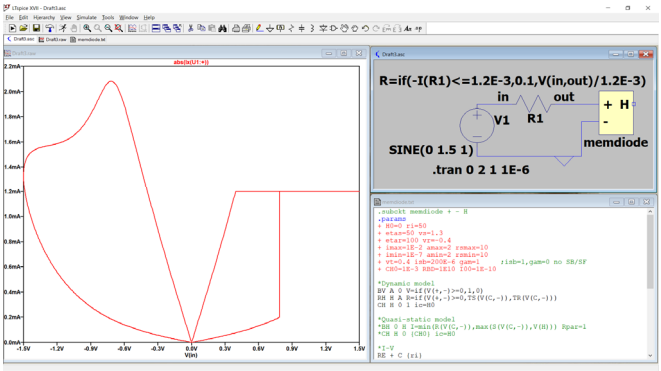


2) *I-V* characteristic including electroforming



vs in combination with isb are used to determine the forming voltage.

c) *I-V* characteristic with compliance in SET condition



The variable resistance limits the voltage so as not to surpass the current limit.