f noise model based on trap-assisted tunneling for ultra-thin oxides MOSFETs

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October 30, 2023

Abstract

We derive an analytical model for 1/f noise in MOSFETs, highlighting a term that is often neglected in literature but becomes important for ultra-thin oxides. Furthermore, we identify an interesting relationship between the thermal noise of the gate impedance and the gate noise due to trapping/detrapping between the free carriers in the channel and the oxide traps, as well as the 1/f noise cross-correlation between drain and gate, showing that a single voltage noise generator is not enough to describe completely the 1/f noise. TCAD simulations are used to verify the model predictive capabilities.

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***Abstract*—We derive an analytical model for 1/f noise in MOSFETs, highlighting a term that is often neglected in literature but becomes important for ultra-thin oxides. Furthermore, we identify an interesting relationship between the thermal noise of the gate impedance and the gate noise due to trapping/de-trapping between the free carriers in the channel and the oxide traps, as well as the 1/f noise cross-correlation between drain and gate, showing that a single voltage noise generator is not enough to describe completely the 1/f noise. TCAD simulations are used to verify the model predictive capabilities.**

***Index Terms*—1/f, noise, TCAD, TAT, modelling, traps, cross-correlation noise, carrier number fluctuations, elastic tunneling, inelastic tunneling**

I. Introduction

This paper presents a modelling technique to accurately estimate 1/f noise in MOSFETs biased in the linear region. The study will focus on carrier number fluctuations, meaning that the noise is caused by the variations of free carriers in the channel due to charge trapping/de-trapping in oxide traps [1]. Mobility fluctuation will not be considered at this stage, given that its contribution is generally less significant [2]. Moreover, also diffusion noises will not be considered, as this paper focuses on 1/f noise only.

1/f noise in MOSFETs is of paramount importance in RF circuits, where low frequency noise is up-converted and significantly impacts the overall performance of high frequency circuits such as oscillators [3]. In modern technologies, the introduction of high-k materials and advanced gate stack, has further increased the importance of 1/f noise for transient variability and the interest in noise for accurate and reliable measurement of interface and oxide properties. Conventional techniques, such as impedance spectroscopy (C-V and G-V), are not feasible for nanoscale devices whose characterization instead often relies on 1/f noise measurements and comparison with models to infer the concentration of traps. As a result, the accuracy of the estimation clearly depends on the accuracy of the model employed.

We derive here a 1/f model that differs from most of the ones used in literature mainly by two aspects. Firstly, the noise is described by two noise current generators, one in the drain and one in the gate port instead of the single noise voltage generator usually employed in compact 1/f models [4]. Secondly, our model has an additional term $\left(1-\frac{x}{t_{ox}}\right)^2$ that takes into account the position of the traps in the oxide. This term "weights" the effect of the traps, based on their position in the oxide and has a bigger effect as the oxide thickness scales down. As of nowadays oxide thicknesses, this term cannot be neglected, since it could introduce errors of several order of magnitude in the estimation of the noise. The presence of the $\left(1-\frac{x}{t_{ox}}\right)^2$ term in the drain noise generator expression has been already derived in [5] back in 1972, but the formula has been approximated for large oxides. This approximation, reasonable at that time, has become so common that the additional term is hardly seen in new publications, even when thin oxides are treated [6]- [9]. This has been aided by the fact that no specific study, to our notice, has evaluated the effect of this term on the 1/f spectra.

In this study a small-signal Y-matrix noise representation will be used. Thanks to this general approach, a complete noise description composed by two correlated noise generators at the gate and drain ports will be obtained. We show that the $\left(1-\frac{x}{t_{ox}}\right)^2$ term changes the correlation between drain and gate noise induced by trapping/de-trapping leading to the necessity of including two noise current generators in the model instead of a single noise current generator.

The paper proceeds as follows. In section II, the derivation of the model will be presented, starting from a single layer of traps and successively extending the results to the case where the traps are distributed along the oxide. In section III, a relationship between thermal noise of the gate conductance and gate noise due to trapping will be identified. In section IV, the main results will be validated through TCAD simulations [10]. Finally, the concluding section draws the main implications of the results.

II. Model derivation

A. RC distributed circuit to describe gate stack

Several equivalent circuits, that attempt to describe the gate stack in the presence of traps, have been proposed in literature [11]- [13]. In particular, RC distributed circuits has been proven to successfully represent C-V and G-V frequency dispersion caused by bulk oxide traps [13] [14]. This paper reports the derivation of the noise model based on this circuit representation. A step-by-step approach will be used, starting

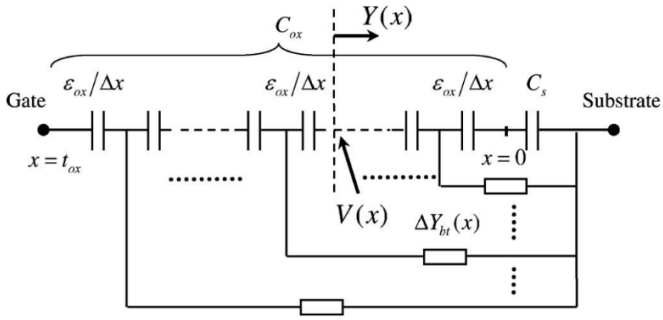

Fig. 1. Equivalent circuit for the bulk oxide traps distributed over the depth of the insulator. Figure is taken from [13]

from the analysis of a gate stack where one layer of traps of infinitesimal thickness dx is located at x. This approach puts emphasis on the position of the traps with respect the semiconductor/insulator interface and highlights the importance of an often neglected term in literature. This additional term has the effect to scale the impact of each trap on the drain/gate noise current according to its position in the oxide. In the following, a n-MOS will be considered, even though the model remains valid also for a p-MOS if the signs are taken in the appropriate way.

B. Derivation of the model for a single layer of traps

In this case, the equivalent circuit is simpler than in Fig.1, since only one RC pair is needed to represent the trap layer. This is represented by the R_{bt} - C_{bt} series shown Fig.2. The inversion capacitance is neglected, due to its large value above threshold. C_2 is the gate stack capacitance from the semiconductor/insulator interface to the trap layer and C_1 is the gate stack capacitance from the trap layer to the gate electrode.

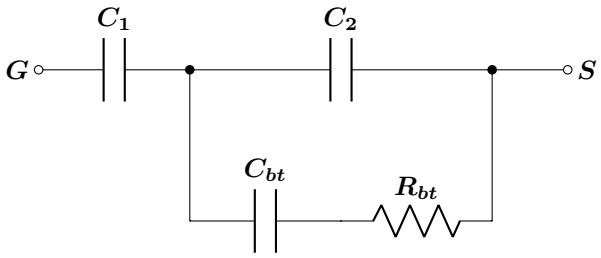

Fig. 2. Equivalent gate stack circuit with one trap layer

These components have the following expressions [12], [15]

$$\begin{aligned} C_{bt} &= \frac{q}{kT} WL\ dx \int f(1-f) N_{bt}(E)\ dE \\ R_{bt} &= \frac{\tau}{C_{bt}} \\ C_1 &= WL \frac{\epsilon_{ox}}{t_{ox} - x} \\ C_2 &= WL \frac{\epsilon_{ox}}{x} \end{aligned} \tag{1}$$

where f is the Fermi distribution function, N_{bt} is the bulk oxide trap concentration and τ is the time constant associated with charge exchange between the traps and the channel.
Firstly, we make a simplification on the circuit: we assume that, in the parallel between C_2 and the series $C_{bt} - R_{bt}$, the impedance is dominated by C_2. This is a reasonable approximation since the value of the RC series trap conductance is much smaller than the conductance associated with the gate capacitance. In this way, the circuit becomes even simpler.

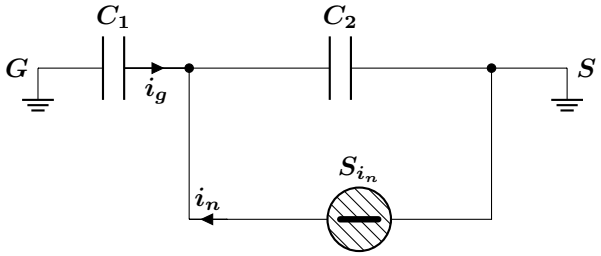

Fig. 3. Approximated gate stack circuit with one trap layer and thermal noise of R_{bt}

The noise generator S_{i_n} is obtained in the following manner: starting from the Thevenin noise representation of the R_{bt} thermal noise, the equivalent current noise generator connected at the terminals of C_2 is calculated. This generator represents the noise current flowing in the RC series. Its expression is:

$$S_{i_n} = \frac{4kTR_{bt}}{R_{bt}^2 + \frac{1}{(\omega C_{bt})^2}} = \frac{4kT}{R_{bt}} \cdot \frac{(\omega\tau)^2}{1 + (\omega\tau)^2} \tag{2}$$

A simple current partition shows that the noise current on the gate is equal to:

$$i_g = -i_n \frac{C_1}{C_1 + C_2} \tag{3}$$

It is then straightforward to obtain the power-spectral-density (PSD) of the current noise generator connected to the gate by squaring the absolute value of i_g:

$$S_{i_g} = 4qWL \cdot \frac{\omega^2\tau}{1 + (\omega\tau)^2} \cdot \left(\frac{x}{t_{ox}}\right)^2 dx \int f(1-f) N_{bt}(E)\ dE \tag{4}$$

Let's now focus on the noise current induced in the drain . The voltage noise across C_2 is equal to:

$$v_{C_2} = \frac{-i_n}{j\omega(C_1 + C_2)} \tag{5}$$

The induced noise charge in the channel is equal to:

$$Q_{ch} = v_{C_2} \cdot C_2 = \frac{-i_n\ C_2}{j\omega(C_1 + C_2)} \tag{6}$$

Applying the Shockley-Ramo theorem [16], [17] for the

MOSFET at low Vds we obtain the current induced on the drain:

$$i_d = \mu \cdot \frac{V_{ds}}{L} \cdot \frac{Q_{ch}}{L} = -i_n \cdot \frac{C_2}{C_1 + C_2} \cdot \frac{g_m}{j\omega C_{ox} W L} \tag{7}$$

Repeating the same procedure as for i_g, we find the PSD of the drain current noise:

$$S_{i_d} = \frac{4q \cdot g_m^2}{W L C_{ox}^2} \frac{\tau \cdot dx}{1 + (\omega\tau)^2} \cdot \left(\frac{t_{ox} - x}{t_{ox}}\right)^2 \int f(1-f) N_{bt}(E)\, dE \tag{8}$$

Using the Eq.3 and 7, we find that the correlation is purely imaginary:

$$C = \frac{i_g \cdot i_d^*}{\sqrt{S_{i_d} S_{i_g}}} = j \tag{9}$$

C. Extension of the model for distributed traps

In order to extend the formulas of the previous paragraph to the case of a general trap distribution along x, we have to integrate the noise spectrum along x:

$$S_{i_d} = \frac{4q \cdot g_m^2}{W L C_{ox}^2} \iint N_{bt}(E,x) \cdot \frac{f(1-f)\tau}{1 + (\omega\tau)^2} \cdot \left(\frac{t_{ox} - x}{t_{ox}}\right)^2 dE\, dx \tag{10}$$

$$S_{ig} = 4qWL\, \omega^2 \iint N_{bt}(E,x) \cdot \frac{f(1-f)\tau}{1 + (\omega\tau)^2} \cdot \left(\frac{x}{t_{ox}}\right)^2 dE\, dx \tag{11}$$

$$C = j \tag{12}$$

The cross-spectrum between the two noise spectra is:

$$i_g \cdot i_d^* = j \frac{4q \cdot g_m^2 \omega}{C_{ox}} \iint N_{bt}(E,x) \cdot \frac{f(1-f)\tau}{1 + (\omega\tau)^2} \cdot \frac{(t_{ox} - x)x}{t_{ox}^2} dE\, dx \tag{13}$$

In the approximation of large t_{ox}, the cross-spectrum expression becomes:

$$i_g \cdot i_d^* = j \frac{4q \cdot g_m^2 \omega}{C_{ox}} \iint N_{bt}(E,x) \cdot \frac{f(1-f)\tau}{1 + (\omega\tau)^2} dE\, dx \tag{14}$$

Eq.14 allows to refer the 1/f noise to the input and represent the drain noise by the means of a single noise voltage generator:

$$S_{V_g} = \frac{S_{i_d}}{g_m^2} \tag{15}$$

However, since the approximation of large t_{ox} is not verified nowadays, the presence of a single voltage noise generator is not sufficient to completely describe the 1/f noise. In general, the Eq.15 is not verified and the input referral procedure must use the Eq.13 and produce two noise generators with their correlation.

The expression obtained in this analysis for the drain noise is the same found in most literature for 1/f noise, *except the term in the brackets that depends on* x. This term modulates the spectrum of the noise generators according to the position of the trap in the oxide. If we assume that t_{ox} is very large, the noise generator S_{ig} goes to zero and the value of S_{id} becomes the one found in many papers. This approximation was reasonable when the oxide thicknesses where in the order of 200-300 nm, but it introduces huge errors with ultra thin oxides, as we will see in section IV. Furthermore, Eq.13 shows that a single noise voltage generator connected at the gate, as it is found in compact models, is not sufficient to completely describe 1/f noise.

It is worth mentioning that the trap distribution can assume any expression in the spatial and energy domain, because it is inside the double integral. Hence, this model describes 1/f noise caused by trapping events in devices operating in the linear region, no matter what the distribution of the traps is.

D. Derivation of the trapping/de-trapping time constant τ

The main parameter of the model, τ, refers to the time constant associated with charge exchange between bulk-oxide traps and channel. Its expression is directly related to the tunneling mechanism and it is often modeled with a exponential dependence on the trap position [13]

$$\tau = f\tau_0 e^{2kx} \tag{16}$$

where f is Fermi function, τ_0 is time constant associated to interface traps, k is wave number inside the potential, as defined in the WKB approximation. This time constant can be also evaluated starting from the capture and emission rates of the traps, respectively denoted by c and e, as:

$$\tau = (c + e)^{-1} \tag{17}$$

In this work we consider both elastic and phonon-assisted transitions [18]- [20], with the expressions implemented in the TCAD simulator SDevice [10], since this tool will be used later to validate our model.

$$c_{elastic} = \frac{\sqrt{8m_t} m_o^{3/2} g_c}{\hbar^4 \pi} V_T [E_C(x_0) - E_{trap}]^2 \times \sqrt{E_{trap}}\; f\left(\frac{E_F - E_{trap}}{kT}\right) \frac{|\Psi(x_0)|^2}{|\Psi(0)|^2} \tag{18}$$

$$c_{phonon} = \frac{\sqrt{m_t m_0^3 k^3 T^3} g_c}{\hbar^3 \sqrt{\chi}} V_T (S - l)^2 \times\; exp[-S(2f_B + 1) + \frac{\Delta E}{2kT} + \chi] \left(\frac{z}{l + \chi}\right)^2 \times\; F_{1/2}\left(\frac{E_F}{kT_n}\right) \frac{|\Psi(x_0)|^2}{|\Psi(0)|^2} \tag{19}$$

where:

- g_c= prefactor to Richardson's constant
- E_C= conduction band energy
- E_{trap}= energy of the trap
- m_t= tunneling mass inside the oxide
- m_0= electron mass
- k= Boltzmann constant
- $\hbar$= reduced Planck constant
- T= temperature
- f= Fermi distribution
- $F_{1/2}$= Fermi integral of order 1/2
- V_T= tunneling volume
- ψ= electron wavefunction
- l = number of phonons emitted
- f_B = Bose-Einstein distribution
- S= Huang-Rhys
- $z = 2S\sqrt{f_B(f_B+1)}$
- $\chi = \sqrt{l^2+z^2}$
- ΔE= dissipated Energy

Fig.4 indicates the reference energy and the meaning of some terms.

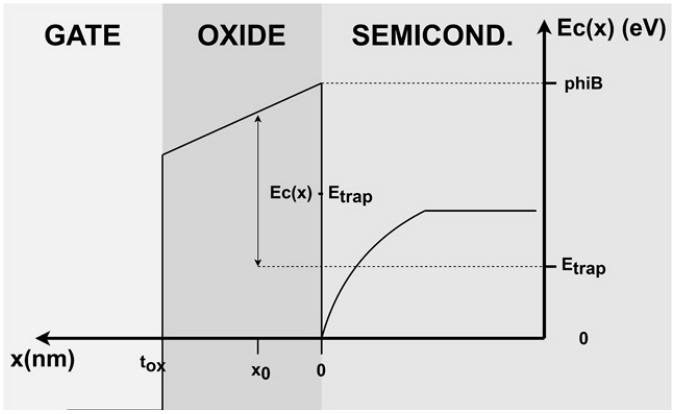

Fig. 4. Conduction band energy diagram in the MOSFET assuming a trap with energy E_{trap}

Since the two events are uncorrelated with each other, it is possible to write the total capture rate as the sum:

$$c = c_{elastic} + c_{phonon} \tag{20}$$

Exploiting the detailed balance principle, capture and emission rates can be related and the final expression for τ can be obtained:

$$\tau = \frac{f}{c} \tag{21}$$

III. Equivalence between trapping/de-trapping noise at the gate and thermal noise

One of the most interesting outcomes of the previous analysis is that we can interpret the 1/f noise as the thermal noise of an effective trap resistance caused by the traps. This observation has emerged several times in literature [21]. Here we show that this consideration can be extended in general to the input conductance of the MOSFET device.

To this purpose, starting from Fig.2, which represents the gate stack in presence of a trap layer of thickness dx located at x, we evaluate the input conductance of this circuit.
Let's denote Y_{par} the admittance of the parallel of C_2 and the trap RC series:

$$Y_{par} = \frac{j\omega(C_{bt} + C_2 + \omega^2\tau^2 C_2) + \omega^2 C_{bt}^2 R_{bt}}{1+\omega^2\tau^2} \approx j\omega C_2 + G_{bt}$$

The approximation is reasonable, since the capacitance introduced by the trap is much smaller than the oxide capacitance and the value of $\omega^2\tau^2$ is smaller than 1, even at high frequencies. The input admittance will be:

$$Y_{in} = \frac{\omega^2 C_1^2 G_{bt} + j\omega(C_1 G_{bt}^2 + \omega^2 C_1 C_2 (C_1+C_2)}{G_{bt}^2 + \omega^2 (C_1+C_2)^2}$$

The input conductance is the real part of Y_{in}:

$$g_{in} = \frac{\omega^2 C_1^2 G_{bt}}{G_{bt}^2 + \omega^2 (C_1+C_2)^2} \approx G_{bt} \cdot \left(\frac{C_1}{C_1+C_2}\right)^2 \tag{22}$$

The last approximation is justified, since even with high trap concentrations, the value of the parasitic conductance is way smaller than the conductance associated with the gate capacitance. This difference is so evident that this simplification also holds true when the value of the frequency approaches frequencies close to DC.
The equivalent thermal noise current spectral density thermal noise relative to this conductance is:

$$S_{thermal} = 4kTg_{in} = 4kTG_{bt} \cdot \left(\frac{C_1}{C_1+C_2}\right)^2 =$$

$$= 4qWL \cdot \frac{\omega^2\tau}{1+(\omega\tau)^2} \cdot \left(\frac{x}{t_{ox}}\right)^2 \cdot dx \int f(1-f) N_{bt}(E,x)\, dE \tag{23}$$

This equation is identical to the S_{i_g} we found in the previous section for a single trap layer.
If we extend this result to the case where the traps are distributed in the oxide, we obtain the general result that the trapping/de-trapping noise current through the gate terminal can be seen as thermal noise of the input conductance. Let's recall that we are considering devices operating in the linear region, hence this results derives from the fact that we can see the input port as isolated from the output port.
Furthermore, it is also possible to write an expression for the input conductance of a MOSFET in presence of traps:

$$g_{in} = \frac{qWL}{kT} \iint f(1-f) N_{bt}(E,x) \cdot \frac{\omega^2\tau}{1+(\omega\tau)^2} \cdot \left(\frac{x}{t_{ox}}\right)^2 dE\, dx \tag{24}$$

However, it is worth recalling that we are not considering the diffusion noise in this study. Thus, the derivation of this section holds true only when the 1/f noise dominates over the white noise, hence at low frequencies.

IV. Model validation by comparison with TCAD

We use TCAD simulations implementing the model for generation/recombination noise coupled with the non-local model for tunneling to and from traps [22]. These are implemented through the Sdevice tool of Sentaurus [10]. Diffusion noise will not be active in the simulations, as the main objective is to validate and analyze 1/f noise.

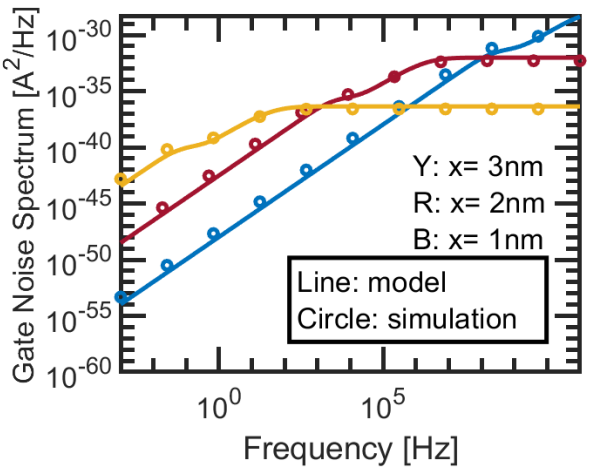

Fig. 5. Comparison between the analytical model of Eq. 11 and the TCAD simulations employing an inelastic tunneling model for a single trap layer of thickness 0.1 nm in a Si/SiO2 gate stack, using N_{BT}=1e22 $cm^{-3}eV^{-1}$, t_{ox}=5 nm, trap volume V_T=8e-9 μm^3, phonon energy=48 meV, S=10, W= 1 µm, L=0.2 µm, Vds=25 mV, Vgs=1 V

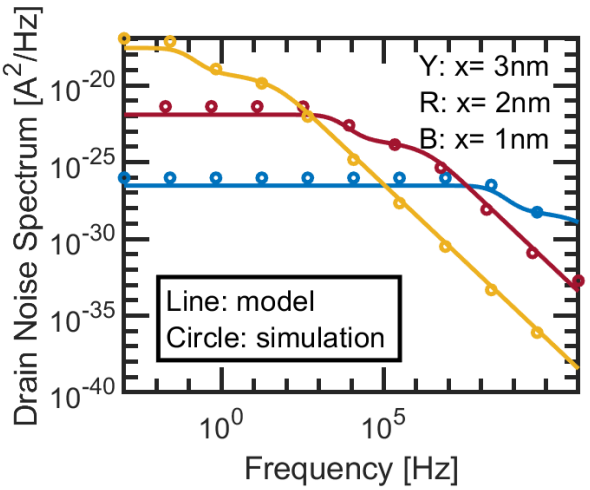

Fig. 6. Comparison between the analytical model of Eq. 10 and the TCAD simulations employing an inelastic tunneling model for a single trap layer of 0.1 nm thickness in a Si/SiO_2 gate stack, using N_{BT}=1e22 $cm^{-3}eV^{-1}$, t_{ox}=5 nm, trap volume V_T=8e-9 μm^3, phonon energy=48 meV, S=10, W= 1 µm, L=0.2 µm, Vds=25 mV, Vgs=1 V

Fig. 5 and 6 refer to a Si/SiO2 gate stack with a single trap layer of thickness 0.1 nm and different trap distance from the interface. The proposed model agrees well with the reference simulation results, showing that the proposed model correctly describes trapping/detrapping events. Furthermore, Fig 7 and 8 consider a Gaussian distribution along the oxide and different oxide thickness in a GaAs/Al2O3 gate stack. The "w/out the new term" curve refers to the model where the term $\left(1-\frac{x}{t_{ox}}\right)^2$ introduced by this paper is not present. The error increases as the oxide thickness becomes smaller, implying that an estimation error based on the commonly used and simpler formula would lead to an unacceptable error. Finally, Fig 9 compares the gate noise and the thermal noise of the input conductance, proving the calculations made in section III.

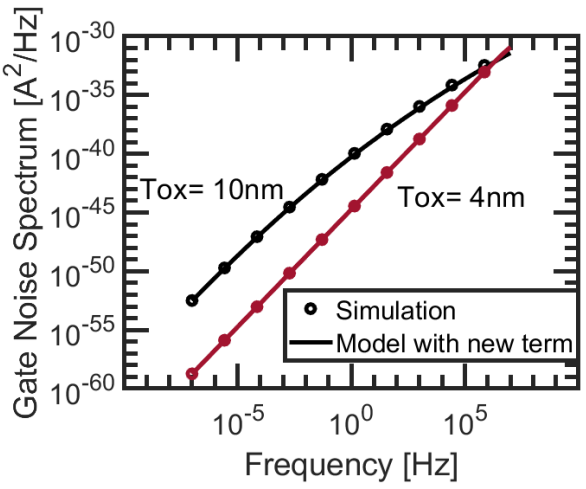

Fig. 7. Comparison between the analytical model of Eq. 11 and the TCAD simulations employing only the elastic tunneling model with a Gaussian spatial distribution of traps in a GaAs/Al_2O_3 gate stack, using N_{BT}=1e17 $cm^{-3}eV^{-1}$ with center x_0=2 nm and σ_x=1 nm, trap volume V_T=8e-9 μm^3, W= 1 µm, L=0.2 µm, Vds=25 mV, Vgs=3 V

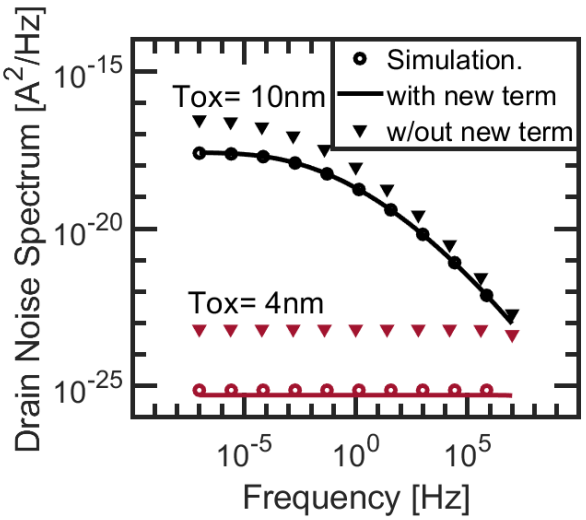

Fig. 8. Comparison between the analytical model of Eq. 10, with the new term and without the new term, and the TCAD simulations employing only the elastic tunneling model with a Gaussian spatial distribution of traps in a GaAs/Al_2O_3 gate stack, using N_{BT}=1e17 $cm^{-3}eV^{-1}$ with center x_0=2 nm and σ_x=1 nm, trap volume V_T=8e-9 μm^3, W= 1 µm, L=0.2 µm, Vds=25 mV, Vgs=3 V

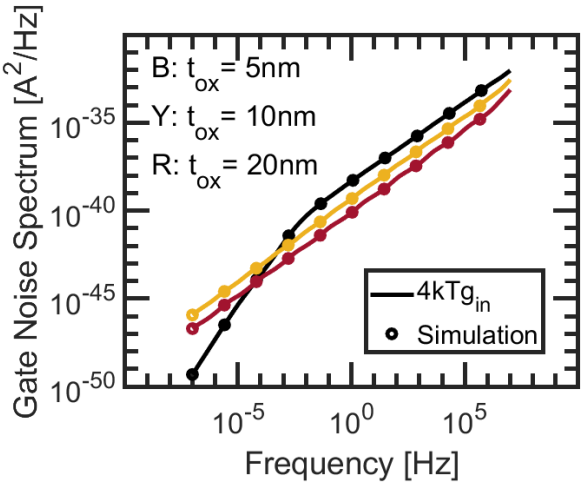

Fig. 9. Comparison between the analytical model of Eq. 23 and TCAD simulations employing only the elastic tunneling model for uniformly distributed traps in a Si/SiO_2 gate stack, using N_{BT}=1e16 $cm^{-3}eV^{-1}$, trap volume V_T=8e-9 μm^3, W= 1 µm, L=0.2 µm, Vds=25 mV, Vgs=1 V

V. Conclusions

We presented a compact way to derive the 1/f noise PSD of MOSFETs on drain and gate and their correlation, based on RC distributed circuits. We have shown that a commonly adopted approximation in noise models no longer holds for ultra-thin oxides devices. This could lead to errors whenever this formula is used to extract traps distributions from experimental samples. Finally, an alternative expression for the gate noise associated to trapping/de-trapping has been extracted, exploiting its correlation with the thermal noise of the input conductance.

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