Design of 2

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[1]Samsung Electronics

October 30, 2023

Abstract

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DesignCon

Design of 2.5D Interposer in High Bandwidth Memory and Through Silicon Via for High Speed Signal

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Abstract

The 2.5D interposer becomes a crucial solution to realize grand bandwidth of HBM for the increasing data requirement of high performance computing (HPC) and Artificial Intelligence (AI) applications. To overcome high speed switching bottleneck caused by the large resistive and capacitive characteristics of interposer, design methods to achieve an optimized performance in a limited routing area are proposed. Unlike the conventional single through silicon via (TSV), considering the reliability, multiple TSV are used as the robust 3D interconnects for each signal path. An equivalent model to accurately describe the electrical characteristics of the multiple TSVs, and a configuration pattern strategy of TSV to mitigate crosstalk are also proposed.

Author(s) Biography

Bo Pu is staff Engineer at Samsung Electronics. He is responsible for driving signal/power integrity design and analysis for chip-package-board system. He received the B.S. in electrical engineering from the Harbin Institute of Technology, China, in 2009, and combined M.S. & Ph.D. in Electrical and Electronics Engineering from Sungkyunkwan University, Korea, in 2015. His research interests include modeling, design, and analysis of chip-package-PCB systems for signal/power integrity, and electromagnetic Compatibility (EMC). Dr. Pu received the Best Student Paper Award at the IEEE APEMC in 2011 and a Young Scientists Award from the International Union of Radio Science in 2014. He served as the session chair of IEEE APEMC 2017 and TPC member of Joint IEEE EMC symposium and APEMC 2018.

Chanmin Jo received the B.S. and M.S. degrees in electrical engineering from Hanyang University, South Korea in 2004 and 2006, respectively with focus on modeling and characterization for signal integrity of integrated circuits and packaging. In 2006, he joined Samsung Electronics where he was responsible for the developing of modeling and analysis methodology for chip-package-board system.

Jun So Pak is a principal engineer at Samsung Electronics. His responsibility includes setting of system level signal integrity (SI) & power integrity (PI) analyses and advising board level SI/PI enhancement methods. He received the M.S, and Ph. D degrees in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea in 2000, and 2005. He worked as a research professor at KAIST from 2007 to 2012 and as a post doctor at AIST, Tsukuba, Japan from 2005 to 2007. He is an editor of the book, which has a title of 'Electrical Design of Through Silicon Via' and was published in 2014 from Springer. He is the author and co-author of 72 journal and conference papers.

Sungwook Moon received a Ph.D. Degree at Purdue University, West Lafayette in 2010. He has been working at Samsung Electronics as a principal engineer since July 2013. His main concern is chip-package-system co-analysis for maintaining power/signal integrity in high-power/performance applications.

Introduction

Recently, an intensive requirement of memory bandwidth for HPC (high performance computing), such as Artificial Intelligence (AI) and graphic processing unit (GPU) gets attracting since not only computation bound but also memory bandwidth bound have a significant effect on the accelerator design for machine learning [1]. The enlargement of the bandwidth can rely on the innovation of the process technology. Development in the process technology has been creating higher density in integrated circuits (ICs). However, Moore's law seems to be difficult to be driven to the next step with a proper cost in the foreseeable future. A 3D integration provides a possibility to continue enlarging the density of ICs, and more than Moore conception is getting a growing number of attentions recently. Among a large amount of more than Moore technologies, 2.5D interposer and Through Silicon Via (TSV) are playing irreplaceable significant role.

Especially, the increasing bandwidth requirement in HPC is driving a 2.5D silicon interposer to be a key solution owing to its tremendous number of fine channels and consequent great channel bandwidth. However, a design of 2.5D interposer in HBM for high speed signal transmission in a limited area is a challenge due to the bottleneck of speed caused by the high resistance and capacitance of the silicon process of interposer. The width and space of the signal traces are the key factors to influence the resistance and capacitance. Therefore, a design method to optimize the physical parameters to achieve the most appropriate electrical performance is required.

Previous publications mainly focused on the single ended memory I/O through the back end of line (BEOL) of 2.5D interposer. While for the high speed SerDes, the TSV occurs and acts as a significant role together with BEOL. Existing equivalent model to describe the electrical characteristic of TSV was established based on the convention single TSV on 1 C4 bump. However, to enhance the reliability, multiple TSV on 1 C4 bump are widely used in the real design. An equivalent model to accurately express the multiple TSV on 1 C4 bump is also needed as a design guide for the high speed signal propagation in the 3D interconnects.

In this paper, design methods of 2.5D interposer channel for HBM are proposed in section II with the consideration of SI performance affected by both signal and ground routing designs. Optimized width and space for signal traces and novel defected ground pattern (void pattern on ground layer) to achieve a good performance on high speed signal transmissions are summarized in the conclusion. Equivalent model to accurately describe the electrical characteristic of not conventional TSV array with double TSV in single C4 bump is first introduced in section III. A design strategy of the TSV pattern with considering both crosstalk and area is also discussed in the section, and the recommended case is finally concluded.

1. Physical Configuration of 2.5D Si-Interposer

The interposer acts as the platform for the transition of signal or power between TSV and micro bump. In our design, there are four layers which are metal 1 (M1) to metal 4 (M4) from bottom to top in the structure of interposer. As the cross section view of interposer

shown in Fig. 2, there are coupled microstrip lines at M4 layer and coupled strip line at M2 layer with thickness of t_1 μm for signal propagation. The length of microstrip line and stripline are around 4~5 mm, respectively.

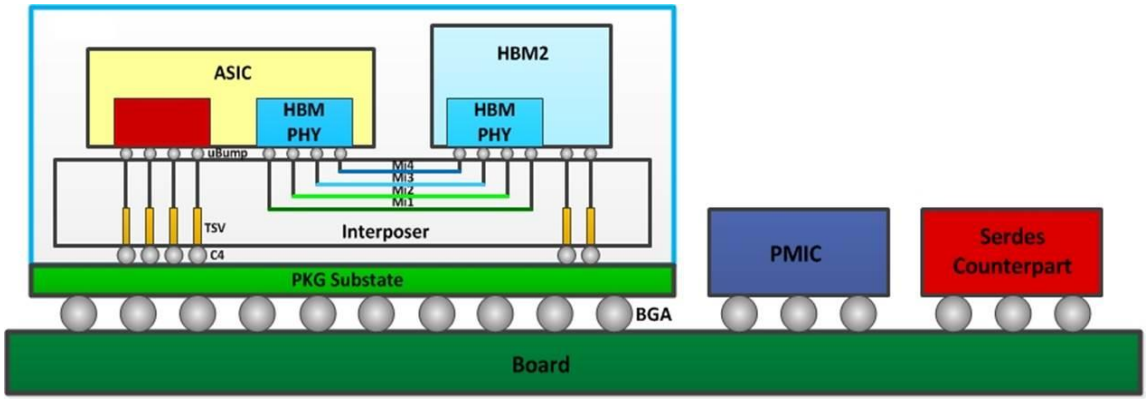


Fig. 1. A conceptual structure of 2.5 interposer for high speed parallel signals in HBM and TSV for high speed serial signals.

The signal lines are fabricated based on the Cu damascene process technology in the foundry back-end-of-line (BEOL) manufacturing process. The return path of the signal line can be the solid or mesh type ground layer below the signal layer or additional adjacent coplanar ground trace at the same layer. Insulation layer as SiO2 filling the space between signal and ground is necessary to provide insulation between two vertical metallic layers, and the thickness of insulation layer is t_2 μm. In traditional interposer of HBM, there is S-S-S-S type, where S represents signal line, in signal layer. To mitigate the crosstalk between signal lines, additional adjacent ground traces are added to form a G-S-G-S-G type, and here G is the ground line acting as the shielding wall. The merit of implementing the adjacent return path in the same layer will be demonstrate based on eye and jitter in the following section.

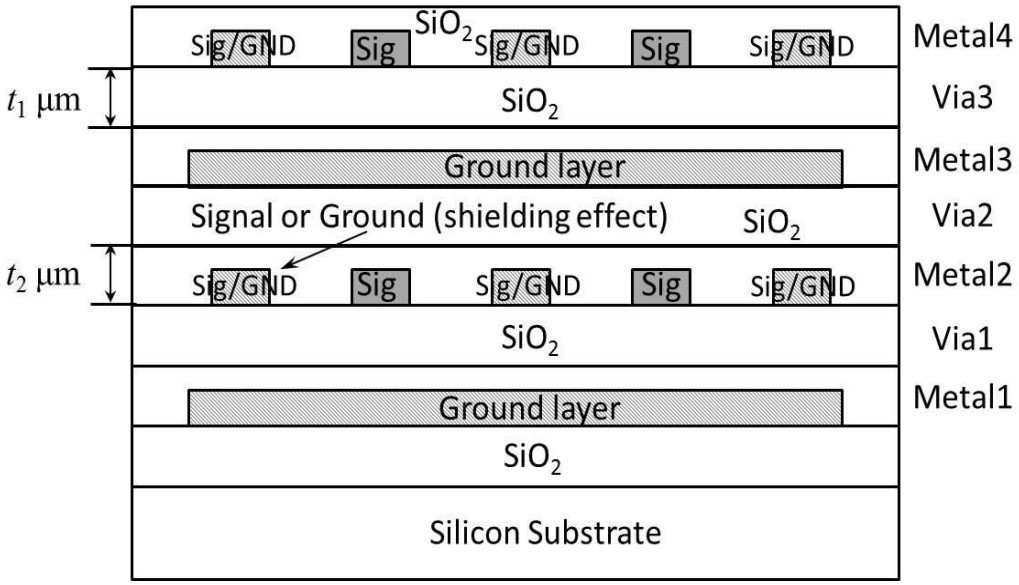


Fig 2. Physical configuration of proposed 2.5D interposer for HBM [3].

2. Design of the 2.5D Si-interposer for HBM

2.1 Design of the Signal Traces with Optimization

The width and space of the traces for signal are the main variables in the design of interposer since the thickness of the line is pre-defined based on the stack up option. Resistance, self-inductance, self-capacitance and mutual couplings exist in the signal traces. Increasing the width of trace and keeping the other geometric parameters, resistance definitely goes down and capacitance gives a rising value. Since eye diagram depends on both resistance and capacitance, a simple single direction trend for eye quality is not easy to be obtained. Diverse designs and corresponding analysis are required.

To predict the eye quality of the signal traces with diverse widths, channel simulation in time domain defined in [1] as shown in Fig. 3 is performed with voltage swing of 1.2V, maximum driver current of 18mA for I/O in transceiver, and only a capacitor of 0.4 pF as the maximum termination of receiver since no resistor termination is used here due to power consumption issue. Stimulus with worst random pattern we made is applied as the input signal in the channel simulation of HBM interposer.

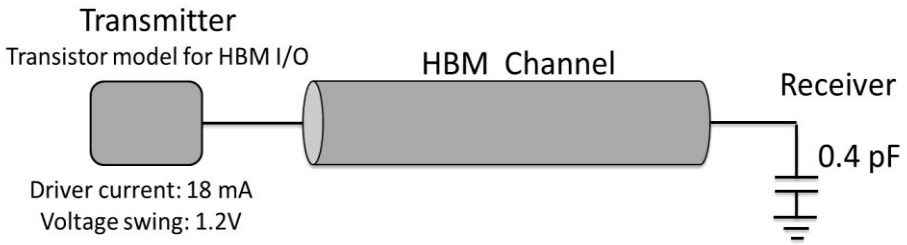


Fig 3. Embodiment of the channel simulation for HBM interposer.

Eye height and jitter are the most common criteria to judge the performance of channel, and they are calculated by the eye mask defined in the specification of HBM [1]. To describe the eye height and jitter, two eye diagrams with traces of 6 mm and 9 mm, which are longer than our real interposer but can give a clear comparison on the change of eye height and jitter, are illustrated in Fig 3.

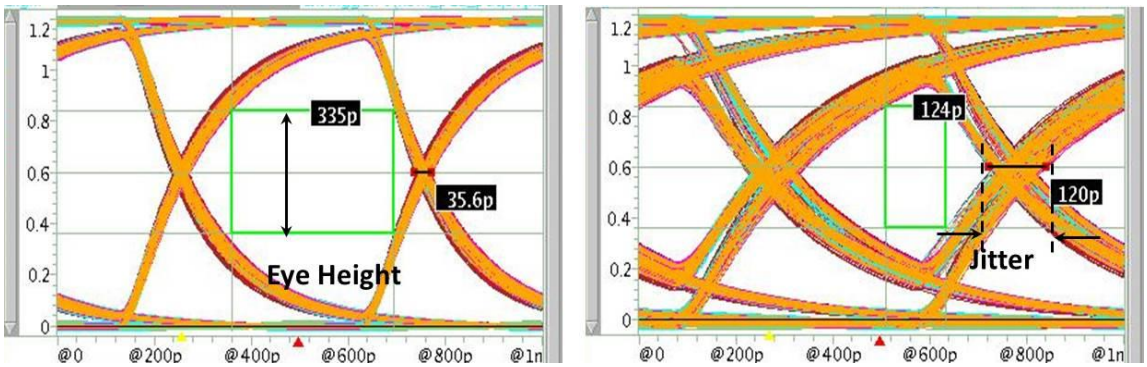
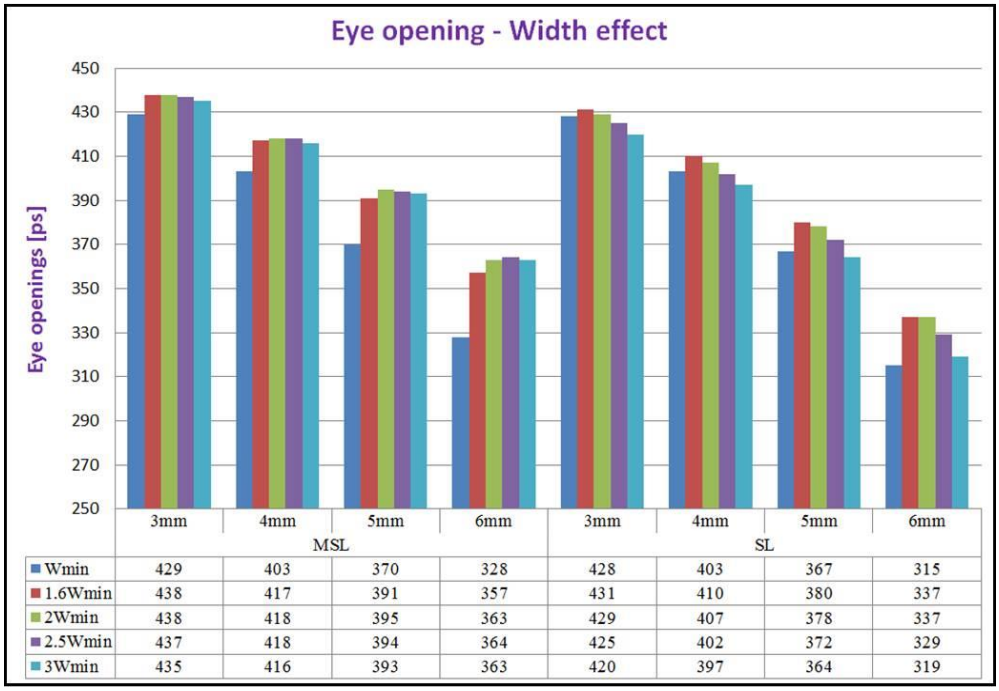


Fig 4 .Eye diagram of traces in interposer with random length of 6 mm and 9 mm for a demonstration.

To figure out the effect of width to the signal integrity of interposer, we designed a Ground-Signal-Ground-Signal (GSGS) structure to mitigate the inductive and capacitive couplings between adjacent signal traces, and only remain the change happened on the trace itself. The widths of the signal and ground traces in the same layer vary from minimum available width by process as w_{min} to $3w_{min}$ which are considered as the appropriate range for width of interposer. Discrete values as $1.6w_{min}$, $2w_{min}$, and $2.5w_{min}$ between w_{min} and $3w_{min}$ are chosen in the intermediate range. The space between ground and signal traces in the same layer and the width of ground trace is fixed as w_{min}. Entire ground planes in M1 and M3 are located below the signal and adjacent ground traces. The effect of width on the eye opening and jitter for GSGS structure with diverse length from 3 mm to 6 mm are shown in Fig. 5 and Fig. 6. The MSL and SL in the figures represent the microstrip line in M4 and stripline in M2 layer.

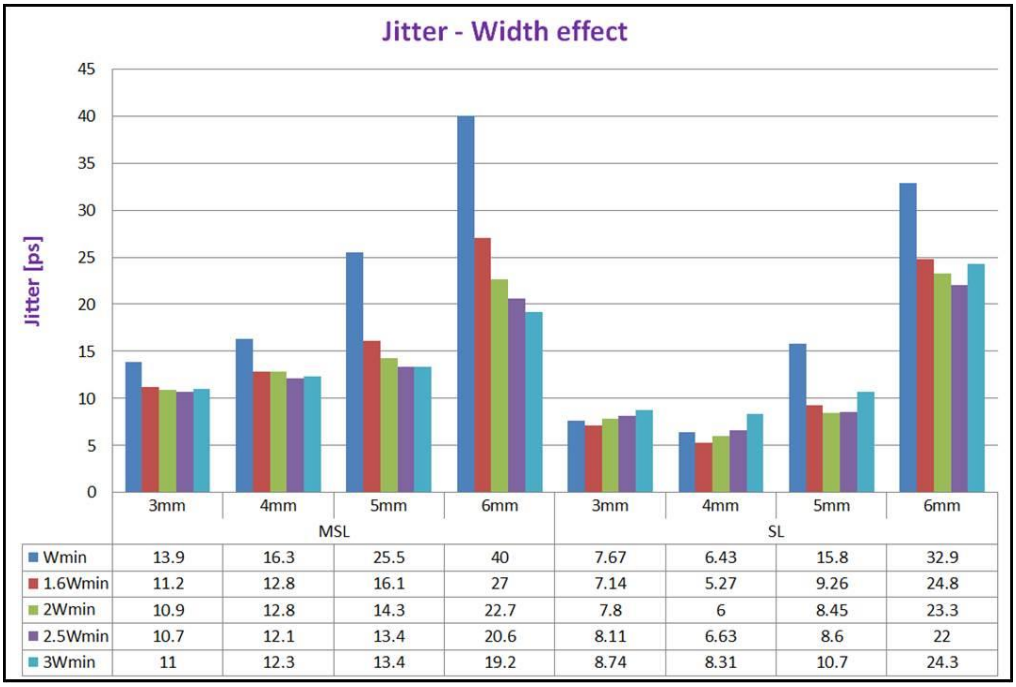


	MSL				SL			
	3mm	4mm	5mm	6mm	3mm	4mm	5mm	6mm
Wmin	429	403	370	328	428	403	367	315
1.6Wmin	438	417	391	357	431	410	380	337
2Wmin	438	418	395	363	429	407	378	337
2.5Wmin	437	418	394	364	425	402	372	329
3Wmin	435	416	393	363	420	397	364	319

Fig 5. Effect of width on the eye height for the GSGS structure.

Usually, the channel bandwidth depends on the total resistance and capacitance, and the resistance and capacitance of interposer are influence by width. Resistance dominates when a line of interposer has a narrow width. Increasing the narrow width can decrease the resistance and still has not obvious change on capacitance. Therefore, in microstrip line type, bandwidth keeps increasing until reaching the width of $3w_{min}$. Capacitance becomes dominant when the width goes over $3w_{min}$, thus a rising on the width will cause a falling on the bandwidth. Since strip lines has both upper and lower capacitance, the total capacitance cannot be ignored even it is a narrow line under $3w_{min}$. A significant reduction on the channel bandwidth is observed as in Fig. 6 with an increase on the width of strip line from w_{min} to $3w_{min}$. With reference to the obtained results of eye opening and jitter, appropriate width for the required length of interposer is able to be determined. The optimized best widths for largest height of eye mask and least jitter are difference, decision of width should be made based on the real eye mask and eye diagram. The jitter

variation affects the eye quality more in the left of Fig 4, and change of height contributes larger to the entire performance of eye diagram in the right of Fig 4.



	MSL				SL			
Wmin	13.9	16.3	25.5	40	7.67	6.43	15.8	32.9
1.6Wmin	11.2	12.8	16.1	27	7.14	5.27	9.26	24.8
2Wmin	10.9	12.8	14.3	22.7	7.8	6	8.45	23.3
2.5Wmin	10.7	12.1	13.4	20.6	8.11	6.63	8.6	22
3Wmin	11	12.3	13.4	19.2	8.74	8.31	10.7	24.3

Fig 6. Effect of width on the eye height for the GSGS structure.

Table I. Comparison of jitter and eye width on microstrip and strip lines for different trace width.

GSGS Type	Criteria	w_{min} (Min. Width)	1.6 * w_{min}	Difference Ratio
Strip Line in Mi2 layer	Jitter (ps)	32.9	24.8	32.7%
	Eye Width (ps)	315	337	6.6%
Mircostrip Line in Mi4 layer	Jitter (ps)	40	27	48%
	Eye Width (ps)	328	357	8.1%

The effect of two different trace widths (w_{min} defined in specific process and $1.6w_{min}$) on the eye width and jitter for the signal line with the same length is listed in Table I. The change on the width of signal trace obviously affects the electrical performance significantly, and the most appropriate value of width for the specific design is able to be determined based on the procedure of our design method.

Adjacent ground traces for signal traces in the same layer is supposed to act as the shielding wall to attenuate the unnecessary couplings between two nearby signal traces, and thus to enhance the signal integrity of interposer. However, implementation of additional ground traces between signal traces at the same layer will inevitably enlarge the area of interposer for fixed number of signal lines, and results in an increase on the cost of fabrication. To get a balance between area and using of additional ground traces, we designed Signal-Signal-Signal-Signal (SSSS) structure to discuss when the adjacent ground traces is required to mitigate the couplings.

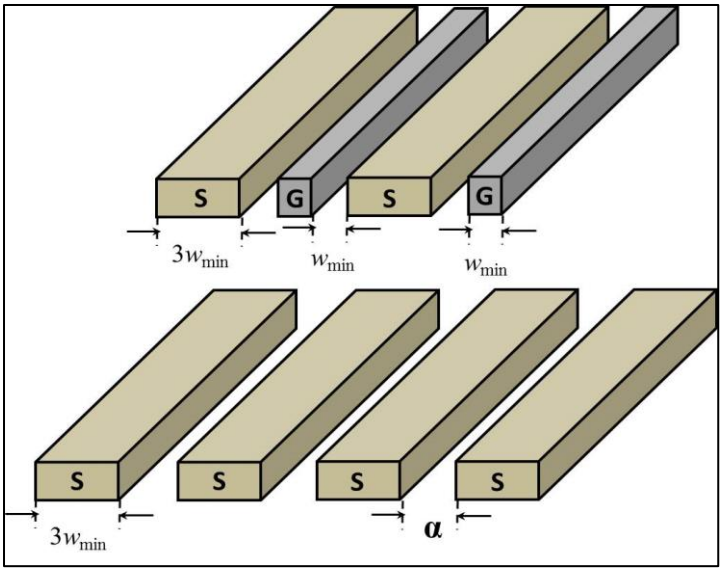
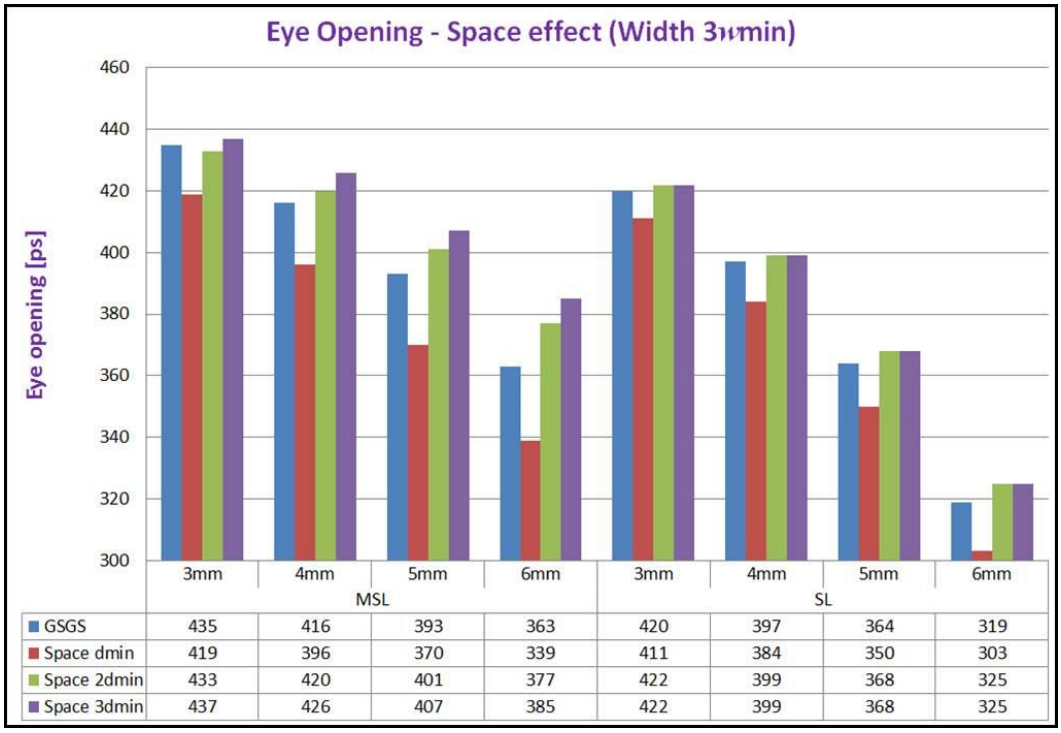


Fig 7. Geometric parameters for the GSGS and SSSS type interposers.

Designed two types are shown in Fig. 7. All the signal traces in both GSGS and SSSS structures are designed with fixed width of $3w_{min}$, and width of ground traces also keeps with w_{min} which is the same in the study of width effect above. The space of the SSSS changes from minimum available distance as d_{min} to $3d_{min}$ with an interval as d_{min}.



	3mm	4mm	5mm	6mm	3mm	4mm	5mm	6mm
	MSL				SL			
GSGS	435	416	393	363	420	397	364	319
Space dmin	419	396	370	339	411	384	350	303
Space 2dmin	433	420	401	377	422	399	368	325
Space 3dmin	437	426	407	385	422	399	368	325

Fig 8. Effect of space on the eye opening for the SSSS structure.

	MSL				SL			
GSGS	11	12.3	13.4	19.2	8.74	8.31	10.7	24.3
Space dmin	29.2	35.2	40	47.1	17.9	19.6	25.1	39.2
Space 2dmin	15.1	16.3	17.6	20.6	8.4	7.48	10.7	22.5
Space 3dmin	10.9	10.8	11.3	13.1	8.46	7.41	9.74	23.1

Fig 9. Effect of space on the jitter for the SSSS structure.

Larger eye opening and less jitter could be achieved with an increasing on the space of microstrip lines in SSSS structure since the mutual inductive and capacitive couplings weaken by a longer distance. A similar phenomenon is observed for strip lines in SSSS case but there is not an obvious difference for those criteria in space of $2d_{\min}$ and $3d_{\min}$. The different trends on miscrostrip line and strip line can be explained by the diverse fringing capacitances happened in the two structures. Fringing capacitances in strip line takes more couplings from the two nearby signal traces because there are both ground layers above and below the strip lines. Thus, the coupling between two signals does not change easily after space of $2d_{\min}$ for strip lines.

As we mentioned in the previous content, the add-in ground traces in the same layer of signal lines need to be consider from both the cost and effect of shielding. In the GSGS structure, the horizontal distance between two most closed signal lines is $3d_{\min}$. Compare the GSGS to the SSSS structure with the same gap of $3d_{\min}$, both the eye opening and jitter do not give a big difference. We can make a decision that it is not necessary to bring the additional ground traces for shielding the signals in the same layer once the distance of signals goes over 3 μm, and this would avoid the cost of ground traces.

2.1 Design of the Ground Pattern with Optimization

With reference to the insertion loss of interposer, the magnitude and phase for both microstrip line and strip line are plotted in Fig. 9. The slopes of the loss less than 1GHz for them are similar since the loss is dominated by DC conductance loss, and both the two lines have the same width. As frequency goes higher and over 1GHz, we can observe a larger slope for strip line than microstrip line from magnitude, and obtain a more added

capacitance from the phase. The reason is the strip line generate more capacitive coupling even with a same width as microstrip line, and the loss in high frequency range depends on the parasitic inductance and capacitance. Capacitance caused by the additional ground in strip line seems to be a demerit to the insertion loss and eye diagram.

Before taking an approach to weaken the unnecessary ground effect on microstrip line, a measurement is taken to validate the simulation result, especially the phase which can accurately offer the information of capacitive coupling. Test pattern of both microstrip lines only for probing are designed and fabricated. Here we only demonstrate the correlation for the microstrip line because via connecting strip line and pad on top would cause additional effect to diminish the accuracy of line itself. Four miscrostrip lines are simulated to decrease the uncertainty from meshing or convergence issues in 3D full wave simulator and one of them is chosen for measurement. As shown in Fig. 10, the correlation of phase for simulation and measurement performs well and validate the ground effect on capacitive couplings as we mentioned above.

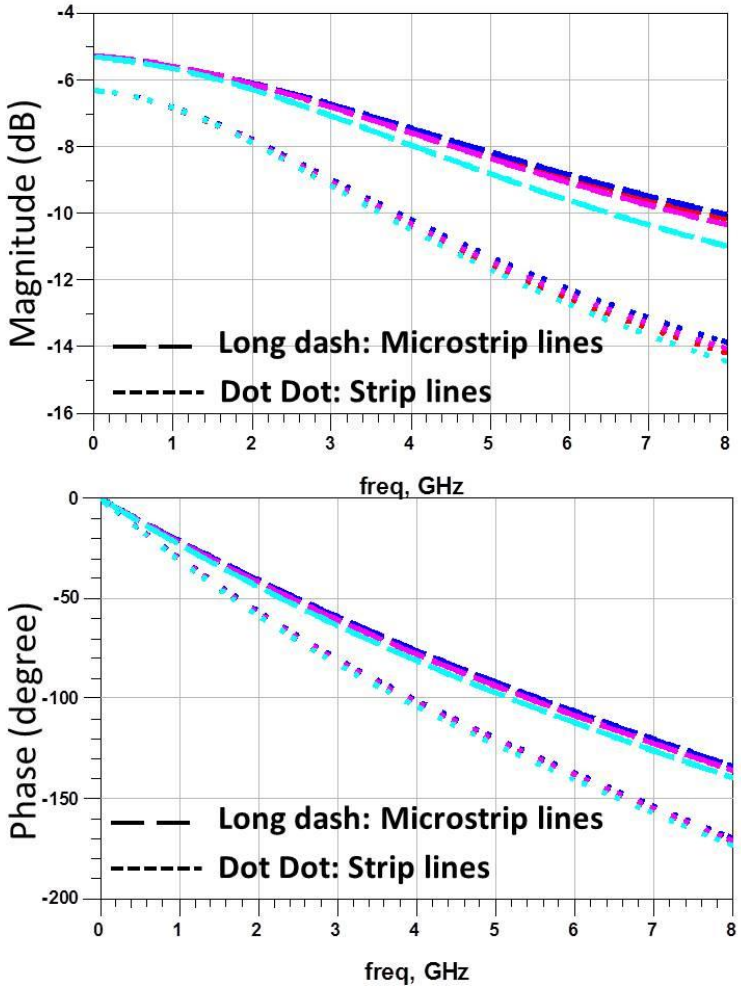


Fig 10. Insertion loss of microstrip lines and strip lines in interposer extracted by 3D full wave simulator

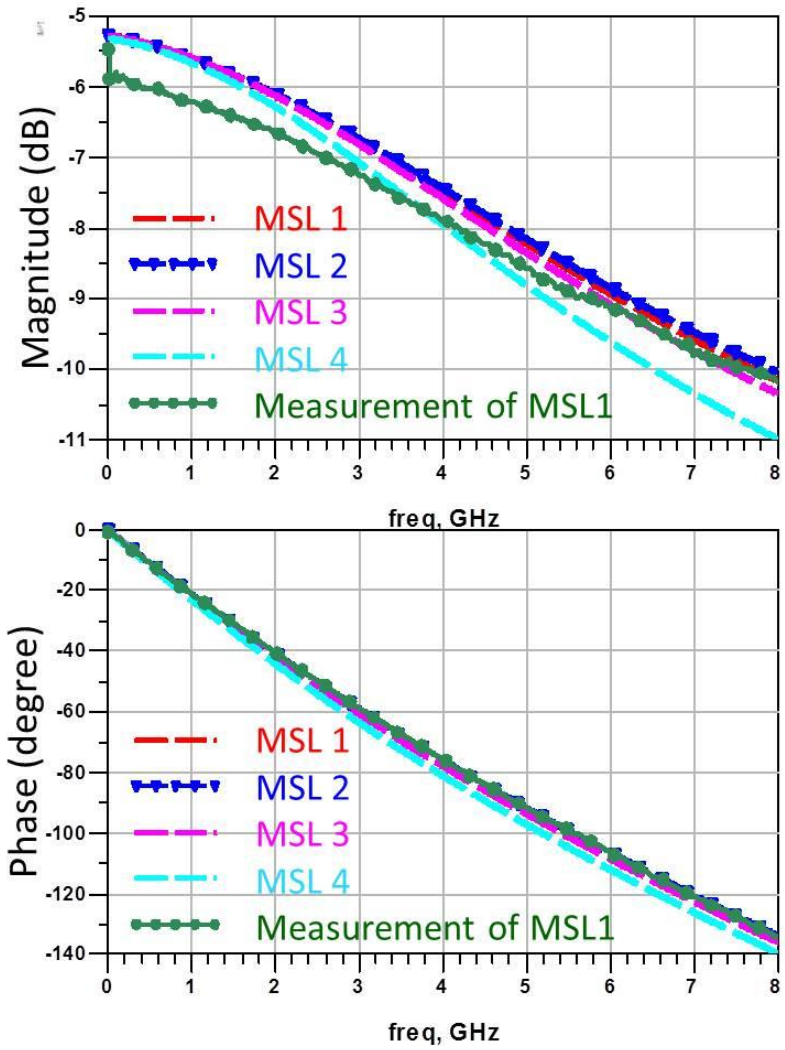


Fig 11. Validation of the result extracted by 3D full wave simulator by measurement.

In the interposer, two types of transmission line exist and they are microstrip line in M4 layer and stripline in M2 layer. With the same width and space for those two kinds of lines, stripline offers a larger capacitance and it inevitably deteriorates the quality of signal propagation by increasing the rising time of signal. To avoid the unnecessary or decrease the excessive capacitive couplings, a design strategy of the ground pattern will be discussed in the following content.

In the normal design of interposer, considering a reduction of cost, grid-type ground lines are used to instead of the entire ground plane as depicted in Fig. 11. The ground lines locate just above or below the signal lines to provide return paths. However, comparing to microstrip lines, strip lines contain excessive capacitive couplings from ground lines at two sides, and have a worse performance of the eye diagram.

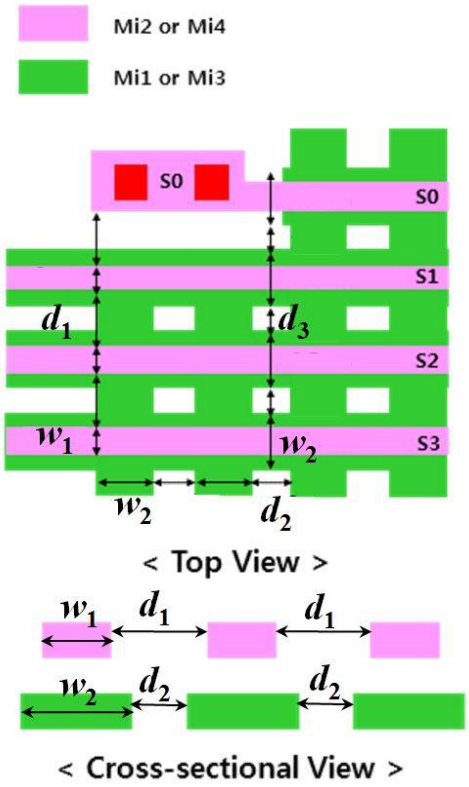


Fig. 12. Traditional grid-type ground pattern in 2.5D interposer of HBM.

An alternative grid-type ground pattern is presented by horizontally shifting the traditional one to generate the defected ground structure above or below the signal lines as shown in Fig. 12. The defected ground may reduce the area of the return path, but the fringing effect could offer an enough return path for current signal since the data rate of the 2.5D interposer still remains less than 3Gbps per channel.

Channel simulation for 2.5D interposer based on the traditional and presented ground pattern were taken and a comparison for them is illustrated in Fig. 13. The change on the ground pattern does not obviously affect the microstrip line, and it validated that the presented ground pattern is still able to provide an enough capability for return path of signal. With reference to the stripline, eye width and jitter got enhanced with the presented pattern to the traditional one. The eye width and jitter are 414 ps and 9.52 ps in traditional pattern but improved to 429 ps and 9.39 ps in the presented one, respectively. The presented way does not required additional process and area, and it could be realized by a not complicate modification on the basis of tradition ground design.

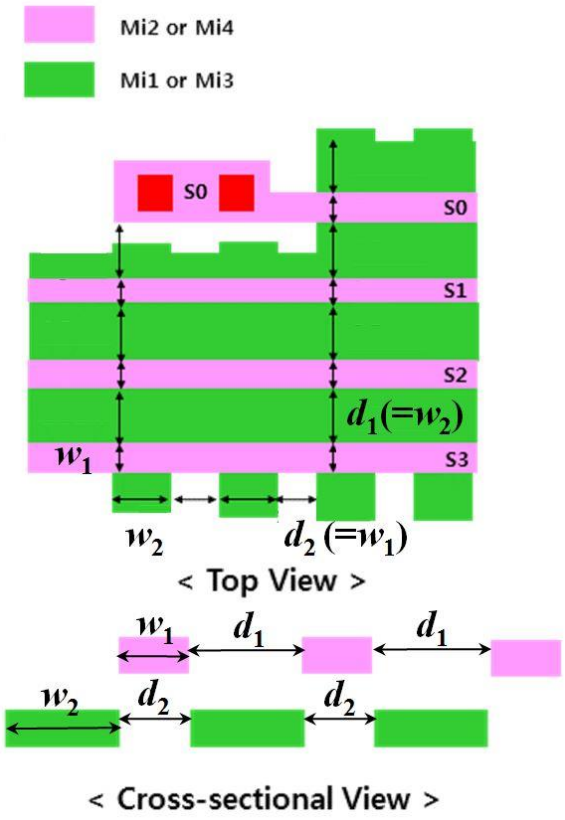


Fig. 13. The proposed grid-type ground pattern in 2.5D interposer of HBM to enhance the quality of signal propagation.

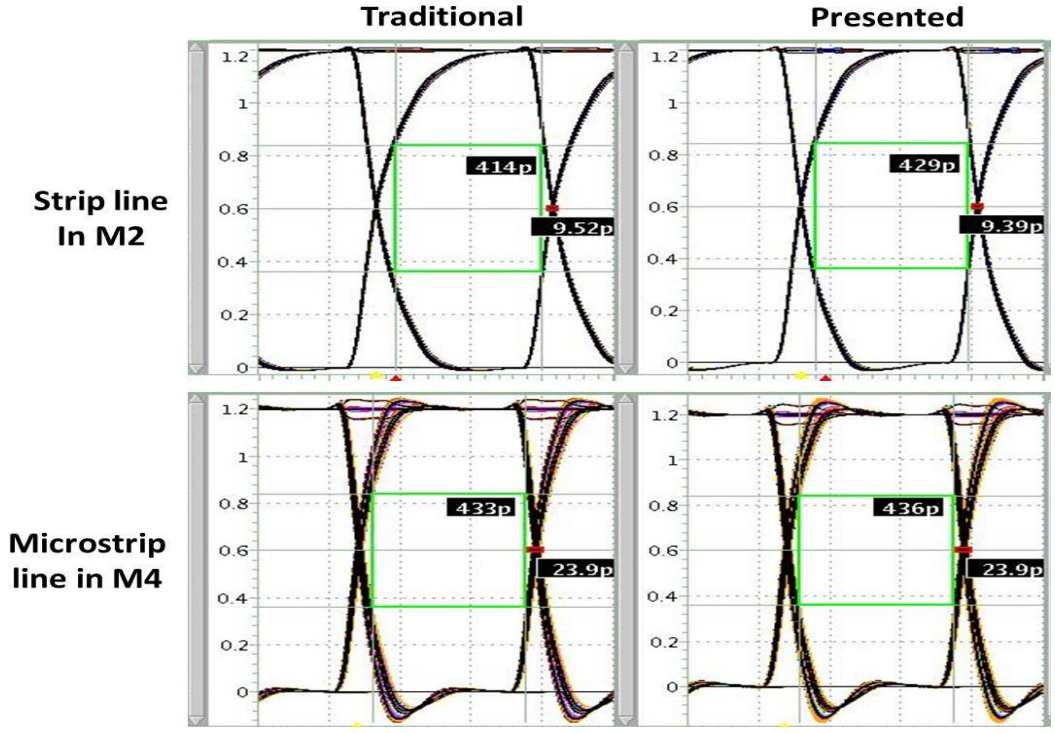


Fig. 14. Eye diagram of stripline and microstrip line with traditional or presented ground patterns.

3. Design of the TSV for High Speed Signals

3.1 Equivalent model for the GSSG and Duo-Coaxial structures with 2 TSV on each C4 bump

Through Silicon Via (TSV) makes a 3D integration be possible by its characteristic of vertical interconnection. Existing publications well demonstrated the equivalent modeling of signal TSV on each C4 bump. However, due to the tiny size of TSV and weakness of process technology, single TSV of each bump cannot provide a robust connection in the vertical direction. In the real application, multiple TSV in each bump is used instead to guarantee the reliability. Here we proposed an equivalent circuit for the duo-coaxial TSV, where there are multiple TSV in each bump, for differential high speed signal propagation.

A typical structure of the GSSG type differential array with double TSV on each C4 bump is depicted in Fig. 15. Two signal TSV pairs for differential signal propagation are located in the center, and corresponding ground TSV pair generates the return path at left and right sides of differential signal pairs.

The length and diameter of TSV are denoted as h_{TSV} and d_{TSV}. An insulator such as silicon dioxide (SiO2) layer with thickness t_{ox} surrounds the TSV and establishes a keep out zone between metal and the semiconductor (Si substrate) to block the DC leakage current. Center to center pitch of two TSV and two C4 bump are indicated as p_{center} and p_{C4}, respectively.

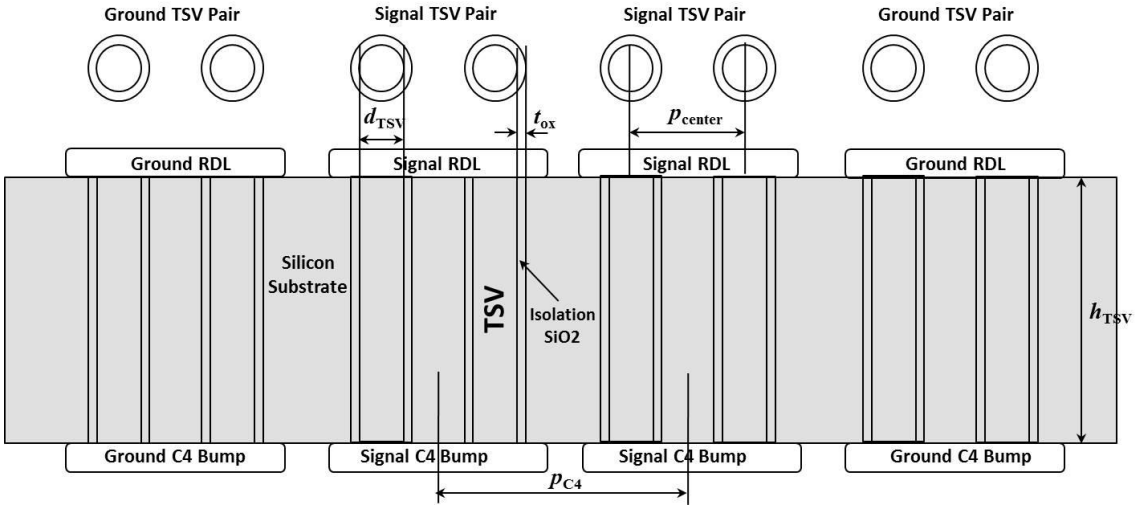


Fig. 15. The configuration of a GSSG type array with double TSV on each C4 bump.

TSV barrel has its own resistance R_{TSV} and inductance L_{TSV}, and capacitive coupling also exists between TSV pairs. The capacitive couplings between TSV can be divided into two stages. One of them is the capacitance C_{ox} by silicon dioxide between barrel and silicon substrate, and the other is the capacitive coupling C_{si_sub} happened in the silicon substrate. Conductance G_{si_sub} also has effect in the silicon substrate and it is parallel with C_{si_sub}. Not only self-inductance L_{self} of each TSV, mutual inductive coupling L_m interacts

between adjacent TSV pairs to form a loop inductance with L_{self}. Once the electrical characteristic is figured out, the equivalent circuit of the GSSG TSV array with double TSV on each C4 bump is able to be established and shown in Fig. 16. Electrical parameters are derived considering the physical dimension and material by the equations mentioned in [5].

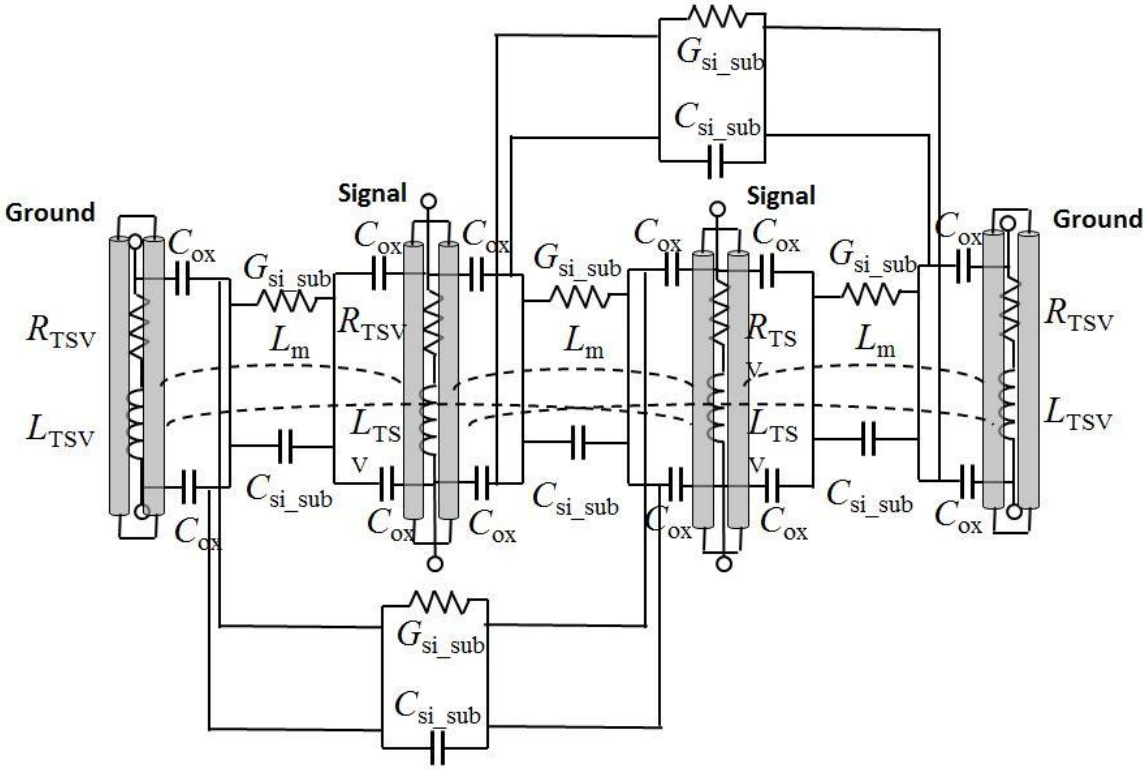


Fig. 16. The equivalent circuit of a GSSG type array with double TSV on each C4 bump.

To validate the accuracy of the proposed equivalent circuit, a 3D model based on the commercial full-wave tool is created as shown in Fig. 17. The port assignment requires a PEC to combine all ground via to provide a return path. However, the added-in PEC area inevitably bring into an excessive effect on the accuracy of TSV modeling. Narrow and wide PEC areas are both made and the comparison between results from equivalent circuit and full-wave model is shown in Fig. 18. A very good agreement for both magnitude and phase can be achieved up to 50GHz, and it is enough to cover most of the current high speed interfaces.

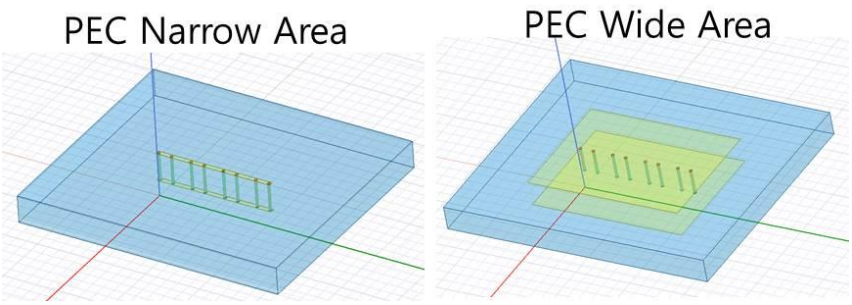


Fig. 17. 3D full-wave model for the GSSG TSV array with narrow and wide PEC area for port assignment.

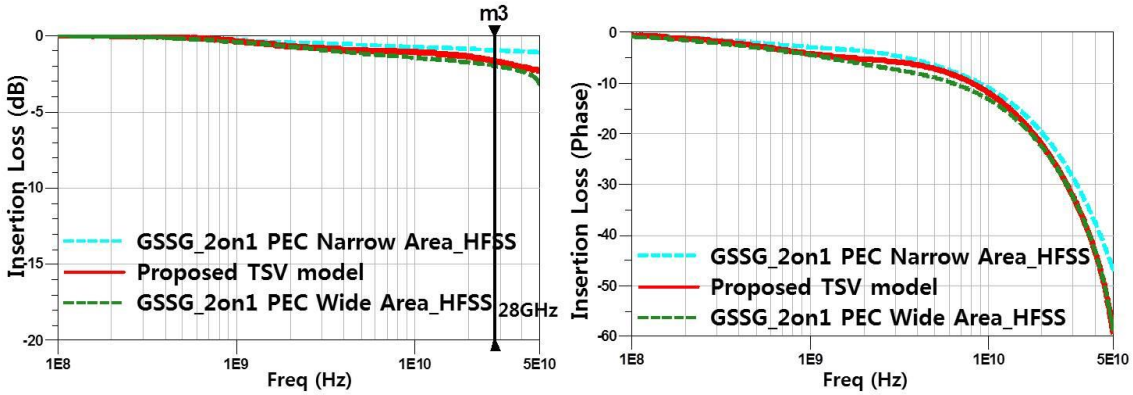


Fig. 18. Comparison of results between full-wave simulator and proposes equivalent circuit for GSSG.

TSV pairs are located in a miniature area, and the pitch of TSV usually varies from tens of micrometer (um) to hundreds of micrometer (um). Couplings between adjacent high speed signals on TSV are much more severe than the vias on the board level. To mitigate the crosstalk among TSV pairs, ground TSV are demanded to be assigned around the signal TSV to provide a fence for shielding. Therefore, we introduce a duo-coaxial structure with 2 TSV on each C4 bump and propose the equivalent circuit for it with a top view as shown in Fig. 19. In the duo-coaxial TSV array, ground pairs surrounded the differential signal TSV pairs, and offer an effective return paths and shielding fence for crosstalk mitigation. Since the narrow and wide PEC should include the area of all signal and ground TSV in the duo-coaxial structure, the center located signal TSV pairs are fully covered by narrow or wide PEC. Thus, the effect of PEC for the port assignment is negligible as shown in Fig. 20. The accuracy of proposed equivalent circuit for duo-coaxial TSV array is also got ensured as illustrated in Fig. 20 by the comparison between full-wave simulation and equivalent model.

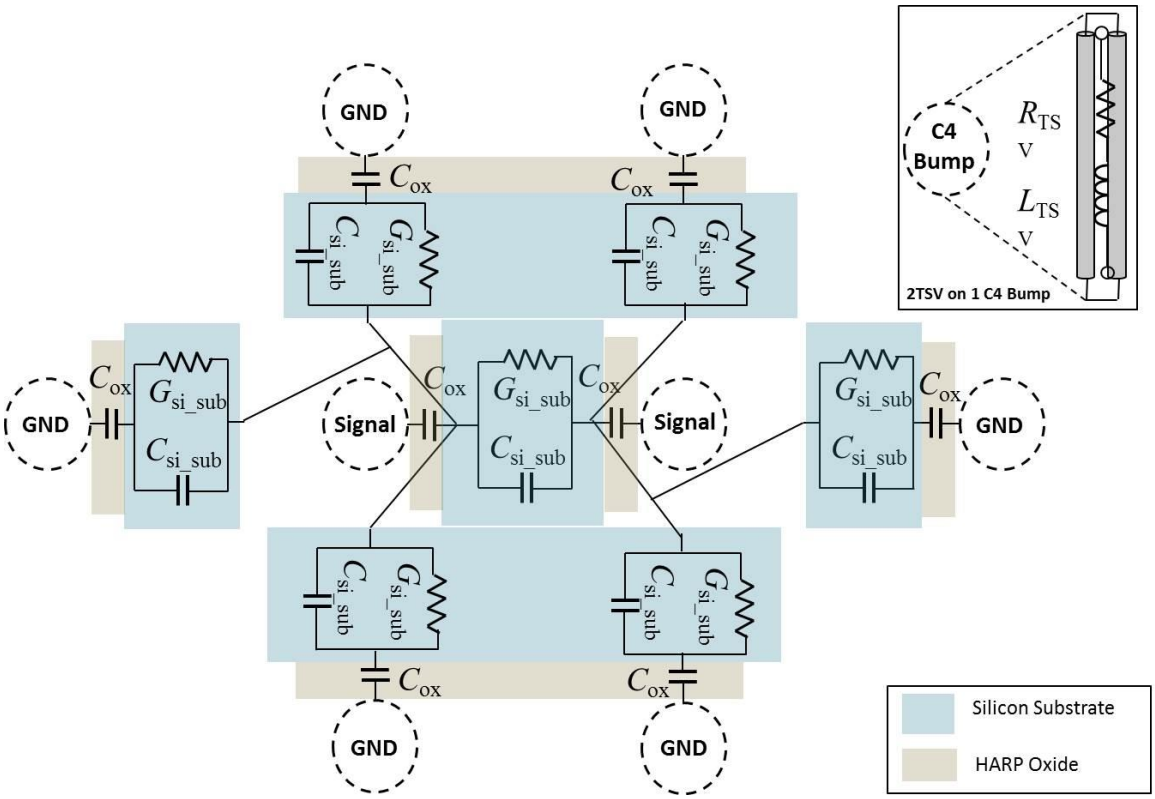


Fig. 19. A top view of the proposed duo-coaxial structure with 2 TSV on each C4 bump to mitigate the crosstalk between signal pairs.

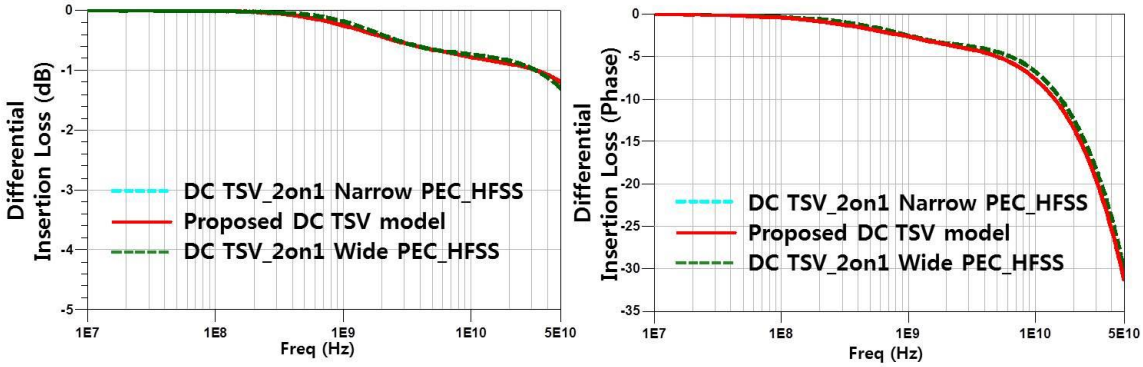


Fig. 20. Comparison of results between full-wave simulator and proposes equivalent circuit for duo-coaxial TSV array.

The magnitude and phase of our proposed model agree with the full-wave simulation up to 50GHz which can cover most of the existing high speed signals. Based on the validated equivalent model, analysis of SI and PI becomes convenient comparing to the time costing 3D full wave simulation.

3.2 Design and optimization of TSV for a Demanded Electrical Characteristics

Although the modeling of TSV array based on the existing design is able to provide an accurate electrical characteristic and corresponding performance, the design method and

optimization strategy in the design stage seems to be more important to generate TSV with demanded loss. In this section, we will discuss the effect of TSV physical parameters on the electrical characteristic to conclude a design guide of the TSV for a required insertion loss.

As describe in Fig. 19, five parameters, which are R_{TSV}, C_{ox}, C_{si_sub}, total loop inductance L_{loop}, and conductance G in silicon substrate, affect the electrical characteristic of the TSV. Among them, the later four factors have influence on the AC response of the TSV. In order to understand the parameter effect on the differential insertion loss regarding frequency, we make use of proposed equivalent model and studied 5 cases. One of them is the case with original 4 factors mentioned above, and others are the case with changing 1 factor each time.

The result is shown in Fig. 21, and we can find that the C_{ox} dominates the mid frequency range, which is from 100M to 1GHz for this duo coaxial model, parameters happened in the silicon substrate, which are C_{si_sub} and G, mainly cover the high frequency from 1G Hz to 10GHz. Over 10GHz, inductance L becomes the premier effect on the insertion loss. Usually, higher inductance causes larger impedance and results in more losses. However, the inductance occurred in the TSV can contribute to the impedance of termination and enhance the bandwidth over a wide frequency range. Therefore, it can improve the performance regarding to the insertion loss. It works as an inductive picking function to compensate the capacitive coupling from silicon oxide and silicon substrate as what T-coil works.

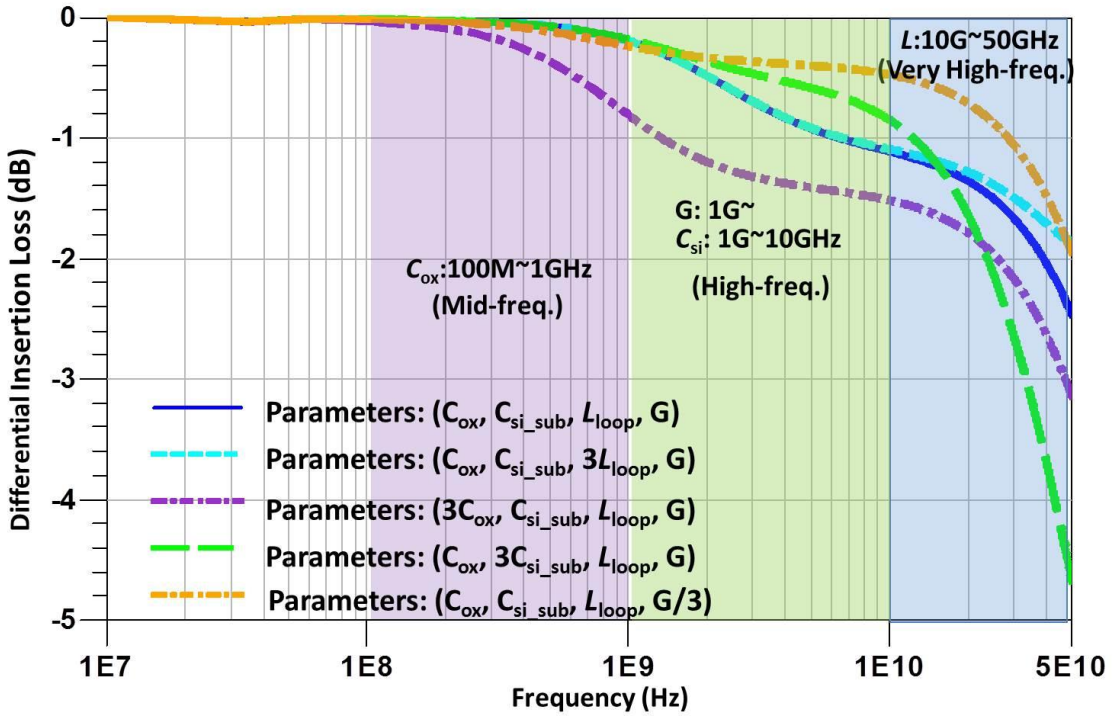


Fig. 21. Parameters effect on the insertion loss regarding frequency range.

Once understanding the relationship between those parameters and their dominating frequency range, a design guide to achieve required electrical performance is able to be established. As mentioned in the previous sections, the parameters in the equivalent circuits depend on the physical geometric dimensions. Usually, the diameter, height of TSV, and the thickness of SiO2 are defined by the process technology where the TSV is implemented. The controllable main factors only remain as pitch of C4 bump, and silicon conductivity. In our present model with double TSV on each C4 bump, the pitch of TSV on one C4 bump would also be an adjustable parameter. Cases with variable pitch of TSV on single C4 bump, pitch between C4 Bump, and silicon conductivity are studied, and a guide to achieve less insertion loss, in other words, better signal integrity, is illustrated in Fig. 22 to Fig. 24.

It is obviously to conclude that a less insertion loss rely on the smaller pitch of double TSV on each C4 bump, larger pitch between C4 bump and less silicon conductivity. The smaller pitch of double TSV on single C4 bump increases the distance between signal and ground nets on different C4 bumps even with a fixed pitch for C4 bumps. With decreasing on the C_{si_sub} between signal and ground, the insertion loss gets enhanced with a lower leakage loss through capacitive coupling. The change of the C4 bump pitch has the same effect that larger pitch between C4 bumps of signal and ground reduces the capacitance, and therefore improves the insertion loss. The last factor is the silicon conductivity, which is affects by process, temperature, etc.. A descend of the silicon conductivity can significantly diminish the insertion loss. As a conclusion, in order to achieve a better performance regarding to insertion loss, smaller pitch of double TSV on single C4 bump, larger pitch between C4 bumps, and less value of silicon conductivity is recommended.

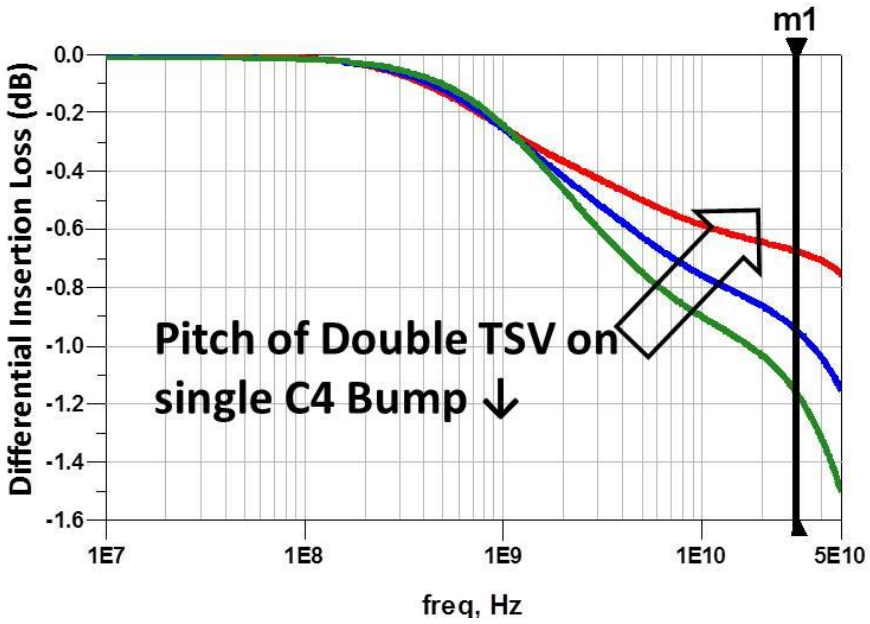


Fig. 22. Effect of pitch between double TSV on single C4 bump on the differential insertion loss.

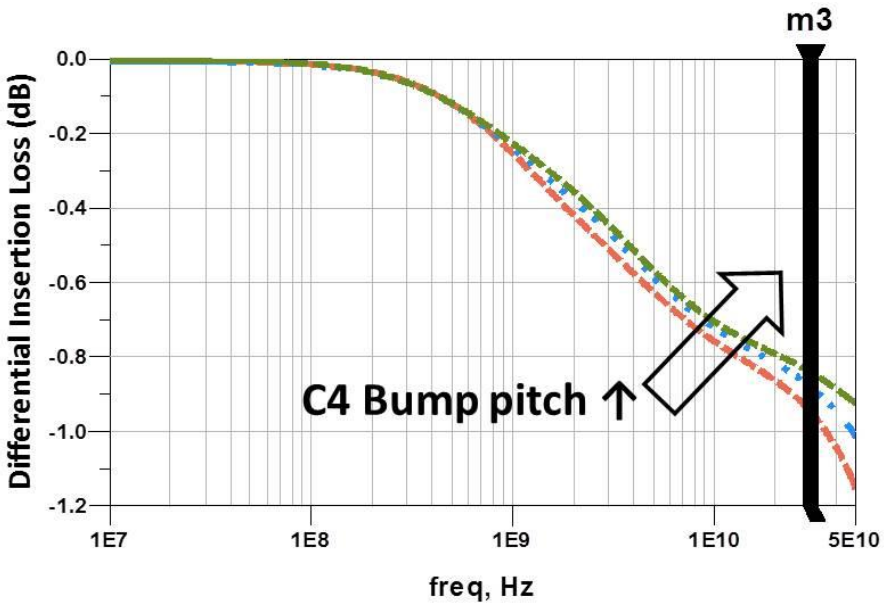


Fig. 23. Effect of pitch between C4 bumps on the differential insertion loss.

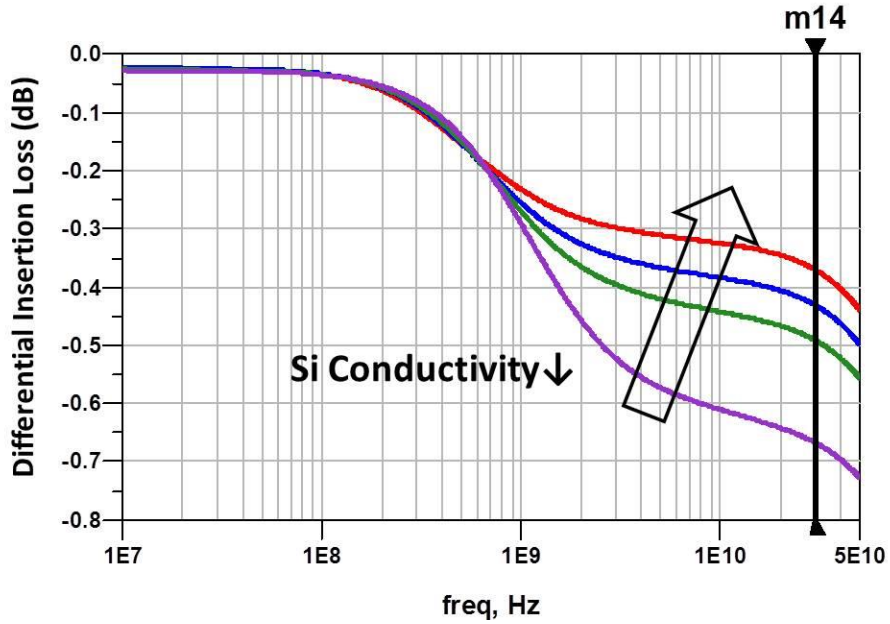


Fig. 24. Effect of silicon conductivity of substrate on the differential insertion loss.

Crosstalk among vias is a significant problem in high-speed multilayer printed circuit boards (PCBs), deteriorating signal quality and increasing jitter, especially when circuit density is high [6]. The crosstalk concern on TSV is much more severe than the convention via on PCB since a tremendous shrink of size from PCB to silicon interposer causes a dense environment and closer couplings for TSV. As well known, the implementation of ground around signal is able to generate a shielding effect between aggressor and victim signals. However, more grounds result in better shielding performance but take more area. The area of interposer is limited and costs high.

Therefore, the placement of ground TSV should consider both shielding effect and density

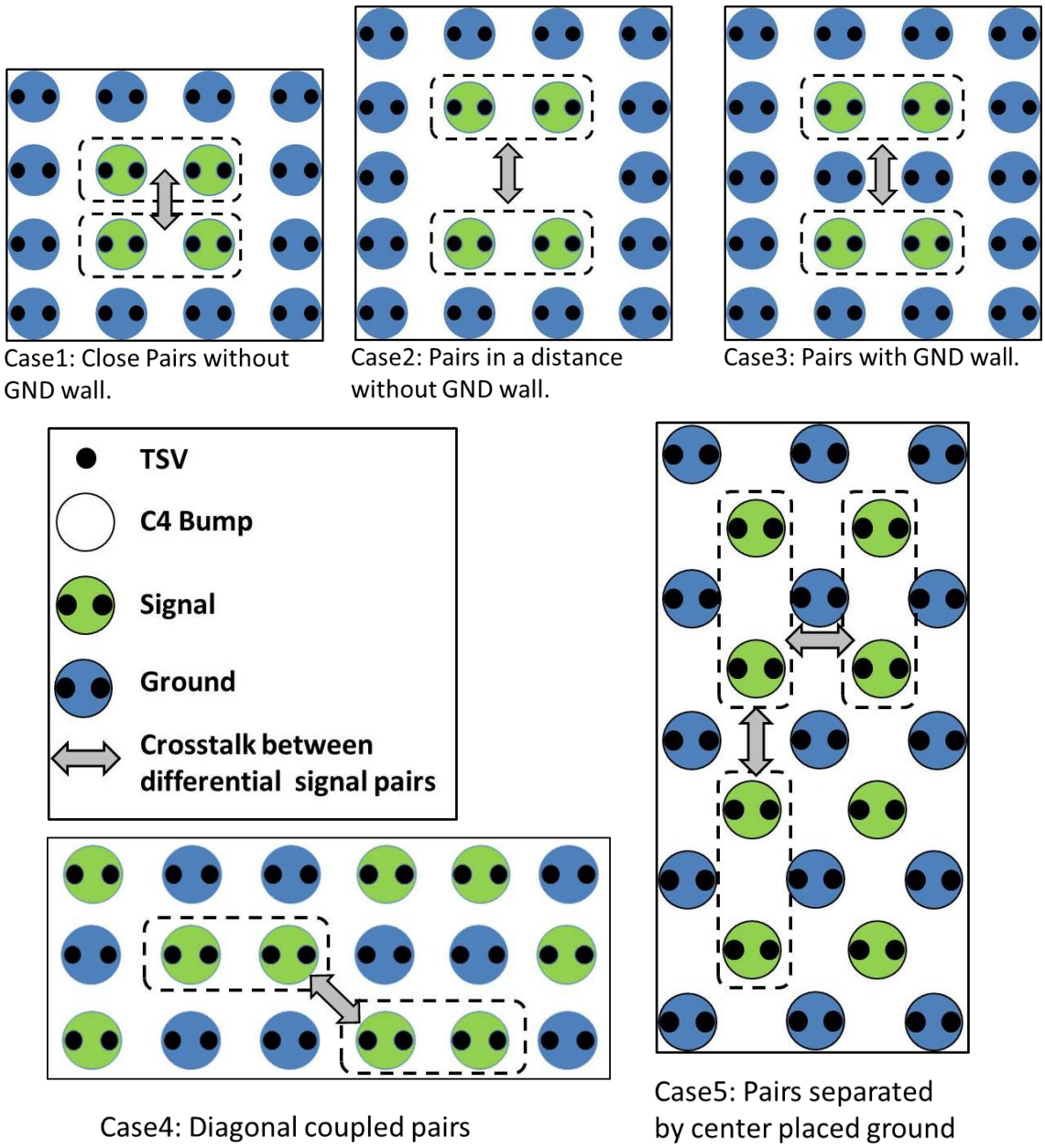


Fig. 25. Common used TSV pin map for estimation the crosstalk effect and area cost.

To estimate the effect of crosstalk, we designed 5 common used TSV pin assignment patterns with the same pitch between each C4 bump as shown in Fig. 25. Pattern in Case 1 is the most conventional tightly coupled differential pairs, which has the worst crosstalk level between two signal pairs. In order to reduce the crosstalk, an enlargement of the gap between two pairs can be applied as case 2. It increases the area taken compared to case 1. The crosstalk level is able to be continuously attenuated by inserting the ground TSV

between signal pairs as case 3. Sometimes, the signal pairs are not aligned a line, and placed diagonally as case 4. The space can be diminished from case 2/3 to case 4, but it is still larger than case 1. The staggered pattern of case 5 spends the largest area because it considers couplings happened in both horizontal and vertical directions. It is interested to note that the balanced horizontal coupling, which has the same gap of positive and negative nodes between two differential pairs, works in a better level to mitigate crosstalk than the vertical unbalanced coupling. Based on this experience, it had better to create a balance coupling in the high speed signal design. Comprehensively taking account into crosstalk reduction and area costing, case 3 where signal pair surrounded by ground TSV is recommended for the high speed signal routing.

Table 1: Crosstalk VS Area for diverse common used pattern of TSV array.

Category	Area	Differential Insertion Loss (dB)			Differential Crosstalk (dB)		
	Normalized	2GHz	4GHz	8GHz	2GHz	4GHz	8GHz
Case1	1.00	n/a	n/a	n/a	-51.807	-54.532	-54.021
Case2	1.41	-0.430	-0.594	-0.738	-70.978	-81.817	-70.761
Case3	1.41	-0.441	-0.613	-0.737	-79.376	-99.456	-79.364
Case4	1.23	-0.436	-0.600	-0.745	-65.278	-71.235	-71.736
Case5_H	1.93	-0.436	-0.602	-0.730	-68.577	-72.793	-69.906
Case5_V					-64.965	-69.444	-70.640

4. Conclusion and Future Plan

This paper proposes a design method of the 2.5D silicon interposer for the high speed signal transmission in HBM. Since the stack up of the interposer depends on the process technology, the possible variables in the structure would be the width of channel and the relative location between the signal and adjacent shielding ground traces. We discussed the effect of diverse width on the electrical performance, especially the eye width and jitter which are affected by the resistive and capacitive characteristics of interposer and also are the indices of the high speed signal quality. Then the most proper widths for both the microstrip and strip lines of the 2.5D interposer is able to be determined based on the mentioned analysis. The shielding effect of the coplanar ground trace on the signal pairs was also studied, and a decision of choosing the coplanar ground or not can be made by a budgeting between area costing and SI performance.

5. Reference

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