Practical implementation of diode SPICE model with reverse recovery

Denys Zaikin [1]

[1]Serenergy A/S

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Abstract

This paper presents a way to generate the correct SPICE sub- circuit using only parameters from the manufacturer's diode datasheet. Characterization tool software was created and tested and is now freely available to download and use.

Practical implementation of diode SPICE model with reverse recovery

Denys Igorovych Zaikin
den913@gmail.com

Abstract

A way of implementing a physical model of reverse recovery for soft recovery diodes was offered by Peter O. Lauritzen and Cliff L. Ma in 1991. This paper presents a way to generate the correct SPICE sub-circuit using only parameters from the manufacturer's diode datasheet. Characterization tool software was created and tested and is now freely available to download and use.

1. Introduction

Of the many SPICE-based simulators on the market, most still use the old standard diode SPICE model that does not cover reverse recovery correctly. Both LTspice [1] and Pspice [2] are powerful pieces of software that are widely used for power electronics simulation. These SPICE simulators use a basic diode model. Adding a feature to simulate diode reverse recovery will improve loss estimation and circuit behaviour simulation. This is especially attractive for Ltspice, which is a powerful, free simulator that can be used in complex design simulation. This paper applies original theoretical work [3] to the practical implementation of a SPICE macro model of diodes with reverse recovery. The model described in [3] is based on real physical processes in a diode and, because of this, is robust.

A Windows OS application was created to generate a diode macro model using only parameters from the diode manufacturer's datasheet or measurement data.

2. Diode model description

Original work [3] provides the following three equations for diodes with reverse recovery:

$$i(t)=\frac{(q_E-q_M)}{T_M} \tag{1}$$

$$0=\frac{dq_M}{dt}+\frac{q_M}{\tau}-\frac{(q_E-q_M)}{T_M} \tag{2}$$

$$q_E=I_s\tau\left(e^{\left(\frac{v}{nV_T}\right)}-1\right) \tag{3}$$

From equations (1)-(3), the forward DC-bias characteristic can be obtained:

$$i=\frac{I_s}{(1+T_M/\tau)}\left(e^{\left(\frac{v}{nV_T}\right)}-1\right) \tag{4}$$

Here, i is the diode current, v is diode junction voltage, $Vt=kT/q$ is the thermal voltage, Is is saturation current (similar to the SPICE basic diode model parameter) and n is the emission coefficient (similar to the SPICE basic diode model parameter). The variables from [3] are as follows: T_M represents diffusion time, τ recombination lifetime, q_M total stored charge and q_E charge variable. This model is completed with ohmic resistance Rs and junction capacitance Cj, as shown in Fig. 1.

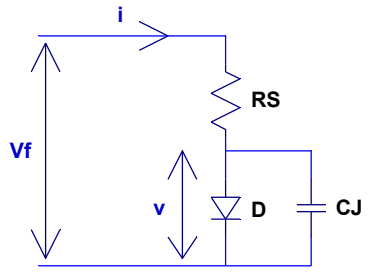

Fig. 1: Diode model components

The practical implementation of equations (1)-(4) in the SPICE model, along with ohmic resistance and junction capacitance, are shown in Fig. 2.

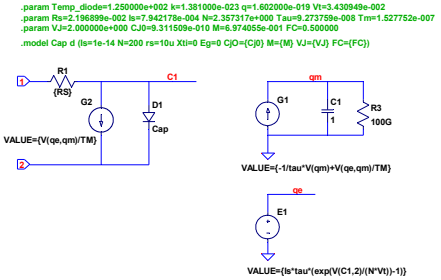

Fig. 2: Implementation of new diode model in SPICE

3. Extraction of model parameters

Equations (1)-(3) fully describe diode reverse recovery and DC bias characteristics of the diode. To use these equations, it is necessary to define τ, T_M, n and Is parameters.

Parameters τ and T_M are defined with the approach used in [3]. An additional intermediate parameter – reverse recovery time constant τ_{rr} – is used and can be measured directly from the reverse recovery waveform or defined from the diode datasheet's parameter τ_{rr}, the reverse recovery time. Fig. 3 shows the JEDEC Standard [4] definition of τ_{rr}.

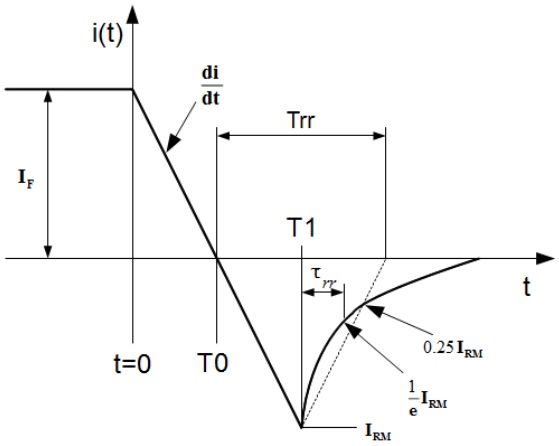

Fig. 3: JEDEC reverse recovery time τ_{rr} definition and waveform

From Fig. 3, τ_{rr} can be found as follows:

$$\tau_{rr} = (I_{RM} * (di/dt) - T_{rr}) / \ln(0.25) \quad (5)$$

Now, when τ_{rr} is known, parameters τ and T_M can be found [3].

To find parameters Is, n and ohmic resistance Rs in equation (4), the standard diode forward DC-bias SPICE model equations are used (Fig. 1):

$$Vf = Rs * i + v \quad (6)$$

$$i = Is' * \left(e^{\left(\frac{v}{nV_T}\right)} - 1\right) \quad (7)$$

Based on (7) and Fig. 4, it can be seen that Is' is the leakage reverse current at the maximum reverse voltage according to the datasheet's reverse DC-bias characteristic of the diode.

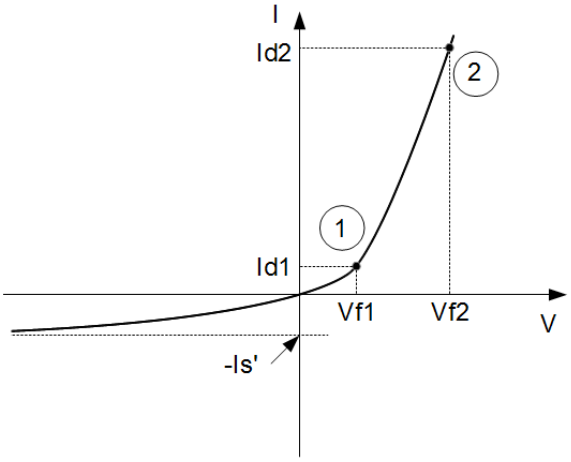

Fig. 4: DC-bias characteristic points

Using (4) and (7), Is can be found:

$$Is = Is' * (1 + T_M/\tau) \quad (8)$$

To find Rs and n, two points should be defined on the DC-bias diode characteristic (Fig. 4). From (6) and (7), there is system of equations with two unknown variables, Rs and n:

$$\begin{cases} Vf1 = n * V_T * \ln(Id1/Is' + 1) + Rs * Id1 \\ Vf2 = n * V_T * \ln(Id2/Is' + 1) + Rs * Id2 \end{cases} \quad (9)$$

After (9) is solved, Rs and n are found:

$$n=\frac{(Vf1*Id2-Vf2*Id1)}{\ln\left(\frac{(\frac{Id1}{Is'}+1)*Id2}{(\frac{Id2}{Is'}+1)*Id1}\right)}*\left(\frac{1}{V_T}\right) \quad (10)$$

$$Rs=\frac{(Vf2-V_T*n*\ln(Id2/Is'+1))}{Id2} \quad (11)$$

To simulate non-linear junction capacitance, equations from the standard diode SPICE model are used [5]:

$$CJ=CJ0*\left(1-\frac{v}{VJ}\right)^{-M},\ v<FC*VJ \quad (12)$$

$$CJ=\frac{CJ0}{(1-FC)^{(M+1)}}*\left(1-FC*(M+1)+\frac{M*v}{VJ}\right),\ v\geq FC*VJ \quad (13)$$

In this model for junction capacitance, fixed parameters are assumed: VJ = 2.0 and FC = 0.5. It is also necessary to find parameters M and $CJ0$ using two points on the datasheet's reverse bias capacitance curve (Fig. 5).

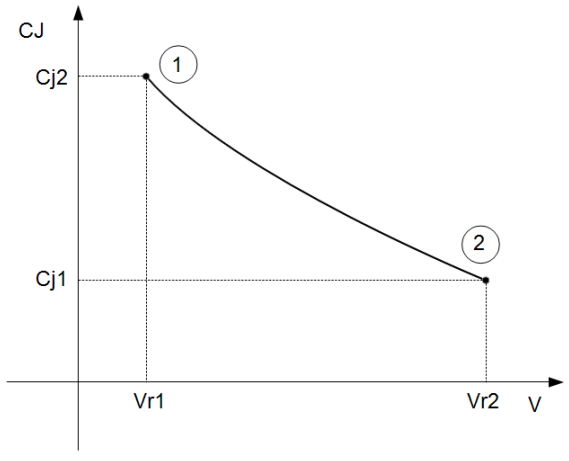

Fig. 5: Junction capacitance points

Using these two points, a system of equations can be obtained based on (12):

$$\begin{cases} Cj1=CJ0*\left(1+\frac{Vr1}{VJ}\right)^{-M} \\ Cj2=CJ0*\left(1+\frac{Vr2}{VJ}\right)^{-M} \end{cases} \quad (14)$$

After (14) is solved, M and $CJ0$ can be found:

$$M=\frac{\ln\left(\frac{Cj1}{Cj2}\right)}{\ln\left(\frac{1+Vr2/VJ}{1+Vr1/VJ}\right)} \quad (15)$$

$$CJ0=Cj1*\left(1+\frac{Vr1}{VJ}\right)^{M} \quad (16)$$

To implement junction capacitance in the new diode model, the standard SPICE diode model is placed in parallel with the diode body (Fig. 2).

The new diode SPICE model implements the behaviour of the diode at a fixed temperature. Lead inductances should be added externally for parasitic simulation.

4. Simulation results

The newly generated model was tested in two simulators – LTspice and Pspice. The LTspice4 simulation results for the MUR460 diode are shown in Fig. 6.

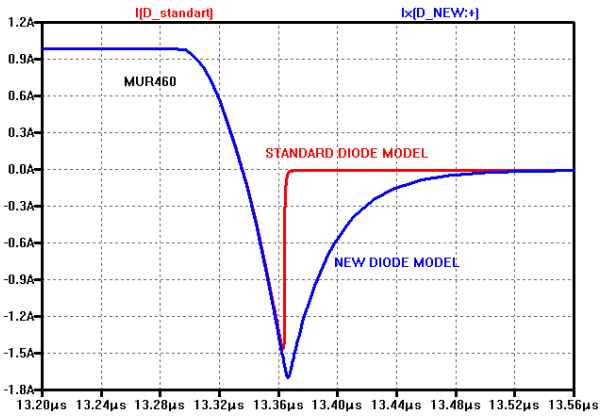

Fig. 6: Comparison of current and standard waveform LTspice4 simulation results for the MUR460 diode. The MUR460 standard diode model was taken from the LTspice4 library.

Pspice 16.6 simulation results for the HFA25TB60 diode are shown in Fig. 7.

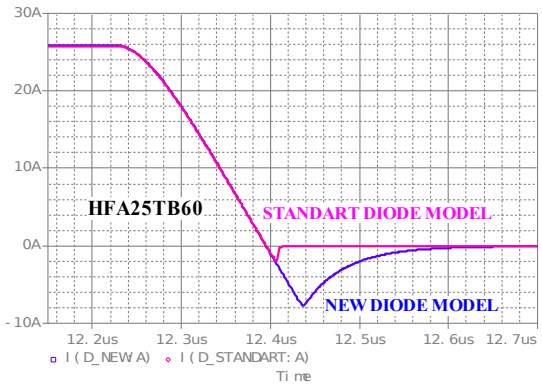

Fig. 7: Comparison of current and standard waveform Pspice 16.6 simulation results for the HFA25TB60 diode. The HFA25TB60 standard diode model was taken from the Pspice 16.6 library.

The Pspice 16.6 simulation results for ISL9R3060 diode are shown in Fig. 8.

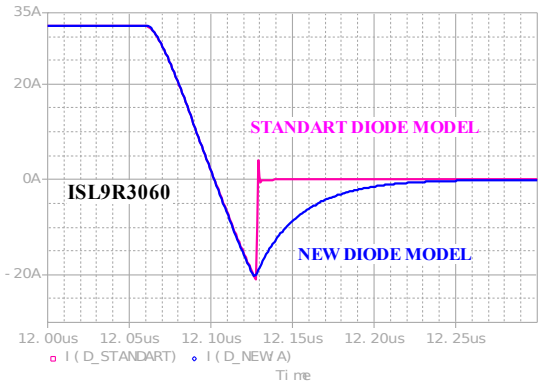

Fig. 8: Comparison of current and standard waveform Pspice 16.6 simulation results for the ISL9R3060 diode. The ISL9R3060 standard diode model was taken from the manufacturer webpage.

5. Software description

To generate the diode SPICE model using the manufacturer's datasheet characterization, the software (SW) tool "DiodeRRSubmodel" was made (Fig. 9). It is a Windows OS application and can be freely downloaded from the links [6], [7]. Next, input data from the datasheet are used as follows:

- user enters diode name;
- user defines work temperature of diode;
- user enters two points on the DC-bias forward characteristic for the specified temperature (Fig. 4, Fig. 10). Points far enough away from each other should be chosen;
- user enters reverse leakage current for diode at specified temperature;
- user enters two points on the junction capacitance (Fig. 5, Fig. 11). Points far enough away from each other should be chosen;
- user enters the reverse recovery specification from the diode datasheet at the specified temperature: *If* , *di/dt*, *Irm*, and *Trr* (Fig. 3, Fig. 12).

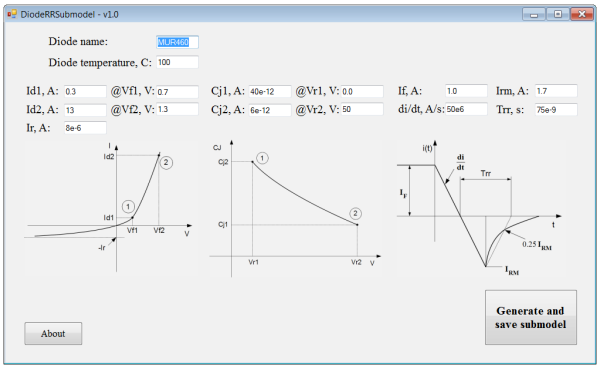

Fig. 9: Windows OS application SW for diode model extraction.

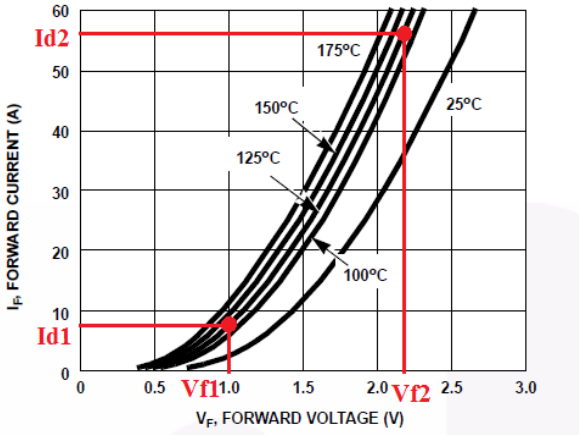

Fig. 10: Two points selected on the DC-bias characteristic.

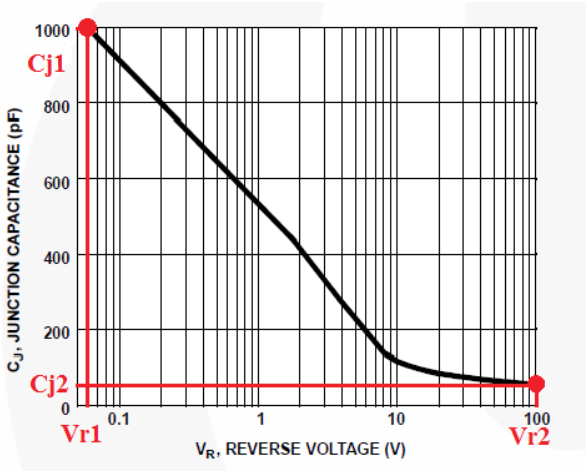

Fig. 11: Two points selected on the junction characteristic.

Q_{rr}	Reverse Recovery Charge		-	450	-	nC
t_{rr}	Reverse Recovery Time	I_F = 30 A, dI_F/dt = 1000 A/µs, V_R = 390 V, T_C = 125°C	-	60	-	ns
S	Softness Factor (t_b/t_a)		-	1.25	-	
I_{rr}	Reverse Recovery Current		-	21	-	A
Q_{rr}	Reverse Recovery Charge			730	-	nC
dI_M/dt	Maximum di/dt during t_b		-	800	-	A/µs

Fig. 12: Reverse recovery datasheet's specifications

The extracted model file is placed in the same folder as the .exe file of the SW. An example of a generated netlist is shown in Fig. 13.

```
* Diode isl9r3060g2 A K
.subckt isl9r3060g2 1 2
.param Temp_diode=125 k=1.381E-23 q=1.602E-19 Vt=0.03430948
.param Rs=0.02156586 Is=0.0004614982 N=2.460456 Tau=5.909138E-08
+Tm=3.181049E-08
.param VJ=2 CJ0=9.311509E-10 M=0.6974055 FC=0.5
R1 C1 1 {RS}
G1 0 qm VALUE={-1/tau*V(qm)+V(qe,qm)/TM}
C1 qm 0 1
E1 qe 0 VALUE={Is*tau*(exp(V(C1,2)/(N*Vt))-1)}
G2 C1 2 VALUE={V(qe,qm)/TM}
R3 qm 0 100G
D1 C1 2 Cap
.model Cap d (Is=1e-14 N=200 rs=10u Xti=0 Eg=0 CjO={Cj0} M={M} VJ={VJ}
+FC={FC})
.ends isl9r3060g2
```

Fig. 13: Generated netlist of new diode sub-model.

6. References

[1] Linear Technology Corporate , *LTspice simulator*, https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html .

[2] Cadence Design Systems, Inc. , *OrCAD PSpice Designer*, https://www.orcad.com/products/orcad-pspice-designer/overview .

[3] Peter O. Lauritzen, Cliff L. Ma, *A Simple Diode Model with Reverse Recovery*, IEEE Trans. on power electronics, vol. 6, No 2, APRIL, 1991.

[4] JEDEC Standard No. 282B.01 .

[5] Ron M. Kielkowski, *SPICE: Practical Device Modeling*, McGraw Hill , 1995.

[6] ZAIKIN D.I., *Software tool for the article: Practical implementation of diode SPICE model with reverse recovery*, https://doi.org/10.6084/m9.figshare.14912769.v1 .

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