Voltage Controlled Domain Wall Motion based Neuron and Stochastic Magnetic Tunnel Junction Synapse for Neuromorphic Computing Applications

Aijaz Lone [1], Selma Amara [2], and Hossein Fariborzi [2]

[1]King Abdullah University of Science and Technology,
[2]Affiliation not available

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Abstract

The present work discusses the proposal of a spintronic neuromorphic system with spin orbit torque driven domain wall motion-based neuron and synapse. We propose a voltage-controlled magnetic anisotropy domain wall motion based magnetic tunnel junction neuron. We investigate how the electric field at the gate (pinning site), generated by the voltage signals from pre-neurons, modulates the domain wall motion, which reflects in the non-linear switching behaviour of neuron magnetization. For the implementation of synaptic weights, we propose 3-terminal MTJ with stochastic domain wall motion in the free layer. We incorporate intrinsic pinning effects by creating triangular notches on the sides of the free layer. The pinning of domain wall and intrinsic thermal noise of device lead to the stochastic behaviour of domain wall motion. The control of this stochasticity by the spin orbit torque is shown to realize the potentiation and depression of the synaptic weight. The micromagnetics and spin transport studies in synapse and neuron are carried out by developing a coupled micromagnetic Non-Equilibrium Green's Function (*MuMag-NEGF*) model. The minimization of the writing current pulse width by leveraging the thermal noise and demagnetization energy is also presented. Finally, we discuss the implementation of digit recognition by the proposed system using a spike time dependent algorithm.

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Aijaz H. Lone, *Student Member IEEE*, S. Amara, *Member IEEE*, and H. Fariborzi, *Member IEEE*

Computer, Electrical and Mathematical Science and Engineering Division, King Abdullah University of Science and Technology, Thuwal, Saudi Arabia.

The present work discusses the proposal of a spintronic neuromorphic system with spin orbit torque driven domain wall motion-based neuron and synapse. We propose a voltage-controlled magnetic anisotropy domain wall motion based magnetic tunnel junction neuron. We investigate how the electric field at the gate (pinning site), generated by the voltage signals from pre-neurons, modulates the domain wall motion, which reflects in the non-linear switching behaviour of neuron magnetization. For the implementation of synaptic weights, we propose 3-terminal MTJ with stochastic domain wall motion in the free layer. We incorporate intrinsic pinning effects by creating triangular notches on the sides of the free layer. The pinning of domain wall and intrinsic thermal noise of device lead to the stochastic behaviour of domain wall motion. The control of this stochasticity by the spin orbit torque is shown to realize the potentiation and depression of the synaptic weight. The micromagnetics and spin transport studies in synapse and neuron are carried out by developing a coupled micromagnetic Non-Equilibrium Green's Function (*MuMag-NEGF*) model. The minimization of the writing current pulse width by leveraging the thermal noise and demagnetization energy is also presented. Finally, we discuss the implementation of digit recognition by the proposed system using a spike time dependent algorithm.

***Index Terms*— Neuromorphic computing, magnetic tunnel junction (MTJ), voltage-controlled neuron, domain wall motion, Spin orbit torque, thermal effects, and pattern recognition.**

I. INTRODUCTION

HE highly energy efficient computational power of brain has inspired a paradigm shift in hardware implementation of computing systems [1][2] . The realization of DNN's on GPU and ASICS based on CMOS are limited by the high energy cost associated with the Von-Neumann Bottleneck. [3][4][5]. In comparison to the CMOS implementation, the memristor-based neuromorphic computing is promising to be energy efficient and scalable down to even 2-nm [6][7]. Some spintronic devices such as magnetic tunnel junctions (MTJ), the basic building block of magnetic random-access memories (MRAM), are competitive candidates for the next generation memory applications thanks to their non-volatility, high endurance, low power consumption, high operation speed and integration capability [8][9]. Moreover, the scaling of the MTJ dimensions changes the switching characteristics of the MTJ from the non-volatile and deterministic switching [10][11] to the super-paramagnetic and stochastic behaviour [12][13]. In recent years the MTJ has been widely used in neuromorphic computing as neurons [14] and synapses [15]. Furthermore, with advances in device fabrication technologies, new thermally stable and topologically protected spin textures such as domain walls and skyrmions have emerged. The synapses and neurons based on these emergent spintronic phenomenon have been widely used in the neuromorphic computing[16] [17].

The voltage control of the surface magnetic anisotropy (VCMA) in the 5d transition metals results in temporary lowering of energy barrier during the switching process[18]. Thus, application of voltage along with spin transfer torque or spin orbit torque in the MTJ switching is promising to be more energy efficient [19]. The VCMA is driven by the electric field dependence of the 5d- orbital occupancy of the interface atoms [20]. The electric field control of these devices has attracted extensive attention in memory and logic applications, as it provides an efficient way to improve the data storage density [21][22]. The domain wall velocity in a magnetic layer varies with change in the surface anisotropy by VCMA [23]. Moreover, VCMA improves the magnetic domain nucleation and storage density in a chip [24]. The voltage control of magnetic domain traps shows that a pinning strength of 650 Oe is easily achievable, which is enough to stop a domain wall moving with 20 ms^{-1} [25]. The MTJ with the domain wall motion-based magnetization switching of the free layer has been shown to provide multilevel weights for a spin-based neuron model [26]. Thus, these devices have been used for energy efficient implementation of the neuromorphic computing solutions such as spike time dependent plasticity STDP [27] and unsupervised spintronic clustering [28]. The combined neuromorphic unit consisting of domain wall motion-based synapse and nanomagnet neurons has shown 95% lower power consumption compared to CMOS counterparts [26].

The present work discusses the proposal of a spintronic neuromorphic system with a spin orbit torque driven domain wall motion-based neuron and synapse. The domain wall motion in the neuron is controlled by the electric field at the gate and this electric field is generated by voltage signals from pre-neurons. The application of voltage as input and output variable helps in reducing power consumption, as pinning site can be turned ON/OFF only when required. Furthermore, it

provides better fanout as post-neuron output from first stage can drive a large number of neurons of the next stage, which is going to play an important role in the realization of large-scale neuromorphic architectures. For the implementation of the synaptic weight, we propose 3-terminal MTJ with stochastic domain wall motion in the free layer. The edge roughness causes the intrinsic pinning of domain wall which leads to the stochastic behaviour of domain wall motion in the presence of spin transfer torque and/or spin orbit torque [29]. We have incorporated these intrinsic pinning effects by creating triangular notches on the sides of the free layer. For modelling the micromagnetics and spin transport in the synapse and neuron, we developed a micromagnetic Non-Equilibrium Green's Function (*MuMag-NEGF*) coupled model**)**. We show that thermal effects plus the domain wall pinning results in stochastic domain wall motion but stochasticity can be tuned by the external current in form of a spin orbit torque. We also explain how leveraging the thermal noise, demagnetization energy and anisotropy energy can minimize the writing current pulse width. Finally, using STDP learning algorithm we discuss the implementation of neuromorphic circuit for digit recognition application. We end by concluding a basic summary of our results and discussing the future prospects of our work.

II. VOLTAGE CONTROLLED NEURON AND STOCHASTIC SYNAPSE DEVICES

The proposed neuromorphic system is based on a 3T-MTJ with an extended free layer with dimensions 512 × 128 × 2 nm^3. The free layer is having a domain wall at the centre as shown in the Fig. 1(a). The reference layer and the tunnel barrier are placed towards the right with width same as the free layer but the effective MTJ length is varied in order to capture the neuron output characteristics. The easy axis of the free and reference layer lies in z direction. Depending upon the length of the reference layer the neuron output voltage switches from low to high as a sharp spike for small dimensions or it switches gradually for larger dimensions resulting in non-linear sigmoid type thresholding. The domain wall motion is driven by the spin orbit torque generated at the free layer (CoFeB)/heavy metal (Pt) interface. The direction of DWM depends upon the charge current direction in the heavy metal. Charge current moving in -x direction (electrons in +x direction) drives DWM right whereas charge current in +x drives DWM in -x direction. Since we have put reference layer towards right of the origin, a short negative current pulse is used to drive the neuron throughout our simulation. The extra gate (oxide layer) is placed at the 30 nm right between the origin and the MTJ. This small oxide layer acts as the gate by controlling the surface anisotropy of the free layer below the gate oxide. The electric field at the gate/free layer interface modulates the 5d-orbital occupancy of surface's atoms which varies the surface's anisotropy [30]. The current signals from the pre-neurons after getting weighted by their respective synapses add up and generate gate voltage. Depending upon the sign and magnitude of gate voltage the anisotropy can be increased or reduced by few percent (~5%). This results in the increasing of the DW-velocity, reduction of DW-velocity or complete pinning of DW.

Fig. 1(b) shows the MTJ synapse device structure with dimensions $1\mu m \times 128nm \times 2nm$. We consider the domain wall at the origin (0) and it moves in both +x and -x with the application of charge current across the heavy metal. The magnetic free layer/heavy metal interface generates SOT which acts as main driving force for the DWM. For the realization of the thermally stable resistance values the domain wall should remain stable in absence of an external bias. Thus, we create artificial pinning in our design which can be justified by the interface roughness resulting in some intrinsic pinning of the DW. We model this pinning by creating small (5~10) nm triangular notches in the free layer sides. In presence of thermal noise and pinning, the DWM becomes stochastic but, by applying a proper number of positive and/or negative SOT pulses, the DW ends up either in right end with current in -x axis or it moves left in the presence of +x directed current pulses.

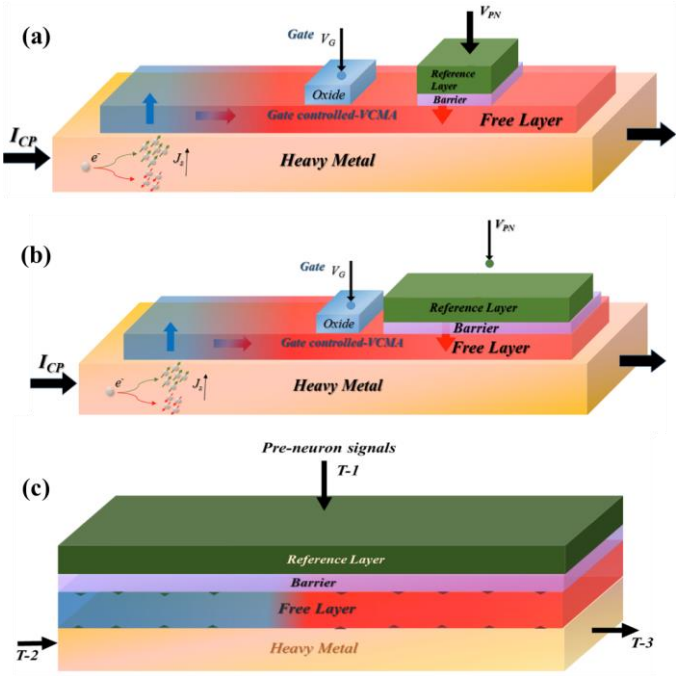

Fig. 1(a) Voltage-controlled neuron with reference layer of length 50nm, for realization of spiking neuron output. **(b)** For the same current density, the device with larger reference layer, length *L*= 170 nm switches gradually thus, sigmoid function of tuneable slope can be realized. **(c)** MTJ-Synapse device structure with notches for artificial pinning and stochasticity.

III. SYNAPSE AND NEURON MODELING

For modelling the micromagnetics and spin transport in synapse and neuron, we developed a micromagnetic Non-Equilibrium Green's Function (*MuMag-NEGF*) coupled model as shown in Fig. 2(a). The micromagnetic simulations were carried out using MuMax having Landau Lipsitz Gilbert (LLG) equation as the basic magnetization dynamics computing unit [31]. The LLG in absence of any spin transfer torque or spin orbit torque term describes the magnetization evolution by

$$\frac{d\hat{\boldsymbol{m}}}{dt} = \frac{-\gamma}{1+\alpha^2}\left[\hat{\boldsymbol{m}} \times \boldsymbol{H}_{\boldsymbol{eff}} + \hat{\boldsymbol{m}} \times (\hat{\boldsymbol{m}} \times \boldsymbol{H}_{\boldsymbol{eff}})\right] \quad (1)$$

Where, $\hat{\boldsymbol{m}}$ is the normalized magnetization vector, γ is the gyromagnetic ratio, α is the Gilbert damping coefficient and $\boldsymbol{H_{eff}} = \frac{-1}{\mu_0 M_S}\frac{\boldsymbol{\delta E}}{\boldsymbol{\delta m}}$ is the effective magnetic field around which magnetization preces. The total magnetic energy of the free layer includes Exchange energy, Zeeman energy, Uniaxial anisotropy energy, demagnetization energy and any other energy terms [32].

$$E(\boldsymbol{m}) = \int_V [(A\nabla \boldsymbol{m})^2] - \mu_0 \boldsymbol{M}.H_{ext} - \frac{\mu_0}{2} M.H_d - \overrightarrow{K_U}.\boldsymbol{M}]dv \quad (2)$$

We also include the thermal noise term into our simulations by adding a random field term H_{th} as a function of the temperature with properties [33] such as zero mean and spatially-temporally uncorrelated:

$$\langle H_{th}(\boldsymbol{r},t)\rangle = 0 \quad (3)$$

$$\langle H_{th}(\boldsymbol{r},t)\rangle \ .\langle H_{th}(\boldsymbol{r}',t')\rangle = \frac{2k_B T\alpha}{M_S \gamma}\delta(r-r')\delta(t-t') \quad (4)$$

By adopting the method from [34] [35] we add spin orbit torque as a custom field term in MuMax.

$$\boldsymbol{\tau_{SOT}} = -\frac{\gamma}{1+\alpha^2} a_J[(1+\xi\alpha)\boldsymbol{m}\times(\boldsymbol{m}\times\boldsymbol{p}) + (\xi-\alpha)(\boldsymbol{m}\times\boldsymbol{p})]$$

$$a_J = \left|\frac{\hbar}{2M_S e\mu_0}\frac{\theta_{SH} j}{d}\right| \quad \text{and } \boldsymbol{p} = sign(\theta_{SH})\boldsymbol{j}\times\boldsymbol{n} \quad (5)$$

Where θ_{SH} is the spin Hall coefficient of the material, j is the current density and d is the free layer thickness.

The magnetization of the free layer acts as the input variable to the spin transport module which computes the time evolution of the synapse resistance and the neuron output. We use effective mass tight binding and mode space approach method to formulate the MTJ device as shown in Fig. 2(b) [36]. The complete device Hamiltonian is expressed as below-[37]

$$H_D = H_{LFM} + H_{I1} + H_{TB} + H_{I2} + H_{RFM} \quad (6)$$

where, H_D is the complete device Hamiltonian consisting of the H_{LFM}, H_I, H_{TB}, H_{RFM} corresponding to the Hamiltonians of left FM, interface, TB, and right FM respectively. The Hamiltonian is described in terms of onsite potential ε_0, and hopping parameter t is given by-

$$t = \frac{-\hbar^2}{2ma^2} \quad (7)$$

Where h, m, and a are reduced Planck's constant, effective mass of the electron and lattice spacing in the model, respectively. The retarded Green's function describing this device is computed as per [19]

$$G^R(E) = [(E+i\eta) - H - \sum L - \sum R]^{-1} \quad (8)$$

and advanced Green's function as

$$G^A(E) = G^R(E)^+ \quad (9)$$

Where E is the energy range of interest in the transport direction and is computed from the band structure (E, k).
Solving it further, the current between unit cell k and $k+1$ is computed by

$$I_{C_\sigma} = trace\left\{\sum_{k_t} C_\sigma \frac{i}{\hbar}\begin{Bmatrix} H_{k,k+1}\, G^n{}_{k+1,k} \\ -G^n{}_{k,k+1} H_{k+1,k}\end{Bmatrix}\right\} \quad (10)$$

$$R_{syn} = \frac{V_{PreN}}{I_{MTJ}} \quad (11).$$

$$V_{PostN} = V_{Read} - I_{PostN} R_F \quad (12)$$

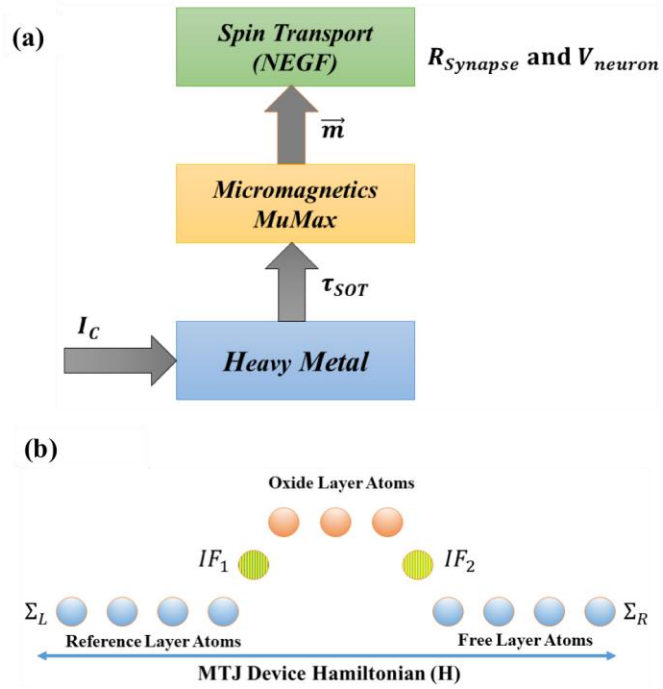

Fig. 2(a) MuMax coupled NEGF model for micromagnetics and spin transport study of synapse and neuron. **(b)** The pictorial representation of NEGF formulation of the neuron and synapse for computation of resistance (weight) and post-neuron output.

IV. Results and Discussion

The voltage control of the domain wall motion is shown in Fig. 3. The voltage control of the surface magnetic anisotropy is expressed by [38].

$$K_S(V) = K_S(0) - \frac{\xi E}{t_F} \quad (13)$$

Where $K_S(V)$ is the anisotropy at voltage V, E is the electric field across oxide, ξ is the VCMA coefficient and t_F is the thickness of the free layer. In Fig. 3(a) we observe that for the zero bias at gate the domain wall moves up to 90 nm in 4 ns in presence of the spin orbit torque. For the positive bias at the gate the surface anisotropy of the region below the gate is reduced depending upon the magnitude of gate voltage. For different values of the ξ and the free layer thickness the voltage dependence of K_S is tabulated in I.

Table. I
Variation of surface anisotropy with gate voltage
for different VCMA coefficients and ferromagnet thickness

$\xi(\mu Jm^{-2}/(Vnm^{-1})^{-1}$	$t_F(nm)$	$\Delta K_S(\%)$	Vg(V)
77	1.5	1	1.14
77 [35]	1.5	2	2.29
77	1	1	0.76
77	1	2	1.53
130 [35]	1	1	0.45
130	1	2	0.9

In case of a positive gate voltage of magnitude 1.53 V, the domain wall velocity is increased and it moves 110 nm. The negative gate voltage of same magnitude increases the surface anisotropy resulting in the reduction of domain wall velocity and the domain wall gets completely pinned for voltage above this threshold value. The domain wall velocity variation with VCMA has also been reported by [20].

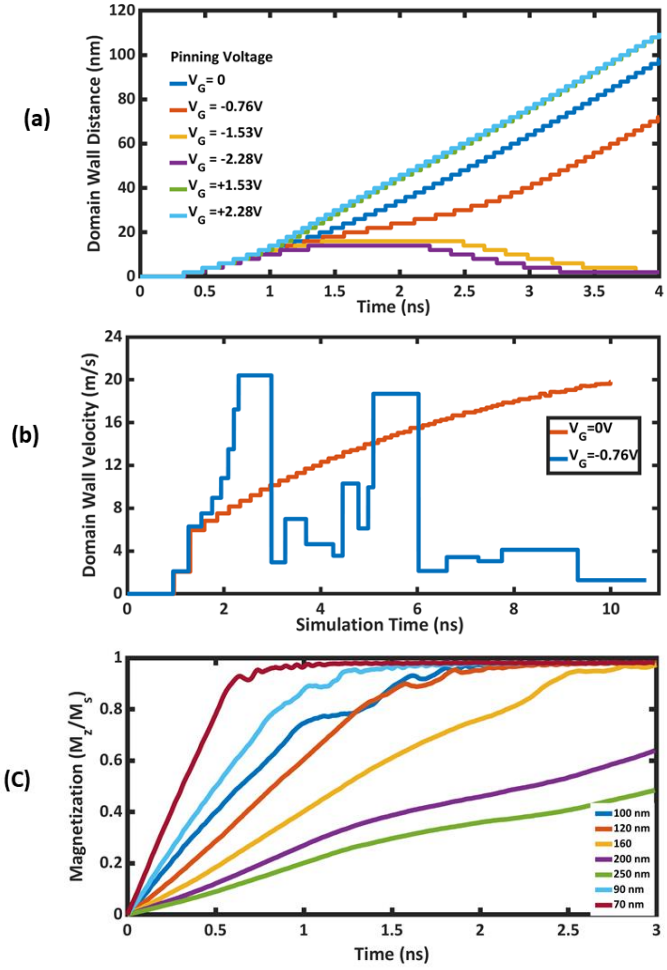

Fig. 3(a) Voltage control of the domain wall motion. (b) The DW- speed for zero bias and negative bias case. (c) Neuron threshold function modulation versus the area of the effective MTJ.

In Fig. 1(c) we show the response of MTJ-neuron magnetization for different cross-sectional areas. For the same magnitude of current, we observe that if the length of the reference layer is small the domain wall traverses this length abruptly, which reflects in the spike type neuron output. As we increase the length, the output voltage starts changing gradually. Thus, for spiking type neurons, we prefer the smaller effective MTJ length whereas larger effective MTJ lengths can be useful for the realization of the sigmoid type threshold functions. Thus, by proper device fabrication we can adjust the slope of the neuron thresholding function as per learning algorithm requirement.

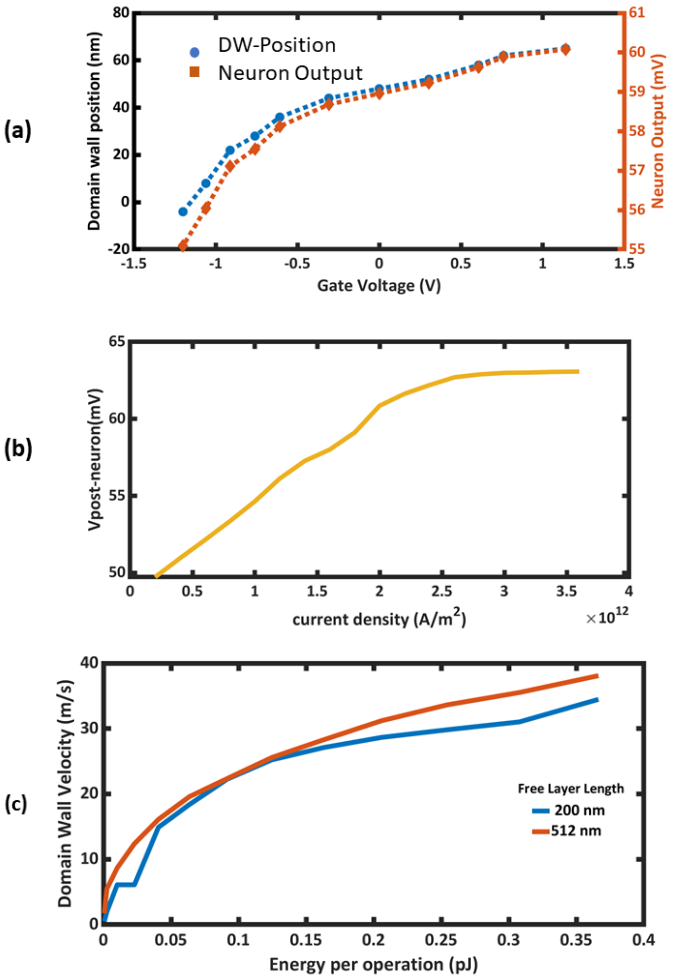

Fig. 4 (a) Domain wall position and post-neuron output voltage controlled by the gate bias. (b) The post neuron output response for the driving current density showing more flexibility in adjusting the behavior of thresholding function. (c) Energy per neuron operation (4 ns) versus domain wall velocity scaling for large and small length effective.

Fig. 4(a) shows the domain wall position and post-neuron output voltage as function of the gate voltage. The domain wall moves more right with increase in gate voltage and this gets reflected in the increased post neuron output voltage. The neuron output voltage is given by

$$V_{PostN} = V_{Read} - I_{PostN} R_F \quad (14)$$

The increasing neuron output voltage indicates reduction in post-neuron current. Thus, the MTJ gradually switches from parallel to antiparallel state. The magnitude of neuron output voltage is controlled by the gate voltage. In Fig. 4(b) we show the response of the post-neuron with respect to the magnitude of the driving pulse current density. The neuron output voltage response is linear for lower current density *J*, it becomes non-linear for current density around $1.5x10^{12}$ A/m^2 and starts to saturate at J=$2.5x10^{12}$ A/m^2. Thus, using by tuning the gate bias and driving current simultaneously we can adjust the thresholding function of the post-neuron as per algorithmic requirement. So, the proposed neuron device structure is more flexible to adjustments in behavior of the thresholding function which is valuable to deep learning community. The energy per neuron operation versus domain wall velocity scaling for large and small length effective MTJ is presented in the Fig. 4(c) we observe that the domain wall velocity increases sharply for low energies but a saturating behavior is seen after 0.15 pJ energy. In addition to that, for the same energy the velocity of larger length MTJ is slightly higher. The time evolution of the synaptic weight in terms of 3T-MTJ resistance and domain wall position is shown in Fig. 5. For the realization of the better thermal stability and non-volatile weights, the temporary domain wall pining is important as domain wall moves across the free layer. In Fig. 5 we clearly observe the pinning and depinning of the domain wall at different sites across the free layer length. The thermal noise and the artificial pinning sites in the proposed device cause the stochastic domain wall motion during the training phase. But the stochasticity is tunable with SOT. In the presence of more positive current pulses, we observe domain wall moving righter and resistance is increased correspondingly which indicates synaptic weight depression while the dominating number of negative current pulses results in the domain wall motion more towards left. Consequently, the resistance is decreased indicating synaptic weight potentiation.

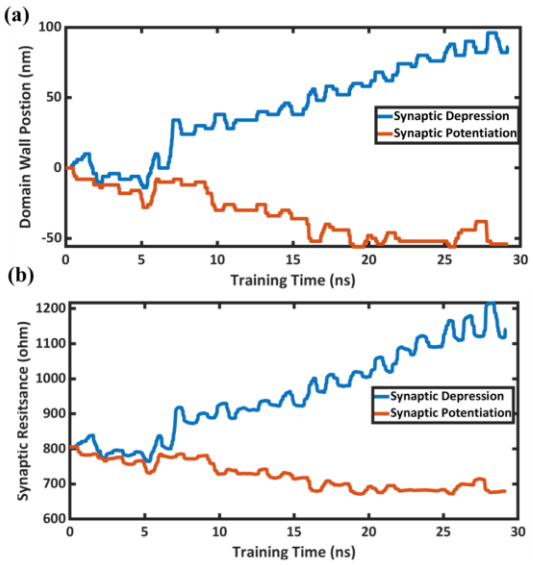

Fig. 5 (a) The time evolution of domain wall position during the training phase showing potentiation and depression. (b) The synaptic weight evolution in terms of 3T- MTJ synapse resistance for potentiation and depression.

To analyze the impact of temperature and demagnetization on the performance of both neuron and synapse performance. we simulated the devices in presence of the thermal noise with temperature as parameter. In Fig. 6 (a) we show that the presence of thermal noise and demagnetization field help in reducing the energy dissipation during the neuron operation. For different driving current pulses with varying pulse width, we show that if the driving current is switched off just around time 1 ns. The domain wall persists its motion as shown in Fig. 6(a). But, for reliable detection the pulse width should be above 1 ns. In Fig. 6(b) we observe that in absence of any current via heavy metal the domain wall velocity is reduced from average 60 m/s to 20 m/s but domain wall velocity is still enough for a reliable writing operation. Thus, we have a tradeoff between energy dissipation and writing time.

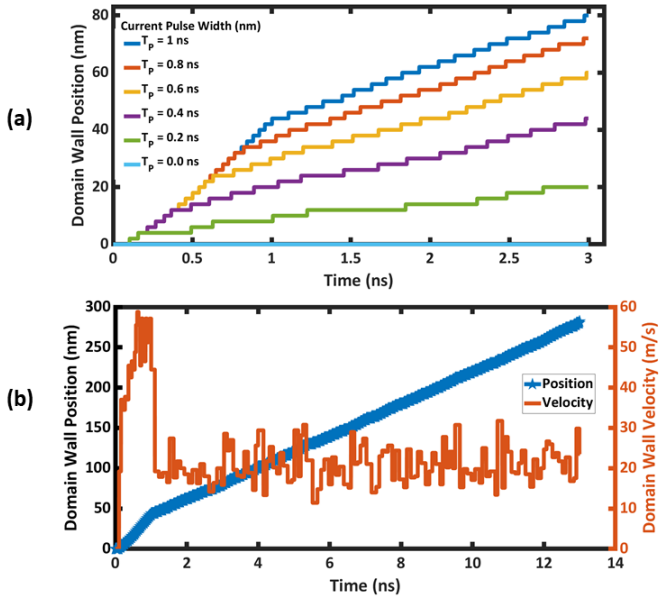

Fig. 6(a) Domain wall motion after a small current spike. (b) The domain wall velocity is reduced by 3 times but still enough for reliable neuron operation.

In case of synapse in Fig 7 (a-b), we show that the evolution of synapse resistance in time is random. With temperatures increasing, the resistance begins to drop sharply indicating increased domain wall velocity. Increasing temperature results in sharper drop and the critical point in time for this behavior shits more towards origin. The critical point is at 2 ns for 300 K and drops to 1.6 ns for 340 K. The free layer magnetization shows an increasing trend with temperature, but the behavior is stochastic.

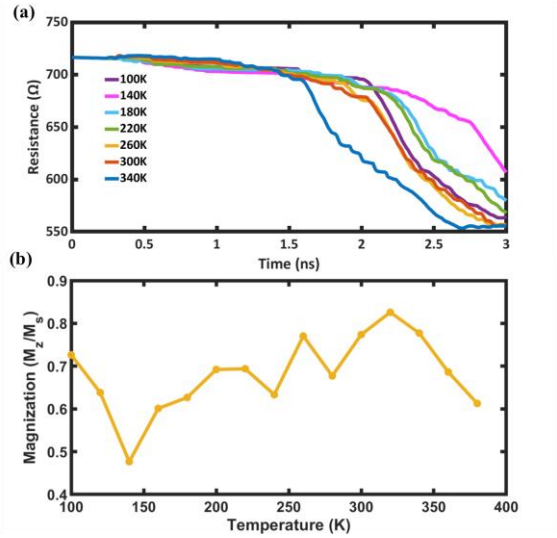

Fig. 7(a) Synapse resistance (weight) time evolution for increasing temperatures shows sharp resistance roll-off after 1.6 ns for high temperatures. (b) Free layer magnetization versus temperature

V. NEUROMORPHIC CIRCUIT IMPLEMENTATION

The neuromorphic circuit for digit recognition applications is based on the voltage-controlled neuron and stochastic domain wall synapses in a cross-bar architecture. The circuit also consists of the sensing unit and weight update circuitry as shown in Fig. 8(c). The circuit description of weight unit and sensing unit is provided in the supplementary material. Following the STDP learning algorithm for the image recognition. In Fig. 8(a) we present the feedforward neural architecture for the implementation of the digit recognition by the circuit. For the reduced complexity we represent the image by 5x4 pixel geometry where each pixel can take values from 0 to 250 mV. Where 0 represents completely dark pixel and 50 mV correspond to bright pixel. The pre-neuron layer consists of the 20 neurons each representing a pixel from image and post neuron layer has total 10 neurons representing digits from 0 to 9 respectively. The number of synapses (Domain wall MTJs) is 200. For training network for digit 1, we first give a small (-0.7 V) negative voltage bias to post-neuron-1 and all other post-neurons are biased more negatively (-1.5 V) to ensure inhibition. The circuit is presented with the pre-neuron voltage pulses where each bright digit pixel has 250 mV amplitude and background noise is below 20 mV.

The total voltage drop across the biasing resistor (transistor) at the post neuron gate is

$$V_G(i) = R_G \times J(i) + V_B(i)$$

Where, $VB(i)$ is the i^{th}- post-neuron bias voltage, $J(i)$ is the net current via gate transistor and is computed by:

$$J(i) = \sum_{k=1}^{n} \frac{V_{Pre}(k)}{W_{ik}}$$

Since, post-neuron-1 is biased less negatively, in absence of any current coming from the pre-neurons, the surface anisotropy below gate remains high by around (1 to 2) % thus causing domain wall pinning, even if we turn on the driving current pulse at terminal T_3. As soon as network is presented with the training pulses, the gate voltage at post-neuron-1 switches from negative to positive which increases the DW velocity thus, neuron is on. At the same time a short current pulse of current density -2x10^{12} A/m^2 flows via heavy metal, driving DW towards right which gets detected by the effective MTJ.

The domain wall velocity determines the slope of the post-neuron output and once the neuron fires the small output signal is detected by the sensing unit. The sensing unit switches ON the transistor M1 and switches OFF M2 thus circuit is ready for weight update phase. The weight update unit follows the spike time dependent plasticity (STDP) weight update algorithm. The unit takes pre-neuron and post-neuron signals as a gate input. For the positive correlation between pre-neuron and post neuron the domain wall synapses are potentiated with a greater number of positive current pulses whereas for negative and zero correlation synapses are depressed by providing more negative current pulses.

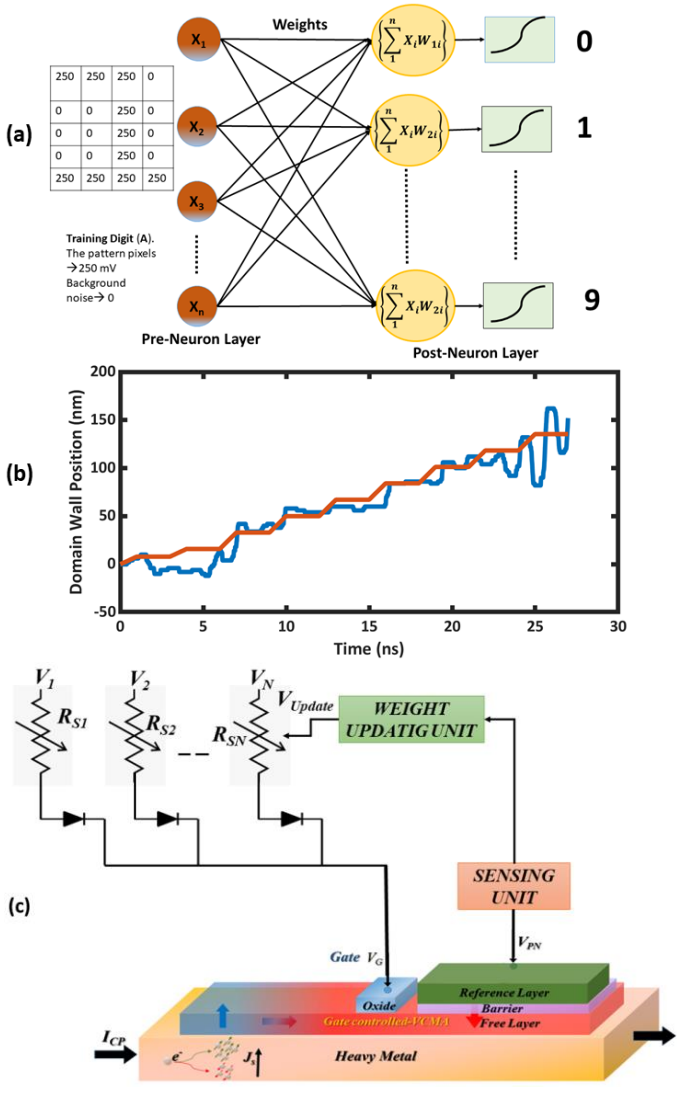

Fig. 8(a) The basic feedforward network involving neurons and synapses in discussion for the circuit representation of the digit recognition application. (b) Analytical fitting (average) of the time evolution of the domain wall position computed with micromagnetic simulations. (c) Neuromorphic circuit schematic for the STDP based digit recognition implementation.

The system level implementation of the STDP for pattern recognition based on these devices is realized by first fitting the synaptic potentiation and depression computed from the device model with an analytical expression:

$$V_{ik}(Avg) = V_{AVG}Y(k) \quad (15a)$$

$$X_{ik}(t) = \int_0^t \alpha V_{ik}(Avg)dt \quad (15b)$$

$$R_{ikS} = R_P\left[\frac{\frac{L}{2} + X_{ik}(t)}{L}\right] + R_{AP}\left[\frac{\frac{L}{2} - X_{ik}(t)}{L}\right] \quad (15c)$$

Fig. 8 (b) shows the analytical expression matching the micromagnetic simulations quite well as an average fit. We consider the analytical model for the system level implementation along with results computed from NEGF-MuMax model to simulate the circuit behavior using MATLAB. The different MOSFET switches are implemented as conditional statements based on the input from pre-neuron, synapse and post-neuron as per the STDP rule discussed earlier.

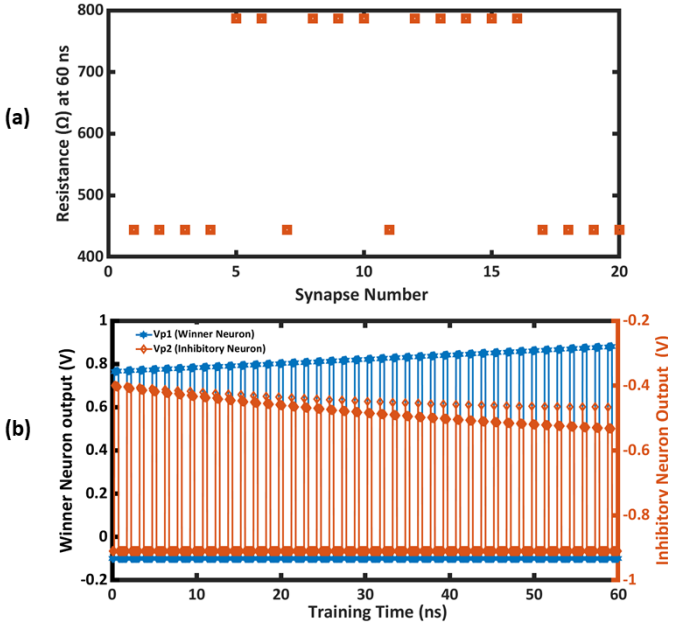

Fig. 9(a) The resistance of synapses connected to winner neuron after 60 ns of training showing all the digit pixel synapses at 443Ω whereas background synapses at 785 Ω respectively. (b) The output voltage (amplified) of post-neuron 1 and 2 showing with training the post-neuron-1 begins to accept more and more digit pixel signals while the all-other post-neurons show opposite trend as their voltage decreases.

We train the network for digit **(1)** for 60 ns and as shown in Fig. 9 the synapse resistance corresponding to the digit pixels have evolved into low resistance state (potentiation) while the background synapses have evolved into high resistance state (depression). Fig. 9 (b) shows the evolution of post neuron output voltage during the learning phase. For the same amount of pre-neuron voltage, we observe the Vp1 is increasing with time so more current flows via heavy metal of post-neuron Vp1 which makes Vp1 the winner neuron. While rest of the neurons Vp2 to Vp10 show a gradually decreasing neuron output which corresponds to the depression of the synapses connecting pre-neurons with rest of the post-neurons. Next, we present the neuron with noisy input **(1)** as the circuit has adopted itself according to pattern 1 the output voltage of post-neuron-1 is highest among all other neurons. Further, depending upon the number of neurons in first layer the recognition accuracy is increased as more voltage will be reaching gate terminal which increases the domain wall velocity. Importantly the speed can be further increased if the driving pulse receives input from the pre-neurons itself thus an increasing current density will automatically increase accuracy.

CONCLUSION

In this paper we proposed a versatile and energy efficient spintronic voltage-controlled neuron which can be tuned by current as well. The dual control provides for the more flexibility in designing neuron threshold function. Further, the fanout is increased as both input and output are voltage. We have also designed stochastic domain wall MTJ based synapse. In order to study and optimize the performance of the MTJ neuron and synapse, a coupled NEGF-MuMAX model is developed. Further, the effect of temperature on the performance in terms of DW velocity of these devices shows how we can take advantage from thermal noise, demagnetization energy and anisotropy energy to reduce the writing energy in these devices. Using the proposed neuron and synapse device structure, we have demonstrated on-chip stochastic dynamic learning by adopting the spike time dependent plasticity as the learning algorithm. At the end of the training phase, we demonstrated that all pattern synapses stochastically evolve into low resistance state (high weight) while the remaining background synapses are in high resistance state (low weight).

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