Compact and Energy Efficient Neuron With Tunable Spiking Frequency in 22-nm FDSOI

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Abstract

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Compact and Energy Efficient Neuron With Tunable Spiking Frequency in 22-nm FDSOI

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***Abstract*—In this paper, we present an integrated and fire neuron designed in a 22-nm FDSOI technology. In this novel design, we deploy the back-gate terminal of FDSOI technology for a tunable design. For the first time, we show analytically and with pre- and post-layout simulations a neuron with tunable spiking frequency using the back-gate voltage of FDSOI technology. The neuron circuit is designed in the sub-threshold region and dissipates an ultra-low energy per spike of the order of Femto Joules per spike. With the layout area of only $30\ \mu m^2$, this is the smallest neuron circuit reported to date.**

***Index Terms*—Spiking Neural Networks, Integrated Circuits, Neuromorphic Computing, Neuron and Synapse, FDSOI, Frequency Modulation**

I. Introduction

Artificial neural networks (ANN) are a promising solution to address the bottlenecks of the Von Neumann paradigms [1]–[18]. Brain-inspired spiking neural networks (SNN) have been introduced as the third generation of ANN emulating biological brain functions in hardware. The basic computing unit in the spiking neural networks (SNNs) are neurons communicating with each other through synapses via the electrical pulses called spikes [2]–[6], [9]–[16], [19]–[24].

Each standard neuronal topology in SNN structures must mimic the known dynamics of a biological neurons such as the adaptive spike-frequency with the biologically plausible time constants. To mimic brain-like functionality a very large number of neurons are required in SNNs. So, the size of the neuronal hardware is also very important. This underlines the need for simple neuronal circuits with minimum number of transistors. The Axon-Hillock [25], Hodgkin-Huxley [26], Morris-Lecar [27], Fitz-Nagumo [28], Resonate and Fire [29], [30], Hindmarsh–Rose [31], Mihalas-Niebur and Izhikevich model [32]–[36] were the leading models inspiring the next generations of the neuromorphic circuit over the last decades [1], [2], [4], [7], [15], [18], [22], [24]. Among these, the Leaky Integrate-and-Fire (I&F) neurons are claimed to be compact, and computationally more efficient. The I&F neurons integrate the pre-synaptic signal through a membrane capacitor and generate spikes once the integrated signal exceeds the spiking threshold [3], [5], [9], [12]–[17], [19]–[21], [23], [32], [37]–[40].

To address the energy issue, the transistors are preferably biased in the sub-threshold region. However, nano-scale CMOS devices suffer from significant leakage currents in sub-threshold. Therefore, novel technologies like the Fully Depleted Silicon on Insulator (FDSOI) have been emerged showing superior performance in terms of leakage and power consumption [1], [16], [18], [41], [42]. The use of back-gate bias is a new possibility in the FDSOI technology to tune the circuit performance. In this paper, for the first time, we propose a neuron design which can use back-gate voltage to modulate the spiking frequency of a compact I&F neuron. Frequency can be modulated in a broad range from $36.8\ kHz$ to $416.67\ kHz$. The proposed neuron operates in the sub-threshold region and consumes an ultra-low energy per spike. The final layout, including the core neuron, six output buffers for measurement purposes, one level-shifter (required for the following I/O block), and all capacitors designed to ensure biological time constants, is only $30\ \mu m^2$ in size.

The paper is organized as follows. Neuron circuit topology and its functionality are presented in the next section. An analytical model of the the frequency modulation as well as the temperature compensation based on the back-gate biasing are also presented in section II. In Section III, the post-layout analysis and the Monte-Carlo simulation results are presented, validating the neuron performance against the process variations, mismatch, leakage, and parasitic components. Conclusions are drawn in the Section IV.

II. FDSOI-based I&F Neuron and Frequency Modulation

A. Neuron Operation

The proposed Integrate-and-Fire neuron is designed in 22-nm FDSOI technology. The topology is shown in Fig. 1. The supply voltage V_{dd} is set to $0.3V$ for the sub-threshold operation. The input synaptic current I_{syn} is a fixed bias current. It is set it to $10\ nA$. Each spike consists of three main transient responses: charging, firing, and resetting. The proposed neuron performs these steps through different parts highlighted in black, green, and red in Fig. 1, respectively. Figure 2 correspondingly illustrate the contribution of each step in the the simplified characteristic of the spikes with the same colour.

The charging step is implemented by C_{mem} and the After Hyper-Polarization (AHP) mechanism composing the transistors M_{4-6} and capacitor C_{ahp}. The AHP mechanism is also used to modulate the spiking-frequency. C_{mem} is responsible for integrating the difference of the synaptic current I_{syn} and the AHP current I_{ahp} and, then, creating the membrane voltage V_{mem}. The charging starts when $I_{syn} > I_{ahp}$. The membrane voltage increases from zero at point A and the charging continues until V_{mem} reaches the spiking threshold V_{th-s} at point B. This step, therefore, takes a charging time t_{AB} that is a function of C_{mem}, I_{syn}, and I_{ahp}. t_{AB} can be calculated by integrating the membrane voltage from zero to the spiking threshold as,

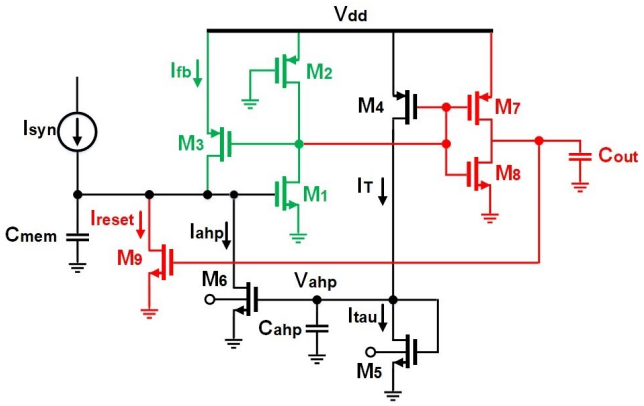

Fig. 1. The proposed I&F neuron with frequency adaptation mechanism.

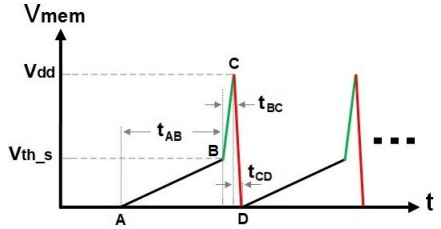

Fig. 2. Simplified spiking characteristic of the neuron in Fig. 1. Each spike composes three steps named the charging (from A to B), firing (between points B and C), and resetting (from C to D).

$$\int_0^{V_{th-s}} C_{mem}\, dV_{mem} = \int_0^{t_{AB}} (I_{syn} - I_{ahp})\, dt \qquad (1)$$

Assuming a fixed pre-synaptic current I_{syn}, the charging time t_{AB} is obtained to be,

$$t_{AB} = \frac{C_{mem} \cdot V_{th-s}}{I_{syn} - I_{ahp}} \qquad (2)$$

Once V_{mem} exceeds the spiking threshold, transistors M_1 turns on. This then turns on M_3. Then, a firing current I_{fb} flows through M_3 which pulls up the membrane voltage V_{mem} to the supply voltage V_{dd} (See point C in Fig. 2). The membrane voltage changes from V_{th-s} to V_{dd} in the firing step. The firing time t_{BC} is calculated as,

$$t_{BC} = \frac{C_{mem} \cdot (V_{dd} - V_{th-s})}{I_{syn} - I_{ahp} + I_{fb}} \approx \frac{C_{mem} \cdot (V_{dd} - V_{th-s})}{I_{fb}} \qquad (3)$$

As soon as M_1 switches on, the inverter (M_7 and M_8) sees a zero bias as its input. As a result the output capacitor C_{out} starts to charge. The output capacitance should be greater than the membrane capacitance to guarantee the sequence of firing and resetting steps. Once C_{out} charges to voltage which can turn M_9 on, the reset current I_{reset} starts to flow. I_{reset} discharges the membrane capacitor to point D (zero volt in our design). The ΔV_{mem} in this step is V_{dd} and the resetting time t_{CD} is given by,

$$t_{CD} = \frac{C_{out} \cdot V_{dd}}{I_{syn} - I_{ahp} - I_{reset}} \approx \frac{C_{out} \cdot V_{dd}}{I_{reset}} \qquad (4)$$

The neuron remains at this point as long as $I_{reset} > I_{syn}$-I_{ahp}. Subsequently M_1 switches off and the inverter is connected to V_{dd} through M_2. Then the next charging starts. t_{BC} and t_{CD} are very small due to the relatively high charging currents I_{fb} and I_{reset}.

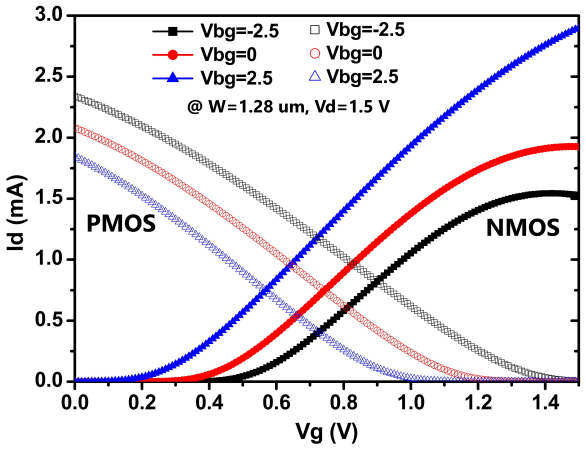

Fig. 3. I_d-V_g characteristics of two NMOS and PMOS device with the same channel width $W = 1.28\ \mu m$ as functions of their back-gate bias.

B. Frequency Modulation

The total period of each spike is the summation of t_{AB}, t_{BC}, and t_{CD}. The spiking frequency f_{spike} is, then, defined as

$$f_{spike} = \frac{1}{t_{AB} + t_{BC} + t_{CD}} \qquad (5)$$

Note that the firing and resetting currents are constant, so, t_{BC} and t_{CD} do not change by back-gate biases V_{bg5} and V_{bg6}. Also, these two time steps are shorter than t_{AB}. To modulate the frequency, we modulate t_{AB} through the AHP current I_{ahp}. FDSOI devices offer unique way to modulate the device current through the back-gate. Figure 3 plots the drain current versus gate voltage (I_d-V_g) characteristics of n- and p-types FDSOI devices with the channel width and length of $W = 1.28\ \mu m$ and $L = 20\ nm$, respectively, and the drain voltage $V_d = 1.5V$. The back-gate voltage V_{bg} is set to $-2.5V$, $0V$, and $2.5V$. As seen, the higher V_{bg}, the smaller threshold voltage, and the greater drain current will be. We use the back-gate bias voltage over of M_6 to change I_{ahp} and, subsequently, the charging time t_{AB}. The back-gate voltages V_{bg5} and V_{bg6} are used to tune the AHP current. Our analytical calculations are validated by comparing with the simulations of t_{AB} with the foundry PDK.

The capacitors are designed by considering the sequence of the charging, firing, and resetting steps. To ensure appropriate sequencing we use $C_{mem} = 3\ fF$, $C_{out} = 9\ fF$, and $C_{ahp} = 40\ fF$. Back-gate voltages are tuned between the allowed range of $0V$ to $1.2V$. Figure 4 sketches the transient characteristics of V_{mem}, derivative of V_{mem} (V'_{mem}), I_{ahp}, I_{fb}, and I_{reset} for $V_{bg5} = 0V$ and $V_{bg6} = 1.2V$. This is the back-gate voltage condition of the lowest spiking frequency.

As shown in Fig. 4 I_{fb} and I_{reset} are equal to the off-current I_{off} and I_{ahp} is constant during the charging period. The rate of charging remains roughly constant from point A to B. However, the firing current I_{fb} starts increasing at point

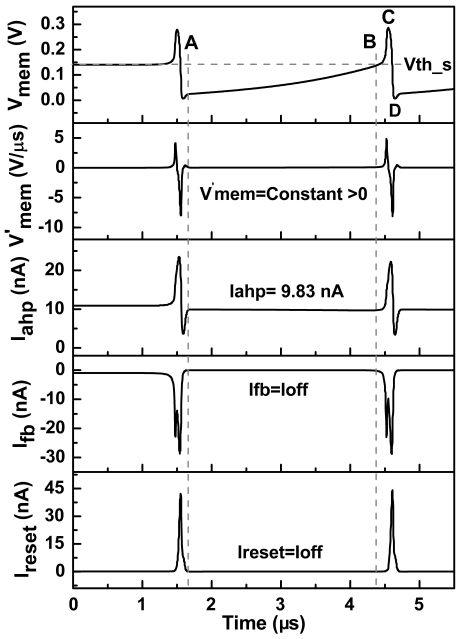

Fig. 4. Calculation of the charging time t_{AB} for the back-gate voltages of $V_{bg5} = 0V$ and $V_{bg6} = 1.2V$. The charging, firing, and resetting steps correspond to the time intervals of A to B, B to C, and C to D, respectively.

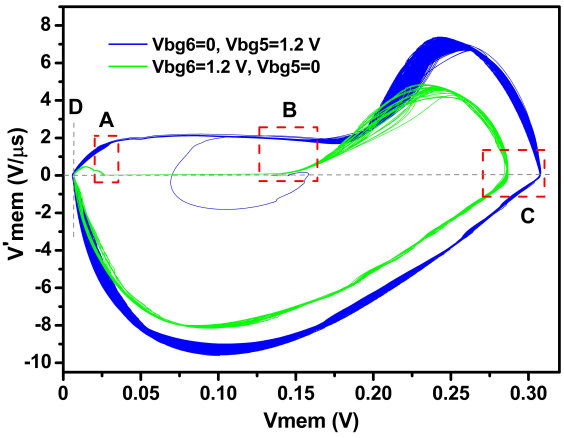

Fig. 5. V'_{mem} versus the membrane voltage for two opposite case of the maximum (blue) and minimum (green) spiking frequencies. The part from point A to point B indicates a relatively fixed slope.

B and V'_{mem} increases. This indicates that the charging step is terminated and the firing step has started.

The maximum V_{mem} in the charging step (at point B) defines the spiking threshold V_{th-s}. Figure 5 provides easier visualization of the spiking threshold. Fig. 5 shows transient simulation results for V'_{mem} as a function of V_{mem} during switching up-to time $t_{tran} = 100\mu s$. This is shown for two back-gate bias conditions which result in minimum and maximum spiking frequency. As seen, V'_{mem} is almost constant from point A to B and, then, changes at membrane voltage of close to $V_{dd}/2 = 0.15V$ which is taken as the spiking threshold. Table I compares the spiking frequency calculated by Eq. (5) with the simulation results for four different bias sets (cases 1-4). From this table, there is an excellent fit between the theoretical analysis and simulation. Plotted in Fig. 6 also illustrates the modulation of the spiking frequency for

TABLE I
COMPARISON BETWEEN THE CALCULATED AND SIMULATED SPIKING FREQUENCY FOR DIFFERENT COMBINATIONS OF V_{bg5} AND V_{bg6}

		Case 1	Case 2	Case 3	Case 4
		$V_{bg5} = 1.2V$ $V_{bg6} = 1.2V$	$V_{bg5} = 0V$ $V_{bg6} = 0V$	$V_{bg5} = 0V$ $V_{bg6} = 1.2V$	$V_{bg5} = 1.2V$ $V_{bg6} = 0V$
f_{spike}	Calculation	$2.5\ MHz$	$3.2\ MHz$	$355\ kHz$	$4.4\ MHz$
	Simulation	$2.2\ MHz$	$2.8\ MHz$	$337\ kHz$	$3.8\ MHz$

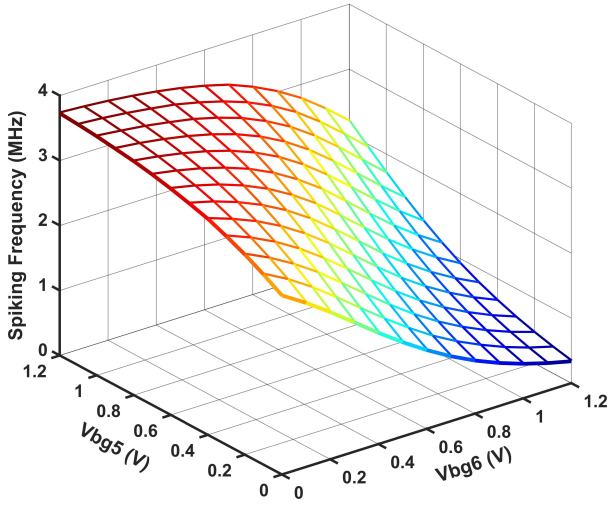

Fig. 6. Variation of the spiking frequency as a function of two back-gate biases V_{bg5} and V_{bg6}.

two back-gate biases V_{bg5} and V_{bg6} swept from $0\ V$ to $1.2\ V$.

C. Monte-Carlo Analysis

To validate the performance of the neuron in terms of mismatch, we performed the Monte-Carlo (M-C) analysis with 200 runs for the firing rate of the neuron. Figures 7(a) and (b), respectively, represent the variations of the maximum and minimum spiking-frequencies with the deviations lower than the standard deviation 3σ.

III. Post-Layout Results and Discussion

A. Layout and the process-variation analysis

The 22nm FDSOI process has many flavors of FETs. After performing I-V simulations of different flavors it become clear that high-threshold FETs (HVTFETs) offer the lowest leakage current as compared to other flavors of FETs in the process. HVTFET is selected to design the neuron circuit. FET widths are optimized with respect to minimize mismatch. The triple well structure, e.g. PMOS in NWELL and NMOS in PWELL, is used for all FETs. This structure allows us to isolate the NMOS device from the global substrate through an NWELL ring surrounding the device and facilitates applying an independent bias to the back-gate node [43]. An n-type current mirror with an input pulse generates the pre-synaptic current I_{syn}. Two 4-bit digital-to-analog converters (DACs) are also designed to generate the two back-gate biases used in

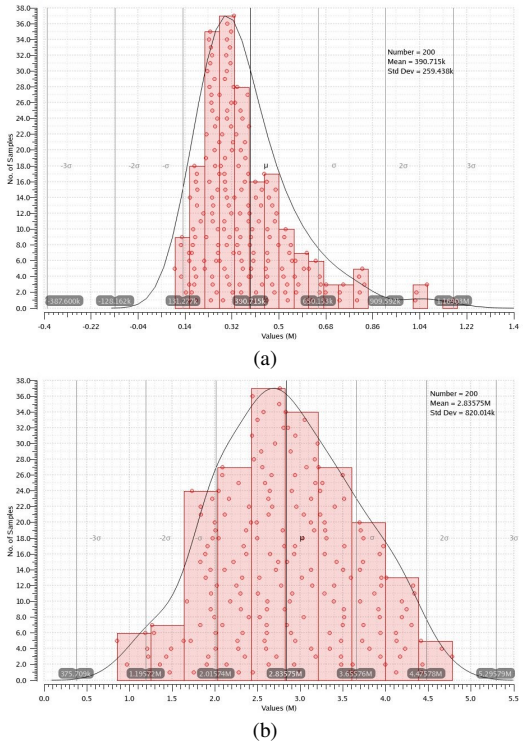

Fig. 7. The Monte-Carlo analysis for (a) the minimum and (b) maximum spiking frequencies.

the neuron circuit (see Fig. 1). These DACs are added to the neuron in the final layout but their areas are excluded from the neuron layout size for a fair comparison with the literature. A level-Shifter circuit [44] is inserted in the neuron layout to generate the output pulses with amplitudes of $0.8V$ needed for the following I/O block. In addition, six output buffers are added for measurement purposes [45].

The Metal-Oxide-Metal (MOM) capacitors are chosen for the capacitors of the circuits as they offer acceptable capacitance density [43]. The final layout is presented in Fig. 8. Transistors with back-gate bias M_5 and M_6, level shifter, and other parts of neuron and buffers are shown in this figure. Total area is $30\mu m^2$ in size considering all blocks and MOM capacitors. Figure 9 shows the output of the level-shifter for the minimum and maximum firing rates. Although the spiking frequency is reduced by the parasitic components [39], [46], [47], the proposed neuron offers a wide frequency range from $36.8kHz$ to $416.67kHz$. The capacitors must take the values to trade-off the area and operating in the real time constants. However, small capacitors in the order of few femto-Farads are vulnerable to the parasitics. We run post-layout simulations for two extreme capacitor corners in PDK (C_{min} and C_{max}) and compare the ratio between f_{max} and f_{min} with the nominal case. The results are summarized in Table II denoting that the frequency ratio remains roughly similar to the nominal case. This means that the capacitors are designed correctly.

B. Energy Dissipation

The energy consumed per spike is an important figure of merit (FoM) for neuron circuit. This FoM has been considered

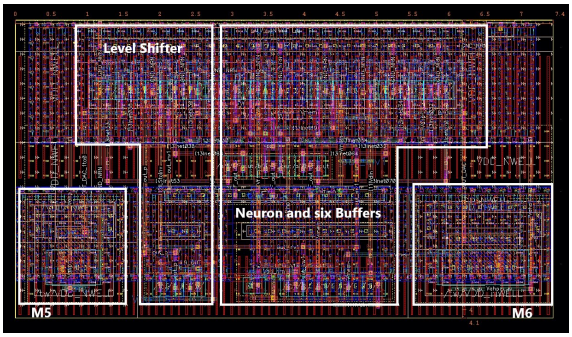

Fig. 8. The final layout including the proposed neuron in Fig. 1, the level-shifter, and all buffers needed for measurement. All capacitors are placed on top of the transistors layout, offering a more compact layout.

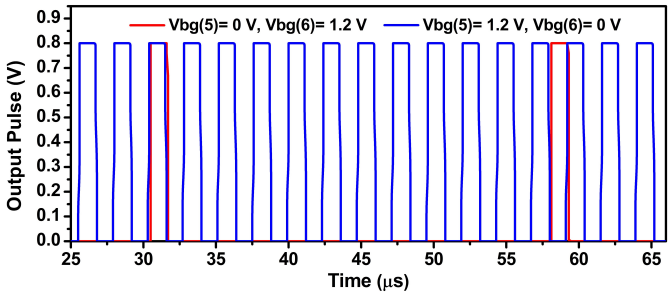

Fig. 9. The output charcteristics of the level-shifter for f_{max} (blue) and f_{min} (red).

TABLE II
CAPACITIVE CORNER-ANALYSIS OF THE NEURON AND COMPARISON THE RESULT WITH THE NOMINAL DESIGN

Corners	$f_{min}(kHz)$	$f_{max}(kHz)$	$\frac{f_{max}}{f_{min}}$
C_{min}	38.28	441	11.52
Nominal	36.8	416.67	11.32
C_{max}	35.52	416.67	11.73

in various works to fairly evaluate the energy efficiency of the neuron circuits [6], [21], [22], [24]. Energy per spike is calculated by dividing the average power consumption P_{ave} by the spiking frequency f_{spike}. The averaged power is given by,

$$P_{ave} = \frac{1}{t_{sim}} \int_0^{t_{sim}} i_{dd}(t) \cdot V_{dd}\, dt \tag{6}$$

or, equivalently,

$$P_{ave} = \frac{f_{spike}}{N} \int_0^{t_{sim}} i_{dd}(t) \cdot V_{dd}\, dt \tag{7}$$

where t_{sim} is the simulation time, $i_{dd}(t)$ represents the total (static and dynamic) current flowing through the supply voltage V_{dd}, and N indicates the number of spikes in the simulation time t_{sim}. The energy per spike E_s is, then, extracted from Eq. (7) and is written as

$$E_s = \frac{P_{ave}}{f_{spike}} = \frac{1}{N} \int_0^{t_{sim}} i_{dd}(t) \cdot V_{dd}\, dt \tag{8}$$

TABLE III
COMPARISON BETWEEN THE PERFORMANCE OF THE PROPOSED NEURON WITH OTHER TOPOLOGIES AND TECHNOLOGIES REPORTED IN THE LITERATURE

Reference		Technology	No. Transistors	V_{dd} (V)	Power	E_s	Frequency	Area
[40]		$0.35\ \mu m\ CMOS$	21	3.3	–	$900\ pJ$	$100\ Hz$	$< 10\ mm^2 *$
[24]		$0.35\ \mu m\ CMOS$	14	3.2	$8 - 40\ \mu W$	$8.5 - 9\ pJ$	–	$2800\ \mu m^2$
[37]		$1.5\ \mu m\ CMOS$	20	5	$0.3 - 1.5\ \mu W$	$3 - 15\ pJ$	$100\ Hz$	–
[1]		$28\ nmFDSOI$	21	1	–	$50\ pJ **$	$30\ Hz$	$50\ \mu m^2$
[5]		$0.18\ \mu m\ CMOS$	21	1.8	–	$883\ pJ$	$30\ Hz$	$1188\ \mu m^2$
[39]		$28\ nmCMOS$	22	$0.7 - 1$	$1.9\ mW$ †	$2.3 - 30\ nJ$	$1 - 100\ kHz$	$64.6\ \mu m^2$
[13]		$0.18\ \mu m\ CMOS$	19	1.8	$2 - 50\ \mu W$	–	–	–
[48]		$CMOS$	$27 - 30$	5	$60\ \mu W$	–	–	–
[49]		$0.35\ \mu m\ CMOS$	21	3.3	–	$7\ pJ$	–	–
[50]		$0.35\ \mu m\ TSMC$	> 32	–	$3.2\ nW$	$45.7\ pJ$	$70\ Hz$	$0.108\ mm^2$
[22]		$65\ nm\ TSMC$	6 ††	0.2	$100\ pW$	$4\ fJ$	$25\ kHz$	$35\ \mu m^2$
[51]		$0.35\ \mu m\ CMOS$	8	–	$1.74\ \mu W$	$17.4\ pJ$	$100\ Hz$	$1887\ \mu m^2$
[12]		$65\ nm\ CMOS$	> 19	–	$78.16\ nW$	$41.2\ pJ$	$1.9\ MHz$	$538\ \mu m^2$
[23]		$90\ nm\ CMOS$	14	0.6	$40.2\ pW$	$0.4\ pJ$	$100\ Hz$	$442\ \mu m^2$
[6]		$28\ nm\ FDSOI$	2	–	–	$35\ fJ$	$56\ kHz$	$12\ \mu m^2$
[7]		$28\ nm\ TSMC$	5 ††	0.2	$30\ pW$	$2\ fJ$	$15.6\ kHz$	$31\ \mu m^2$
[11]		$28\ nm\ CMOS$	–	1.2	–	$35\ pJ$	$100\ MHz$	$1.99\ mm^2$ ‡
[21]		$0.35\ \mu m\ AMS\ CMOS$	21	3.3	–	$7\ pJ$	–	$913\ \mu m^2$
[16]		$28\ nm\ FDSOI$	–	$0.4 - 0.8$	$12 - 49\ nW$	$64 - 280\ fJ$	$16.9 - 524\ MHz$	$574.2\ \mu m^2$
This Work	LF	$22\ nm\ FDSOI$	9	0.3	$1.22\ nW$	$32.36\ fJ$	$36.8\ kHz$	$30\ \mu m^2$
	HF				$4.7\ nW$	$11.28\ fJ$	$416.67\ kHz$	

LF: Low Frequency, HF: High Frequency, * Total area for 32 neurons and 8000 synapses, ** Energy per spike of the whole processor, † Power consumption of the whole neuromorphic system, †† These topologies lack the frequency-adaptation mechanism, ‡192 neurons and 6144 synapses.

The averaged power consumption of the neuron at $f_{min} = 36.8\ kHz$ and $f_{min} = 416.67\ kHz$ are, respectively, $1.22\ nW$ and $4.7\ nW$ that correspond to E_s of $33\ fj/s$ and $11.28\ fj/s$. Table III compares the performance of the proposed neuron with other works. Our design compares well with other silicon neurons in the literature particularly with regards to the energy consumption and the layout size. In addition, it allows frequency modulation in a broad range which is promising for larger SNN systems.

IV. CONCLUSION

In this paper we have presented an Integrate and Fire neuron designed in 22 nm FDSOI technology. The proposed circuit allows spiking frequency modulation. For the first time we propose that the back-gate bias of the FDSOI technology can be used to create this desirable tunability. The performance of the neuron was validated through analytical models, pre-, and post-layout simulations. The proposed adaptive neuron consumes an ultra-low energy with a small layout size.

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