

Design of a Variable-Frequency Inductive Charger for Low-Power Electronic Device Applications

Guodong Zhu ¹ and Dawei Gao ²

¹Tsinghua University

²Affiliation not available

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Abstract

The circuit design method and control strategy of a variable-frequency inductive charger are introduced. The target application is low-power inductive charging systems where the coupling coefficient is relatively stable, e.g., mobile phone chargers with mechanical positioning aids. On the transmitter side, a high-order compensation circuit is deployed to achieve a monotonous frequency-power relation, which allows the output power to be regulated by frequency tuning. Only a half-bridge inverter is required and soft switching is achievable at most operating points. On the receiver side, the load impedance is fixed around the optimal value to improve the energy efficiency. Experimental results show that with low-loss circuit components, the proposed scheme achieves good efficiency performance under full and partial loads.

Design of a Variable-Frequency Inductive Charger for Low-Power Electronic Device Applications

Guodong Zhu, Dawei Gao¹

¹ (Corresponding author) State Key Laboratory of Automotive Safety and Energy, School of Vehicle and Mobility, Tsinghua University, Beijing, China. Email: dwgao@mail.tsinghua.edu.cn

Summary

The circuit design method and control strategy of a variable-frequency inductive charger are introduced. The target application is low-power inductive charging systems where the coupling coefficient is relatively stable, e.g., mobile phone chargers with mechanical positioning aids. On the transmitter side, a high-order compensation circuit is deployed to achieve a monotonous frequency-power relation, which allows the output power to be regulated by frequency tuning. Only a half-bridge inverter is required and soft switching is achievable at most operating points. On the receiver side, the load impedance is fixed around the optimal value to improve the energy efficiency. Experimental results show that with low-loss circuit components, the proposed scheme achieves good efficiency performance under full and partial loads.

Keywords: efficiency, inductive charger, power, wireless charging

1 Introduction

In a typical inductive power transfer (IPT) system, power regulation can be realized via transmitter (TX) -side control, receiver (RX) -side control or dual-side control. Generally, dual-side control can achieve better performance than single-side control due to a higher degree of freedom. For instance, maximum efficiency tracking enabled by a controllable receiver-side converter (either active rectifier [1] or DC/DC converter [2]) greatly improves the partial-load efficiency. The fundamental principle behind efficiency maximization is to match the load impedance to the optimal value [1-2].

In IPT systems, the switching frequency is another degree of freedom. Frequency tuning is utilized to improve the energy efficiency in some references [3], and more commonly adopted to realize zero phase angle of the input impedance [4], zero current switching of the inverter [5] or to regulate the output power within a relatively narrow range [6]. However, the compensation circuit in the last case has not been optimized for power regulation in a wide range at a high efficiency. As a result, power regulation is largely accomplished using other methods.

In this work, frequency tuning is utilized as the major means of output power regulation. A high-order TX-side compensation circuit is deployed to achieve a monotonous power-frequency relation and the output power covers a wide range over the operating frequency band (OFB). Simply a half-bridge inverter is required on the TX side. Series compensation is adopted on the RX side and the load impedance can be maintained at the optimum value using a power converter, thus realizing maximum efficiency tracking. Therefore, dual-side control is utilized in the proposed scheme. The circuit design method and control strategy are introduced, and feasibility of the proposed scheme is validated through simulations and experiments. The target application is

low-power inductive chargers where the coupling coefficient is relatively stable, e.g., mobile phone chargers with mechanical positioning aids.

2 Compensation Circuit Design

2.1 Circuit Diagram

The circuit diagram of the proposed inductive charger is given in Fig. 1. The input DC voltage (U_{IN}) together with the DC-link capacitor (C_{IN}) is connected to the input side of a half-bridge inverter composed of two Si-MOSFETs (Q1 and Q2). Although Si-MOSFETs are outperformed by their SiC-based counterparts in terms of switching loss, their low cost and comparable on-state resistance make them a suitable choice for this work. After all, soft switching of the inverter is one of the goals in the design process. The benefits of using a half-bridge inverter are obvious: simpler structure and lower cost. On the RX side, a passive rectifier composed of four diodes (D1-D4) is used. C_{OUT} is the RX-side DC-link voltage and U_{OUT} is the DC voltage across the load resistance (R_{load}).

Unless otherwise specified, only the fundamental voltages and currents are considered in the calculations. U_{inv} and I_{inv} are phasor forms of the inverter output voltage and current, respectively. U_{rec} is the rectifier input voltage. I_1 and I_2 are the currents in the TX and RX coils, respectively. The TX coil (L_{tx}) and the RX coil (L_{rx}) are coupled by the mutual inductance M . The TX-side compensation circuit is a complex combination of capacitors and inductors (L_{1-3} and C_{1-3}), the purpose of which is to increase the degree of freedom, thereby realizing a monotonous power-frequency relation and a positive input impedance angle ($\angle Z_{inv}$). The RX-side compensation circuit is much simpler, with only a series capacitor (C_{rx}) for reactive power compensation. The impedance observed at the rectifier input port is designated as Z_{rec} .

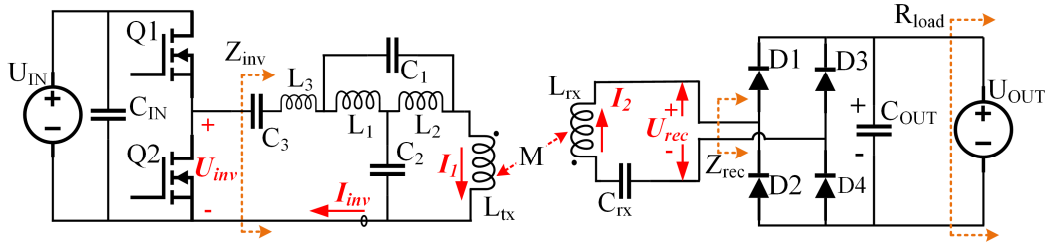


Fig. 1. Circuit diagram of the proposed inductive charger.

2.2 Efficiency Improvement Techniques

There are various loss terms in an IPT system, including conduction loss and switching loss in the power converters and conduction loss in the compensation circuits. Complex relations exist among the loss terms, which adds difficulty to the maximization of system efficiency. Some key issues for improving the system efficiency are discussed below.

2.2.1 Inverter Loss Reduction

With a low on-state resistance of the MOSFETs, switching loss accounts for a noticeable proportion in the total inverter loss when the MOSFETs are hard-switched. $\text{imag}(Z_{inv})$, which is regulated via compensation circuit design, should be positive to facilitate soft switching of the inverter. On the other hand, a high power factor at the inverter output port is beneficial for reducing the inverter conduction loss. An equivalent expression for these two conditions is that $\angle Z_{inv}$ should be positive but its abstract value should be reasonably small.

2.2.2 Coil Loss Minimization

To minimize the conduction loss in coils, the RX side should be fully resonant, i.e., $\omega L_{rx} - 1/(\omega C_{rx}) = 0$, where ω is the angular operating frequency. On the other hand, the optimal $re(Z_{rec})$ is subject to the maximum-efficiency condition:

$$|I_1|^2 R_1 = |I_2|^2 R_2, \quad (1)$$

where R_1 and R_2 are the ESRs of L_{tx} and L_{rx} , respectively. A brief derivation of (1) is given here. The product of $|I_1| \cdot |I_2|$ is constant under a given P_{out} . The basic inequality states that $x^2 + y^2 \geq 2xy$, ($x > 0, y > 0$) and equality is achieved when $x = y$. Therefore, the sum of $|I_1|^2 R_1$ and $|I_2|^2 R_2$ is minimized when these two terms are equal, and the minimum value is proportional to P_{out} . Furthermore, the conditions for minimizing the coil loss can be reformulated as

$$imag(Z_{rec}) = 0, \quad (2-a)$$

$$re(Z_{rec}) = \frac{\omega M |I_1|}{|I_2|} = \omega M \sqrt{\frac{R_2}{R_1}}. \quad (2-b)$$

2.3 Transmitter-Side Compensation Circuit Synthesis

To realize the desired power-frequency characteristic, high-order compensation circuits are necessary. Take the IPT system with series compensation circuits on both sides as an example. The limitation of low-order circuits is illustrated in Fig. 2. When R_{load} is small, the number of resonance peaks for $|I_{inv}|$ is two. With the increase of R_{load} , the resonance peaks are suppressed. By further increasing R_{load} to such a high level that the RX side is almost open-circuited, the number of resonance peaks is reduced to one. Although a monotonous power-frequency relation is obtainable in certain frequency intervals, the $\angle I_{inv}$ curve is far from satisfactory. By contrast, a higher circuit order means more resonance frequencies. Due to the interactions among the multiple resonance frequencies, it is possible to simultaneously improve the power factor and achieve a negative $\angle I_{inv}$.

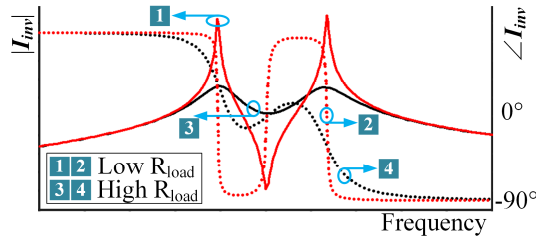


Fig. 2. Frequency characteristics of I_{inv} under different R_{load} values.

Under the premise that the RX side is fully resonant, the equivalent TX-side circuit is shown in Fig. 3, where R_{ref} denotes the reflected resistance. A general abstraction of the TX-side compensation circuit is shown in Fig. 3 (a). The number of unknown potentials (V_{out}) and unknown currents (I_{inv} and I_1) is 1 and 2, respectively, hence a 3-order circuit (π network or T network) can fully define the circuit behavior at a fixed frequency. Regardless of the actual number of reactive components, the circuit can be converted into an equivalent 3-order network, hence adopting a higher-order circuit in a fixed-frequency IPT system has no benefit from the perspective of impedance transformation.

When the frequency is variable, however, the advantage of high-order circuits is that the parameters in the equivalent 3-order network change with the frequency, which makes it possible to derive favorable frequency characteristics. Theoretically, a higher circuit order means more freedom in designing the frequency response curves. The high-order compensation circuit adopted in this work is shown in Fig. 3 (b).

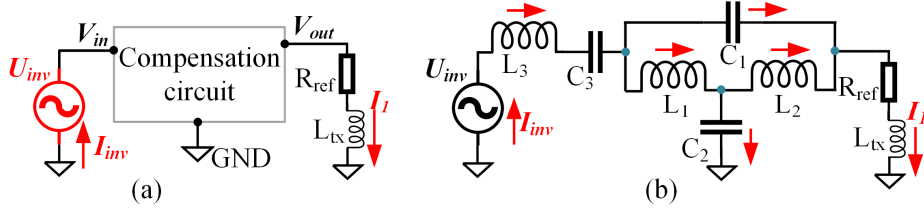


Fig. 3. Equivalent schematic of the TX-side compensation circuit. (a) General abstraction. (b) One possible realization adopted in this work.

The high-order circuit is derived by adding components to the basic T network. Three targets are pursued in the circuit design procedure. (1) The $|I_{inv}| - f$ relation in the OFB should be monotonous. (2) $\angle Z_{inv}$ should be positive and below a threshold to realize soft switching of the inverter and improve the power factor. (3) $|I_{inv}|$ should span a wide range. The following rules should be followed in the design procedure.

- No branch connecting the node V_{in} with V_{out} or with GND should contain purely inductances, otherwise high currents caused by the DC component in the inverter output voltage might occur. Similarly, to avoid high currents at harmonic frequencies, no branch between V_{in} and GND should contain purely capacitances.
- The resonance frequencies should be below the third-harmonic frequency to avoid high current responses caused by the harmonics in the inverter output voltage.
- According to the equations of Y - Δ transformation, the total impedance of the three legs in at least one Δ network or the total impedance of two legs in at least one Y network should be zero near the OFB, so that the near-resonance property leads to significant changes in the parameters of the equivalent 3-order network, which makes the frequency responses more maneuverable. Otherwise the increase of circuit order affects the frequency responses to a very limited extent. For instance, the Δ network in Fig. 3 (b) (composed of L_1 , L_2 and C_1) can be transformed into a Y network, which can be further integrated with C_2 to yield a new Y network. When the condition above is not satisfied, the 4-order network gains very limited performance improvement compared to a 3-order network.

A possible realization obtained by manual optimization is presented in Fig. 3 (b). The following analysis is based on this design. The concrete circuit parameters will be given in the subsequent parts.

2.3.1 Undamped Resonance Circuit

With R_{ref} short-circuited and all ESRs neglected, the compensation circuit is in a no-damping state. Resonance is defined as a state in which the current through any of the three nodes shown in Fig. 3 (a) approaches infinity or zero. The corresponding frequencies are referred to as peak frequency and valley frequency, respectively, and it is the peak frequencies that deserve more attention because high currents are a potential cause of system failure. The number of resonance points is determined by not only the circuit order but also the circuit parameters. Generally, there exist 5 resonance frequencies for $|I_{inv}|$ in the entire frequency range, as is illustrated in Fig. 4. From the lowest to the highest, they are designated as f_1 to f_5 , respectively. At certain parameter combinations, one peak frequency and one valley frequency coincide, thereby reducing the number of effective resonance frequencies to 3. The resonance frequencies are mainly determined by the inductance and capacitance values. With the increase of frequency, $\angle I_{inv}$ is increased by 180 degrees when a valley frequency is crossed and decreased by 180 degrees when a peak frequency is crossed.

I_{inv} is divided between L_1 and C_1 , i.e., $I_{inv} = I_{L1} + I_{C1}$. When the currents through L_1 and C_1 cancel each other out, $|I_{inv}| = 0$, which corresponds to the valleys in the $|I_{inv}| - f$ curve. The cases in which either $|I_{L1}|$ or $|I_{C1}|$ equals infinity correspond to the peaks. The OFB should be located between one peak frequency and its neighboring valley frequency, so that the $|I_{inv}| - f$ relation is monotonous and $|I_{inv}|$ can span a wide range.

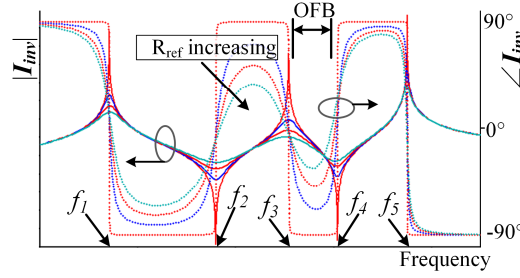


Fig. 4. Influence of damping resistance on the frequency response.

2.3.2 Damped Resonance Circuit

R_{ref} is a damping resistance in the resonance circuit. As is shown in Fig. 4, the influence of R_{ref} is straightforward: it suppresses the peaks and improves the valleys as well as smoothing the $\angle I_{inv} - f$ curve. The influence of damping is most obvious around the resonance frequencies. A higher damping resistance tends to flatten both the $\angle I_{inv} - f$ and the $|I_{inv}| - f$ curves. The former is beneficial because it means a potentially higher power factor over the OFB whereas the latter is a disadvantage because the objective of this work is to use frequency tuning as a major means of power regulation. Therefore, these two considerations should be balanced. It is noteworthy that the conclusions above are under the premise that R_{ref} is not excessively high. When R_{ref} is so high that the branch is almost open-circuited, the frequency response curve is drastically changed. In practical IPT systems, extremely high R_{ref} values hardly exist.

On the other hand, the resonance frequencies are insensitive to R_{ref} . An important concern during circuit parameter design is to achieve one valley frequency and one peak frequency near the OFB, so that even with a relatively large R_{ref} , $|I_{inv}|$ still covers a wide range. Besides, f_5 should be a peak frequency, so that $|I_{inv}|$ attenuates monotonically with frequency when $f > f_5$. Between the highest and second-highest peak frequencies (i.e., f_3 and f_5) there is a valley frequency (f_4). The OFB should be between f_3 and f_4 or between f_4 and f_5 . Considering that $\angle I_{inv}$ is highly sensitive to the variation of frequency around f_5 even when R_{ref} is large, the former frequency interval is more suitable. Another benefit of choosing the $[f_3, f_4]$ interval is that $\angle I_{inv}$ is negative. In addition, the OFB should be close to f_5 , so that the $|I_{inv}|$ response at harmonic frequencies can be effectively suppressed.

2.3.3 Circuit Response at Harmonic Frequencies

Due to the large number of resonance frequencies, the harmonics in the inverter output voltage can potentially induce high current responses in the compensation circuits, thereby posing a threat to system stability. Based on the design in Fig. 3 (b), simulation results demonstrate that all the branch currents at high frequencies are suppressed by the inductors. Therefore, the circuit response at harmonic frequencies is not a big issue unless f_5 is excessively close to the third harmonic frequency.

3 Control Strategy

Fig. 5 shows a possible control algorithm for each side. The TX side regulates P_{out} via frequency tuning. When the switching frequency (f_{sw}) has reached the upper boundary of OFB (f_{max}) but P_{out} is still above the target output power (P_{tgt}), the duty ratio of the half-bridge inverter can be decreased. Meanwhile, the DC-link voltage can also be changed (when permitted) to boost the power regulation capability. The RX-side controller is responsible for maintaining R_{load} (or $|Z_{rec}|$) at the optimal value using a power converter, e.g., a DC/DC converter. The optimal value is mainly influenced by the coil parameters [1-2], as is revealed in (2-b). However, it is noteworthy that simplifications are made in deriving (2-b), hence closed-loop feedback control is needed to maximize the system efficiency.

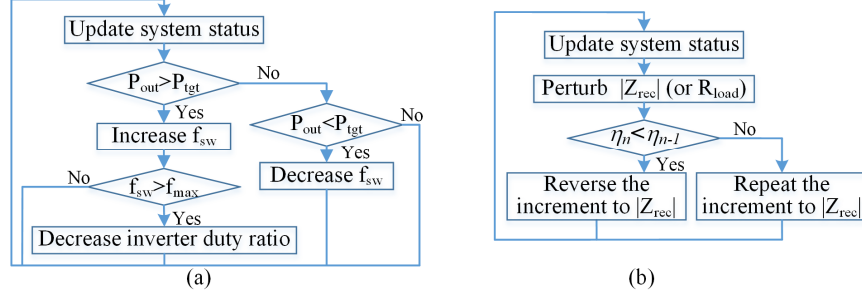


Fig. 5. Suggested control strategy. (a) TX-side control. (b) RX-side control.

4 Simulated and Experimental Results

The circuit parameters in the IPT prototype and the simulation model are given in Table 1. In the prototype, the component values are measured using an LCR meter (HIOKI IM3536) at 110kHz.

Table1: Parameters of the compensation circuit.

	Value	ESR		Value	ESR
L_1	9.6 μ H	8.5 m Ω	C_1	107.5 nF	4.6 m Ω
L_2	11.2 μ H	9.3 m Ω	C_2	146.7 nF	5.2 m Ω
L_3	21.7 μ H	20.5 m Ω	C_3	92.5 nF	5.9 m Ω
L_{tx}	62.3 μ H	93.1 m Ω	C_{rx}	37.3 nF	12.5 m Ω
L_{rx}	60.3 μ H	89.0 m Ω	M	19.8 μ H	--

In the experiments, the maximum DC-link voltage is limited to 80V, which corresponds to $|U_{inv}| = 51V$. The optimal $re(Z_{rec})$ calculated using (2-b) at 106kHz is roughly 13.2 Ω . Considering that the forward voltage of diodes increases the equivalent $re(Z_{rec})$, 15 Ω is assigned to R_{load} , which corresponds to $re(Z_{rec}) = 12.2\Omega$.

4.1 Simulated Frequency Response

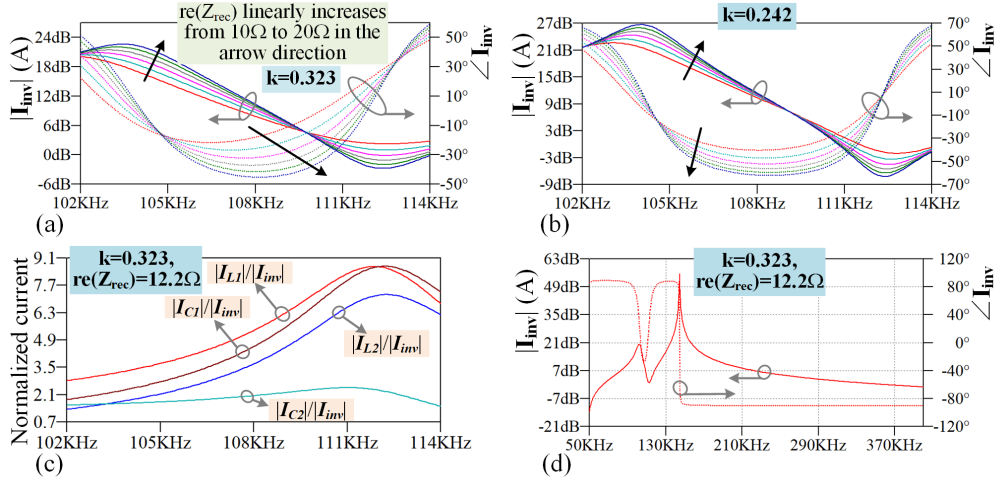


Fig. 6. Simulated frequency characteristics. (a) $|I_{inv}|$ response under $k=0.323$. (b) $|I_{inv}|$ response under $k=0.242$. (c) Currents in the reactive components normalized with respect to $|I_{inv}|$. (d) $|I_{inv}|$ response in a wider frequency range.

The simulated frequency responses obtained using the LTspice software are shown in Fig. 6. For simplicity, the DC load resistor together with the rectifier is replaced by an AC load resistor. Figs. 6 (a) and (b) reveal that increasing $re(Z_{rec})$, i.e., the AC load resistance, has a similar impact as decreasing R_{ref} , hence increasing

R_{load} is a practical means for expanding the P_{out} range. A comparison between these two plots shows that a lower mutual inductance also results in a wider P_{out} range. However, a wider P_{out} range is accompanied by a lower overall power factor. Another conclusion derived from the comparison is that the coupling coefficient varying within a relatively narrow range has no obvious effect on the controllability of P_{out} .

A monotonous power-frequency relation is obtainable in certain frequency intervals. Although $|I_{inv}|$ starts to increase after f_{sw} exceeds a threshold value (f_{th} , not included in the plots), it is observed that P_{out} continues to decrease. Due to the low power factor and the hard switching of MOSFETs, the efficiency is unacceptably low when $f_{sw} > f_{th}$, which makes the frequency range above f_{th} unfavorable. The frequency interval [103.2kHz, 112kHz] is a good choice for OFB.

Fig. 6 (c) presents the frequency characteristics of the branch currents normalized with respect to $|I_{inv}|$. To reduce ESR losses, high-Q components should be adopted, especially for L_1 , L_2 and C_1 . The $|I_{inv}|$ response curve within a wider frequency range is given in Fig. 6 (d), which demonstrates that the harmonic suppression capability is quite acceptable.

4.2 Experimental Results

The experimental setup is shown in Fig. 7. The MOSFETs are DMTH10H025LK3. The maximum drain-source voltage is 100V and the drain-source on-state resistance has a typical value of 17.1m Ω when the gate-source voltage is 10V. The coils are made of 0.1mm*250strand Litz wires. The TX and RX coils have a size of 185mm*185mm and are separated by 60mm air gap. The turn number is 11 for both coils. High-Q film capacitors are adopted in the compensation circuits. The inductors are also made of 250-strand Litz wires (2 wires in parallel). All ferrite objects, including the inductor core and the magnetic core in the coil assemblies, are composed of PC40 ferrite sticks measuring 60mm*15mm*5mm each. A passive rectifier composed of the body diode of DMTH10H025LK3 is adopted and the DC load resistance is fixed at 15 Ω . For simplicity, the closed-loop control strategy is not applied yet.

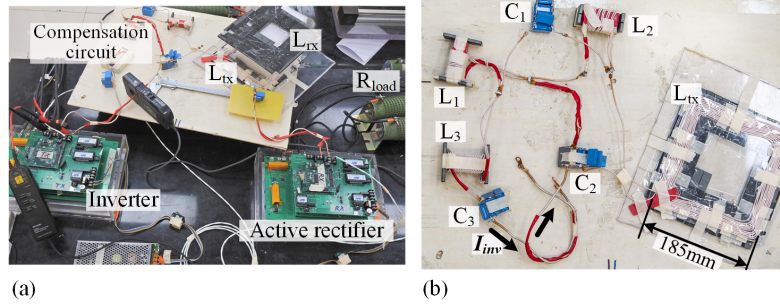


Fig. 7. Inductive charger prototype. (a) Overall configuration. (b) TX-side circuit.

The coupling coefficient in the prototype is 0.323. Fig. 8 demonstrates that the output power spans a wide interval when frequency tuning alone is adopted. The difference between prototype 1 and prototype 2 is that larger ferrite cores are utilized to fabricate the inductors in the latter, which significantly improves the system efficiency. This proves the importance of reducing the power loss in the compensation circuits. The power and efficiency data are acquired using a power analyser (HIOKI PW6001). Soft switching of the half-bridge inverter is achieved when f_{sw} is below 110kHz, as is evidenced by the voltage and current waveforms.

Comparisons between the “frequency tuning” and “ U_{IN} regulation” curves reveal that the power conversion efficiency of the compensation circuits remains stable over a wide P_{out} range. The drastic efficiency degradation at extremely light loads is caused by mainly three factors: the rise of equivalent $re(Z_{rec})$ (the forward voltage of diodes is included in calculating Z_{rec}), the higher proportion of the conduction losses in the compensation circuits (refer to Fig. 6 (c)) and hard-switching of the inverter. Considering that only a small

proportion of energy is transferred to the load resistor at extremely light-load operating points, the impact on the overall energy efficiency is acceptable.

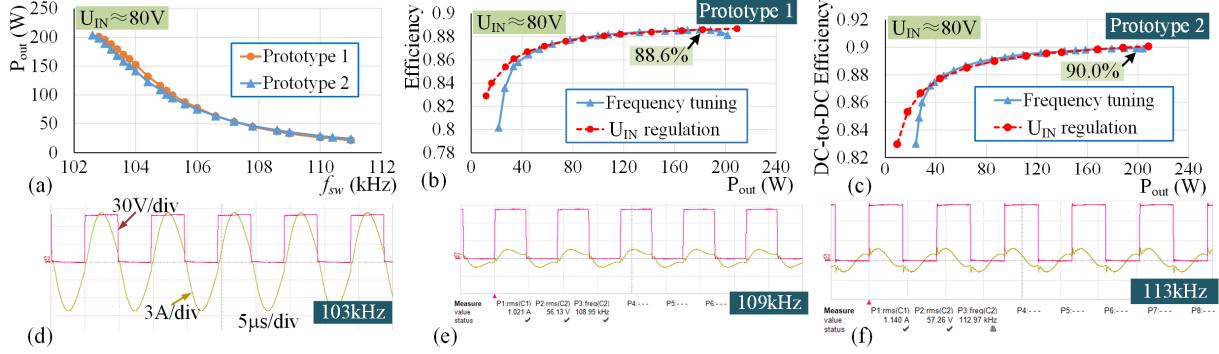


Fig. 8. Experimental results. (a) Power-frequency relation. (b) and (c) Efficiency versus power curves. (d)-(f) Voltage and current waveforms. (Note: in the “ U_{IN} regulation” cases, f_{sw} is fixed at 103.5 kHz.)

5 Conclusion and Future Work

A variable-frequency IPT system design utilizing a high-order compensation circuit on the transmitter side to gain a wide power regulation range is proposed for low-power applications where the coupling coefficient is relatively stable. The output power is controlled mainly by frequency tuning and the efficiency performance is good under full and partial loads. In future work, the coils should be miniaturized to better suit the target application. Moreover, the circuit parameters and the design of the inductors can be refined to reduce the power loss in the compensation circuits.

Acknowledgments

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Authors



Guodong Zhu was born in Zhejiang, China, in 1995. He received the B.S. degree in Automotive Engineering from Tsinghua University, Beijing, China, in 2017, where he is currently working toward the Ph.D. degree in Power Engineering and Engineering Thermo-physics. His current research interest is wireless power transfer, particularly focusing on high-power electric vehicle wireless charging technology.



Dawei Gao was born in Jilin, China, in 1971. He received the B.S. degree from Southwest Jiaotong University, Sichuan, China, in 1992 and the Ph.D. degree from North China Electric Power University, Beijing, China, in 2001. From 2001 to 2003, he was a Postdoctoral Researcher with the Department of Automotive Engineering, Tsinghua University. From 2003 to 2005, he was an Assistant Researcher. Since 2005, he has been an Associate Researcher with the same department. His research interests include DC-DC converters, electric vehicle wireless power transfer, automotive power electronics and electric drive, and electric vehicle powertrain optimization.