Design and Synthesis of a MOD 13 Binary Down Counter

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Abstract

This work explains the process of designing and synthesizing a MOD 13 binary down counter using 180 nm CMOS technology transistors. The beginning of the count is a combination of 1110(2), the end of the count is 0010(2). Simulations are made at the circuit level (transient analysis) to verify that the circuit functions correctly, then the integrated circuit layout is prepared by connecting the components manually. Finally, the layout is simulated to see how the existence of parasitic resistances and capacitances affect the output signals and it is used to estimate the maximum allowable clock frequency (fclk).

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Abstract

This work explains the process of designing and synthesizing a MOD 13 binary down counter using 180 nm CMOS technology transistors. The beginning of the count is a combination of 1110_2, the end of the count is 0010_2. Simulations are made at the circuit level (transient analysis) to verify that the circuit functions correctly, then the integrated circuit layout is prepared by connecting the components manually. Finally, the layout is simulated to see how the existence of parasitic resistances and capacitances affect the output signals and it is used to estimate the maximum allowable clock frequency (f_{clk}).

Index Terms—Digital counters, Binary counters, Flip-flops, Electronic counter, MOD 13 counter.

1. Introduction to digital counters

1.1 General overview

A digital counter is an electronic device that counts how many times a specific event occurred [1-8]. Digital counters are usually driven by a clock. The most widely used scheme is a sequential circuit consisting of flip flops and a clock signal, counters can be implemented using different types of flip flops. The outputs represent the bits for example, for a MOD-16 counter, we need 4 flip flops in a cascade, they either count up or down. Counters are widely used in different industries for different applications.

1.2 Types of digital counters

Digital counters have different kinds, each is suitable for a certain application, they can be broadly classified into two groups: synchronous counters and asynchronous (ripple) counters.

In synchronous counters, as the name indicates the flip flops share the same clock, meaning the output of each flip flop is connected to the input of the next element, an example is shown below:

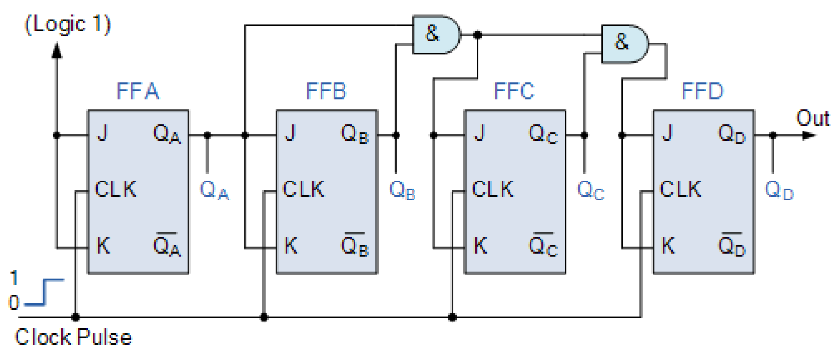

Fig 1.1 (4-bit synchronous up counter)

In contrast, asynchronous (ripple) counters work without a synchronous clock, the output of the previous flip-flop is given to the input of the following flip-flop as a clock signal which are connected in series, and the clock pulse laps through the counter. Because of the ripple clock pulse, it's also known as "ripple counter". Asynchronous (ripple) counters are able to generate 2^n - 1 unique binary combinations.

The two types described above are very broad categories, they can be manipulated to design tens of other counters, other classified groups include: Modulus counters, up/down counters, ring counters, Johnson counters, decade counters, binary coded decimal counters, gray-code counters.

1.3 Applications

Counters are generally used in counting applications. They measure the time interval between two instants of time or frequency of a certain signal. Many common devices like processors, calculators, clocks, ovens use some kind of digital counter. They are also used in alarms, air conditioners, car parking controllers and so on.

In addition to that, they can be used as a clock divider circuit. Modern counters usually have different features, for example presetting the counter for determining the initial step. In certain cases, they are used in machinery controls. In electronics world, counters got wide usage in multiplexer circuits, digital clocks, staircase voltage generators and analog/digital converters.

2. Design of a MOD-13 counter

2.1 The truth table

The truth table can be obtained from the counter requirement (starting at 14 and ending at 2), as shown below:

Decimal	Q3	Q2	Q1	Q0	D3	D2	D1	D0
15	1	1	1	1	-	-	-	-
14	1	1	1	0	1	1	0	1
13	1	1	0	1	1	1	0	0
12	1	1	0	0	1	0	1	1
11	1	0	1	1	1	0	1	0
10	1	0	1	0	1	0	0	1
9	1	0	0	1	1	0	0	0
8	1	0	0	0	0	1	1	1
7	0	1	1	1	0	1	1	0
6	0	1	1	0	0	1	0	1
5	0	1	0	1	0	1	0	0
4	0	1	0	0	0	0	1	1
3	0	0	1	1	0	0	1	0
2	0	0	1	0	1	1	1	0
1	0	0	0	1	-	-	-	-
0	0	0	0	0	-	-	-	-

2.2 Karnaugh-maps and output expressions

The flip-flop output expressions can be obtained using Karnaugh-maps, as following:

D3	Q1 Q0				
Q3Q2		00	01	11	10
	00	X	X	0	1
	01	0	0	0	0
	11	1	1	X	1
	10	0	1	1	1

D3 = Q3Q0 + Q3Q2 + $\mathbf{\overline{Q2}\ Q1\ \overline{Q0}}$

D2	Q1 Q0				
Q3Q2		00	01	11	10
	00	X	X	0	1
	01	0	1	1	1
	11	0	1	X	1
	10	1	0	0	0

D2 = Q2Q0 + Q2Q1 + $\mathbf{\overline{Q3}\ Q1\ \overline{Q0} + \overline{Q2}\,\overline{Q1}\,\overline{Q0}}$

D1	Q1 Q0				
Q3Q2		00	01	11	10
	00	X	X	1	1
	01	1	0	1	0
	11	1	0	X	0
	10	1	0	1	0

D1 = $\mathbf{\overline{Q3}\ \overline{Q2} + \overline{Q1}\ \overline{Q0}}$ **+ Q1 Q0**

D0	Q1 Q0				
Q3Q2		00	01	11	10
	00	X	X	0	0
	01	1	0	0	1
	11	1	0	X	1
	10	1	0	0	1

D0 = Q2 $\mathbf{\overline{Q0}}$ **+ Q3** $\mathbf{\overline{Q0}}$

$$
\begin{aligned}
D3 &= Q3Q0 + Q3Q2 + \overline{Q2}\ Q1\ \overline{Q0} \\
&= Q3\ (Q0 + Q2) + Q1\ \overline{(Q0 + Q2)} \\
&= \overline{\overline{Q3\ (Q0 + Q2) + Q1\ \overline{(Q0 + Q2)}}} \qquad = \overline{\overline{Q3} + \overline{Q0}\ \overline{Q2}\ .\ \overline{Q1\ \overline{(Q0 + Q2)}}}
\end{aligned}
$$

$$
\begin{aligned}
D2 = Q2 \cdot Q0 + Q2 \cdot Q1 + \overline{Q3} \cdot Q1 \cdot \overline{Q0} + \overline{Q2} \cdot \overline{Q1} \cdot \overline{Q0} = \\
&= Q2 \cdot (Q0 + Q1) + \overline{Q3} \cdot Q1 \cdot \overline{Q0} + \overline{Q2} \cdot \overline{\overline{\overline{Q1} \cdot \overline{Q0}}} = \\
&= Q2 \cdot (Q1 + Q0) + \overline{Q3} \cdot Q1 \cdot \overline{Q0} + \overline{Q2} \cdot \overline{(Q1 + Q0)} \\
&= \overline{\overline{\left[Q2 \cdot (Q1 + Q0) + \overline{Q2} \cdot \overline{(Q1 + Q0)}\right] + \overline{Q3} \cdot Q1 \cdot \overline{Q0}}} = \\
&= \overline{\left[Q2 \cdot \overline{(Q1 + Q0)} + \overline{Q2} \cdot (Q1 + Q0)\right]} \cdot \overline{\overline{\overline{Q3} \cdot Q1 \cdot \overline{Q0}}}
\end{aligned}
$$

$$D1 = \overline{Q3}\,\overline{Q2} + \overline{Q1}\,\overline{Q0} + Q1\,Q0$$

$$= \overline{Q3}\,\overline{Q2} + (Q1 \odot Q0) \qquad = \overline{\overline{\overline{Q3}\,\overline{Q2} + (Q1 \odot Q0)}}$$

$$D1 = \overline{(Q3 + Q2)\,.\,(\overline{Q1 \oplus Q0})}$$

$$D0 = Q2\,\overline{Q0} + Q3\,\overline{Q0} \qquad = \overline{\overline{\overline{Q0}\,(Q2 + Q3)}}$$

$$D0 = \overline{Q0 + \overline{Q2}.\overline{Q3}}$$

2.3 Implementation on circuit level

The block diagram of the MOD 13 counter is provided in fig. 2.1, all the inputs (D0, D1, D2, and D3) are realized on circuit level (using only logic gates), then in section 2.4, CMOS implementation of all the used logic gates are provided.

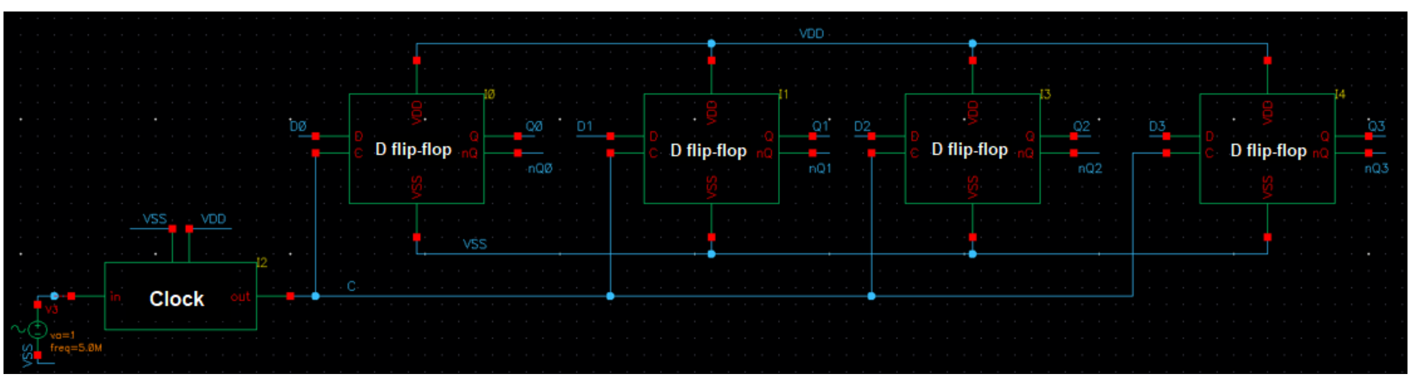

Fig 2.1 MOD 13 counter (block diagram)

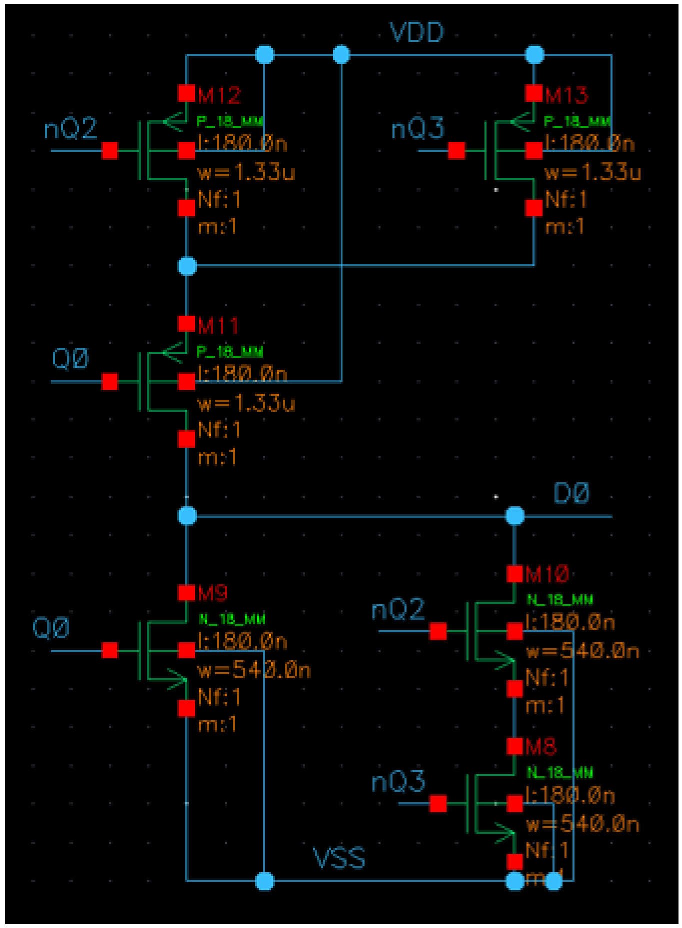

Fig 2.2 Input D0

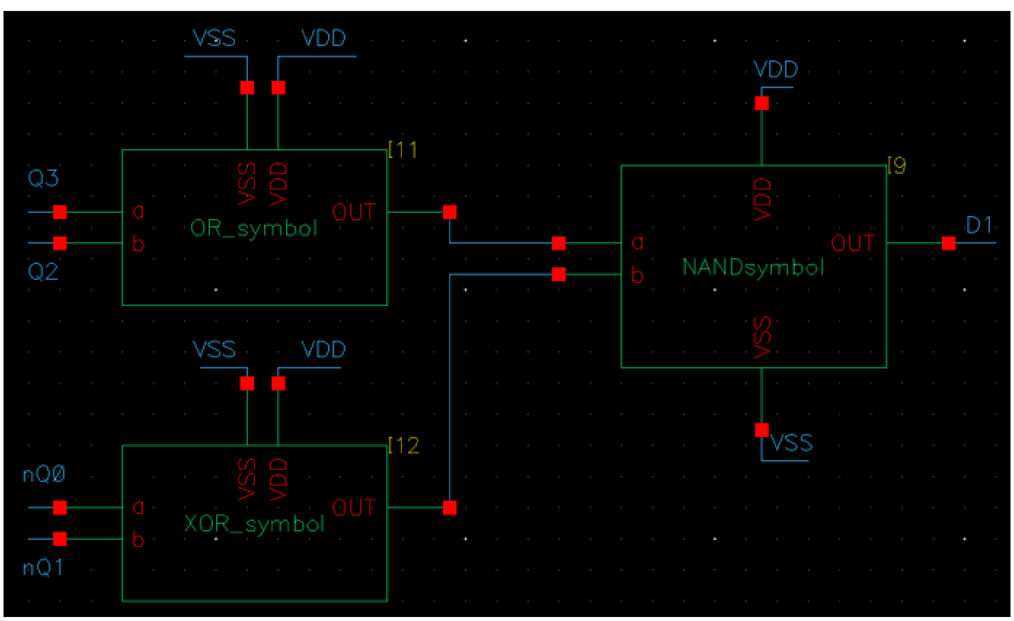

Fig 2.3 Input D1

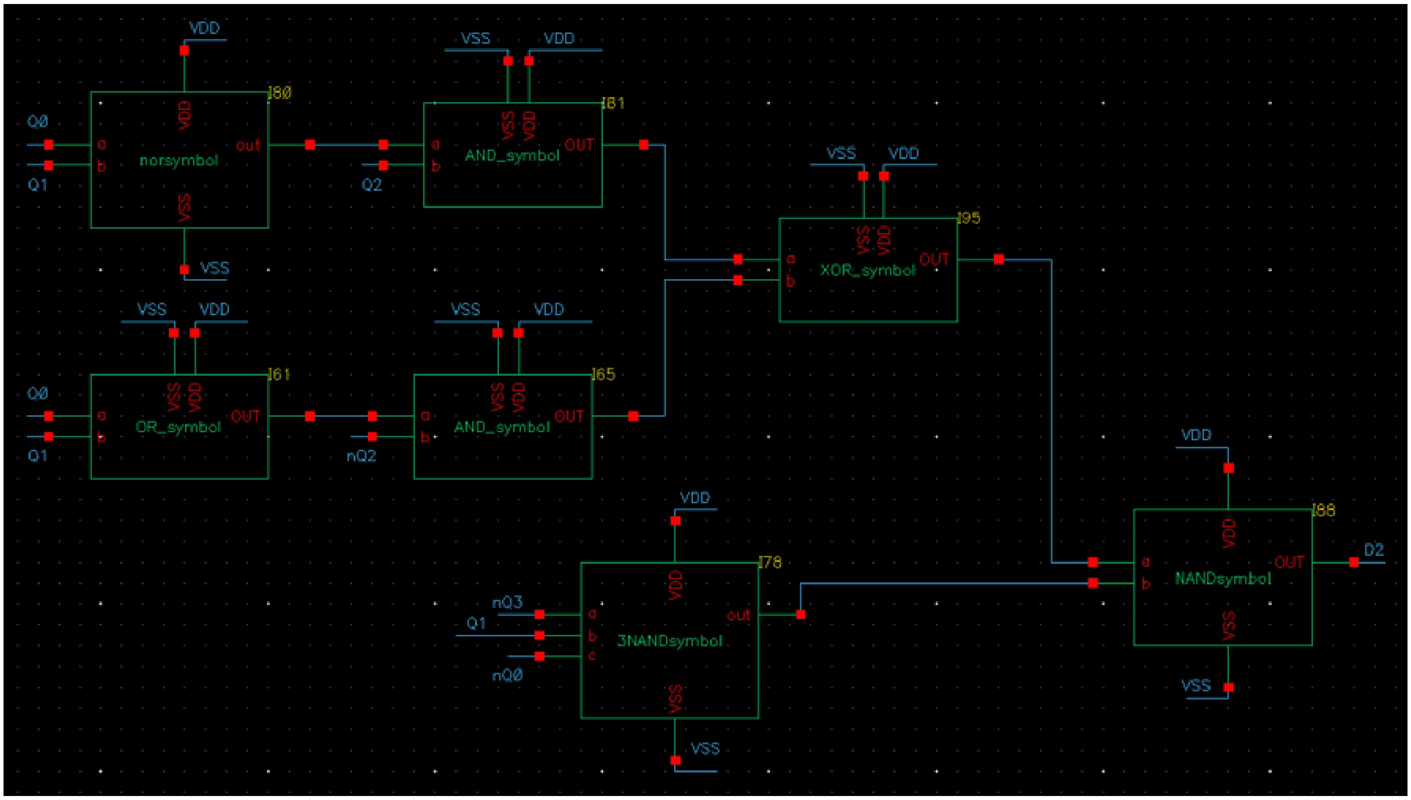

Fig 2.4 Input D2

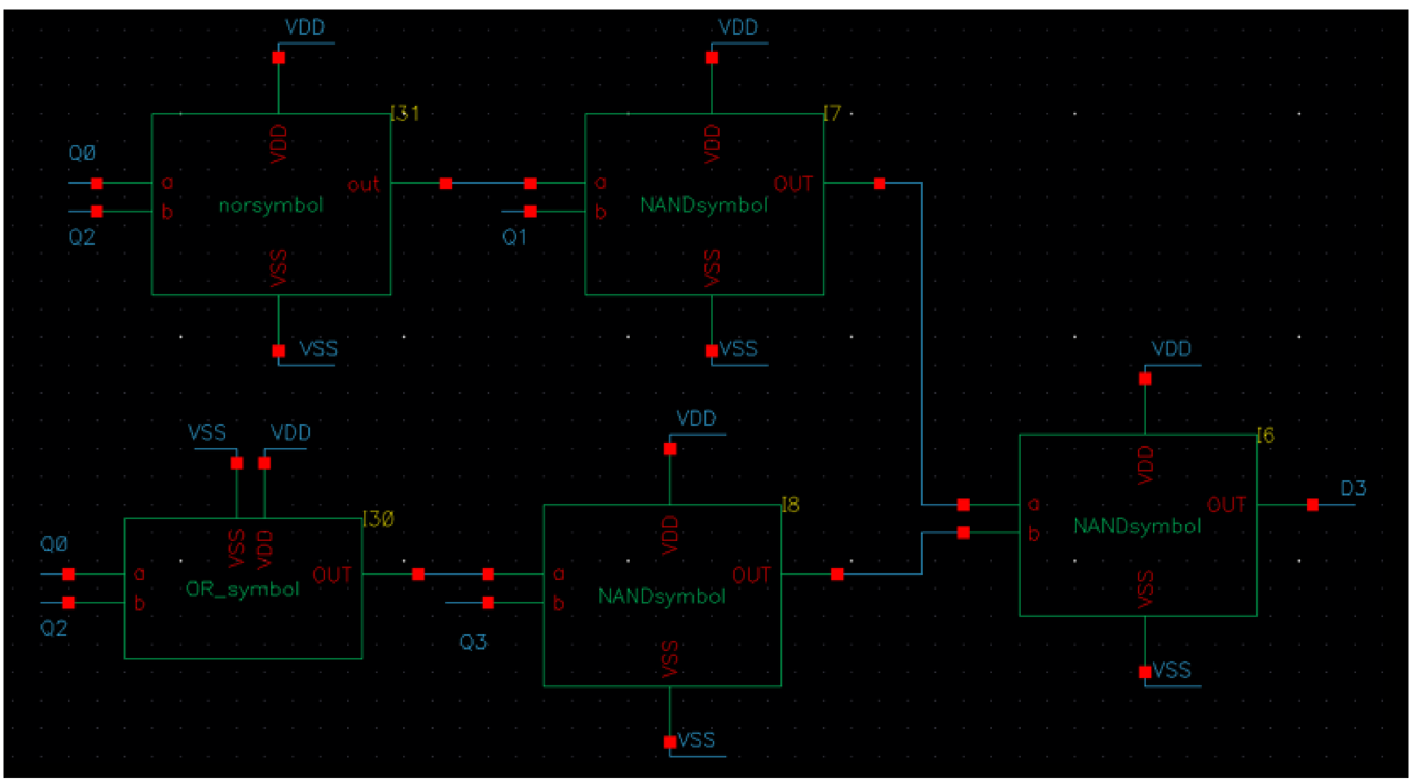

Fig 2.5 Input D3

2.4 Implementation on transistor level

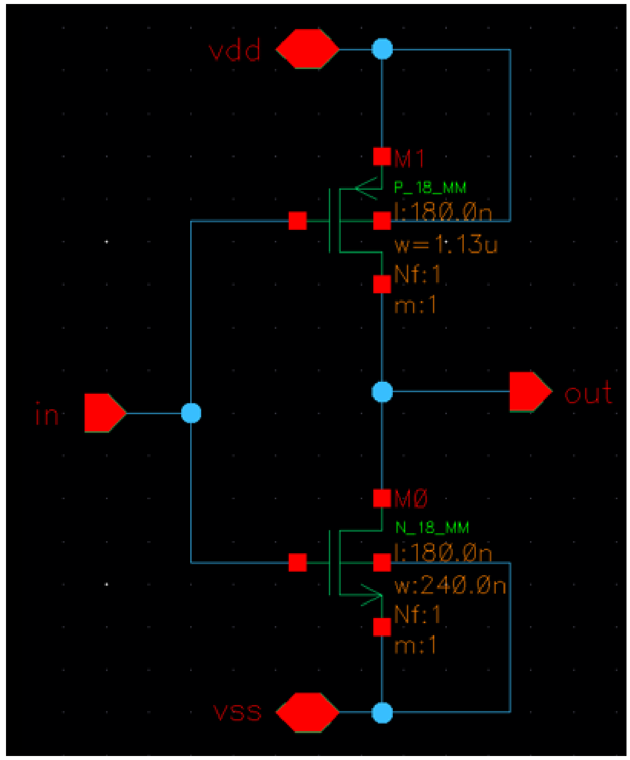

Fig 2.6 Inverter schematic

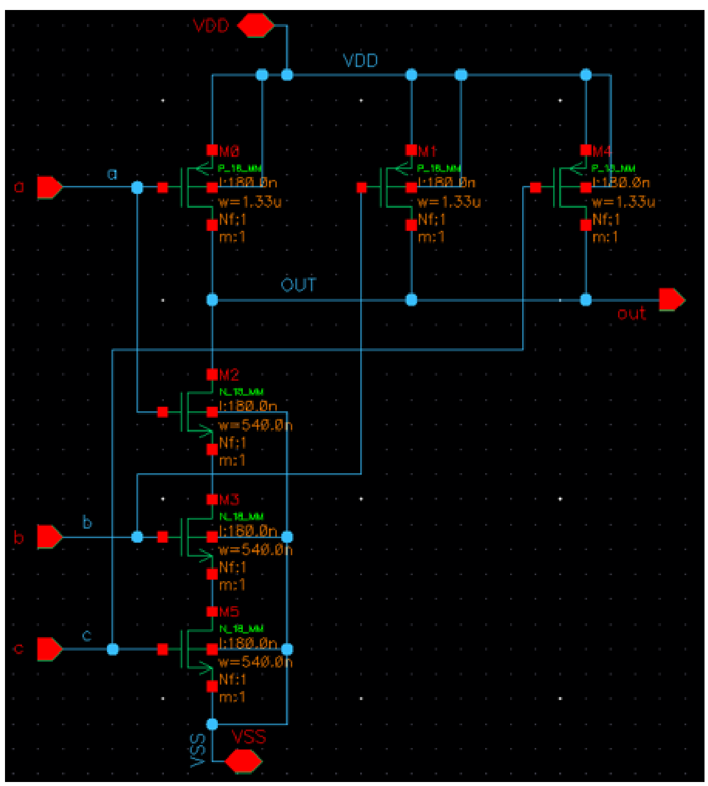

Fig 2.7 NAND gate (3 inputs)

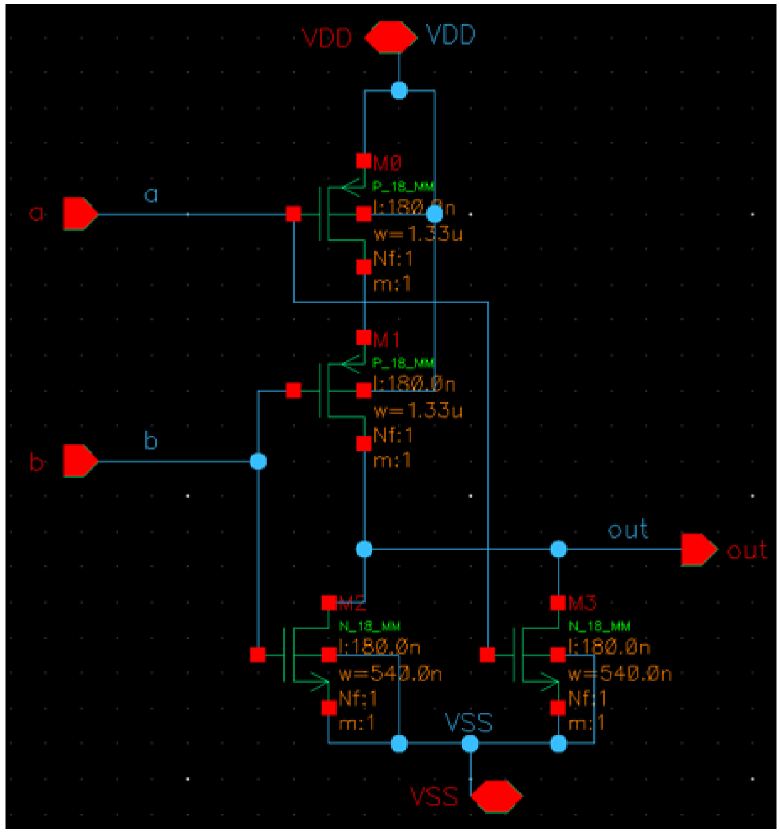

Fig 2.8 NOR gate with 2 inputs

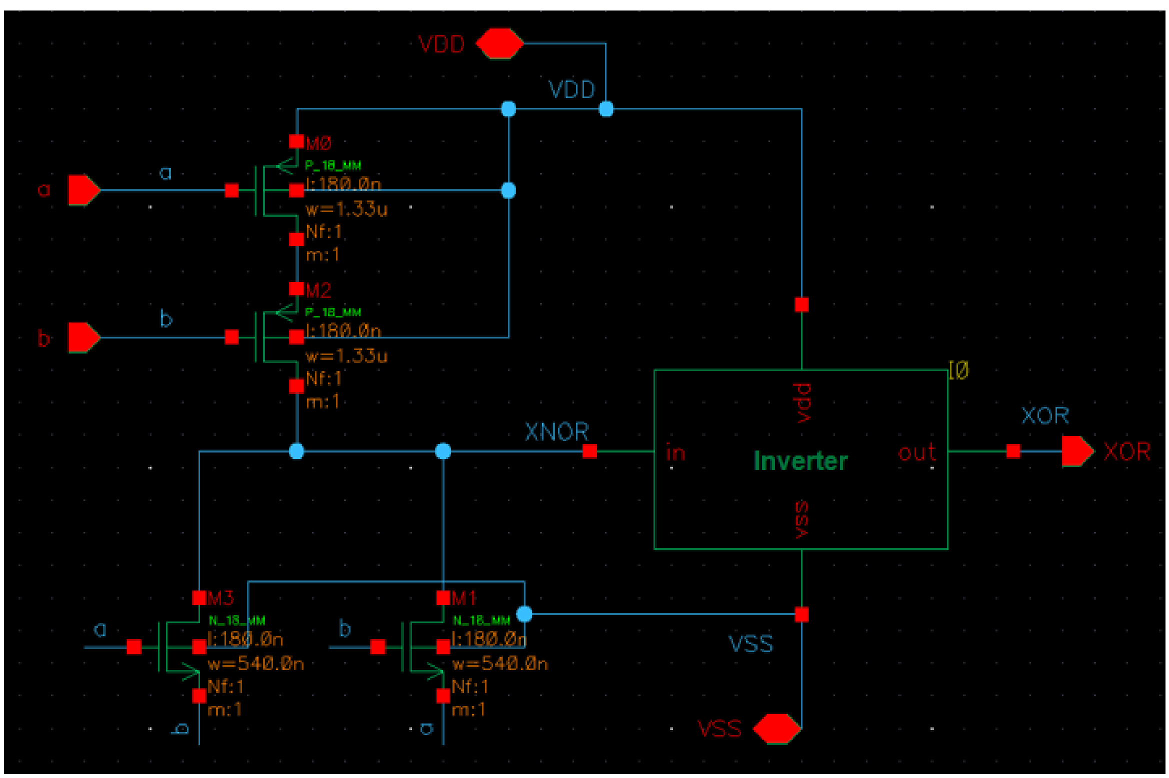

Fig 2.9 Exclusive OR gate

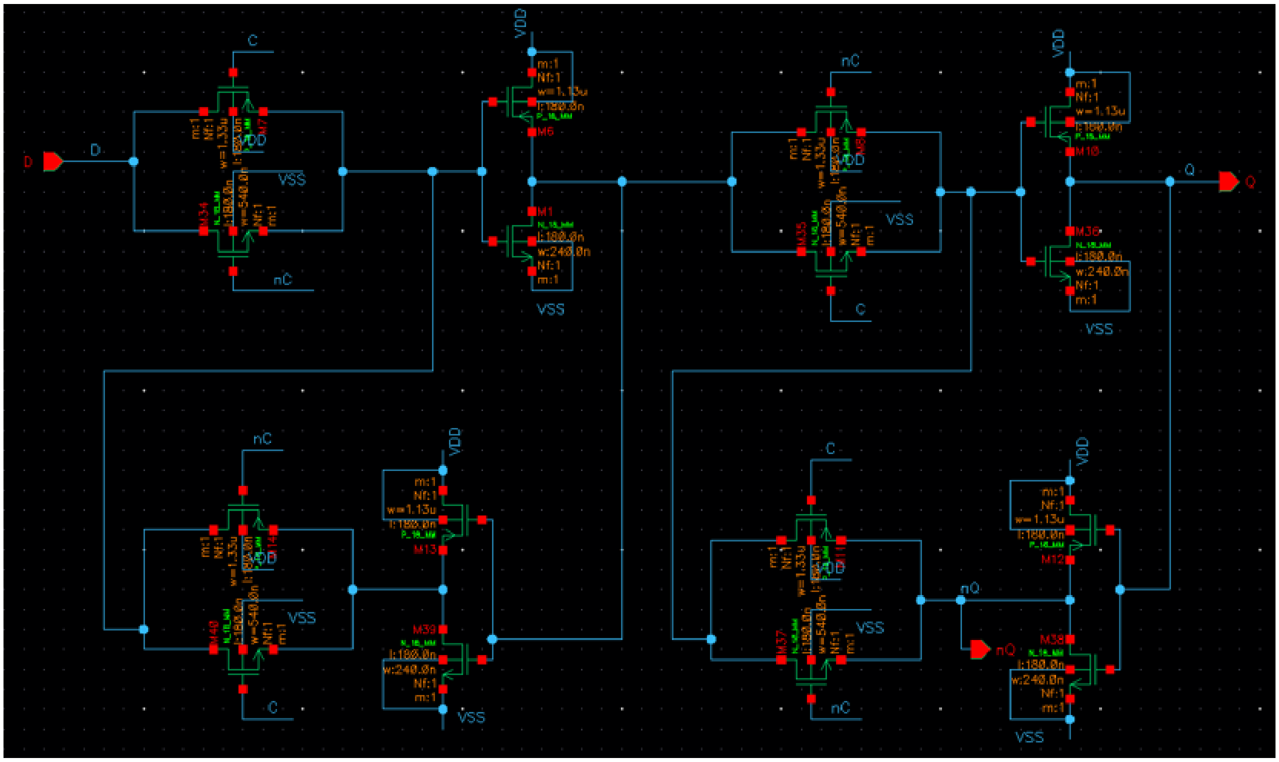

Fig 2.10 D – trigger schematic

2.5 Results

After running the simulation (LVS) the following output signals were obtained:

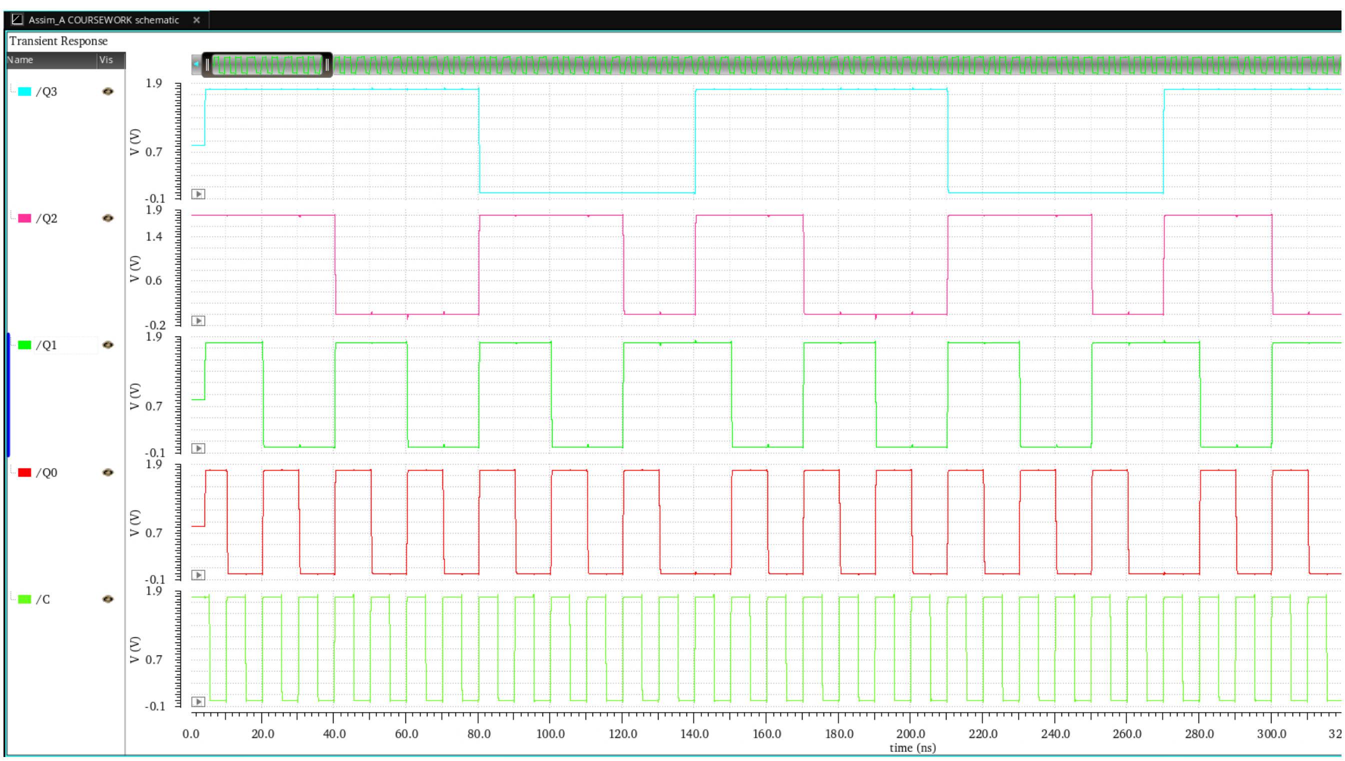

Fig 2.11 Results at clock frequency = 100 MHz

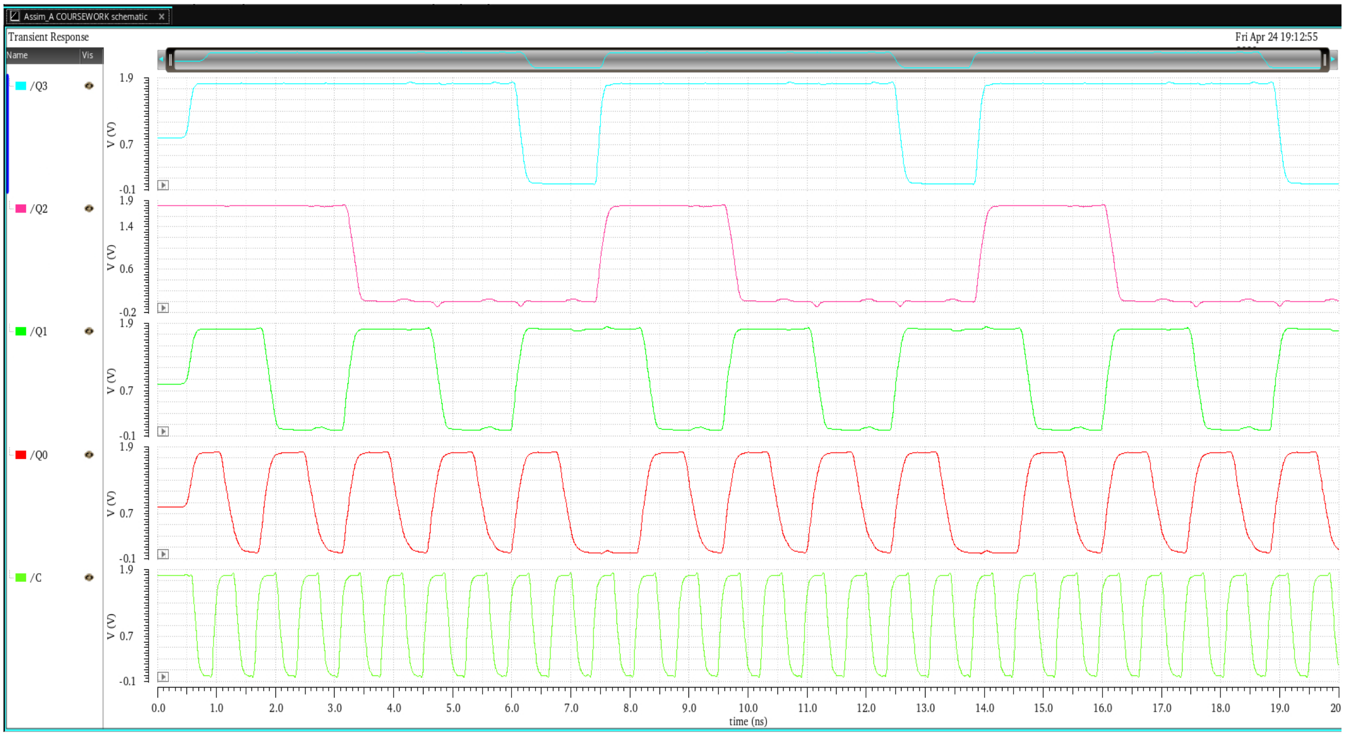

Fig 2.12 Results at clock frequency = 1.4 GHz

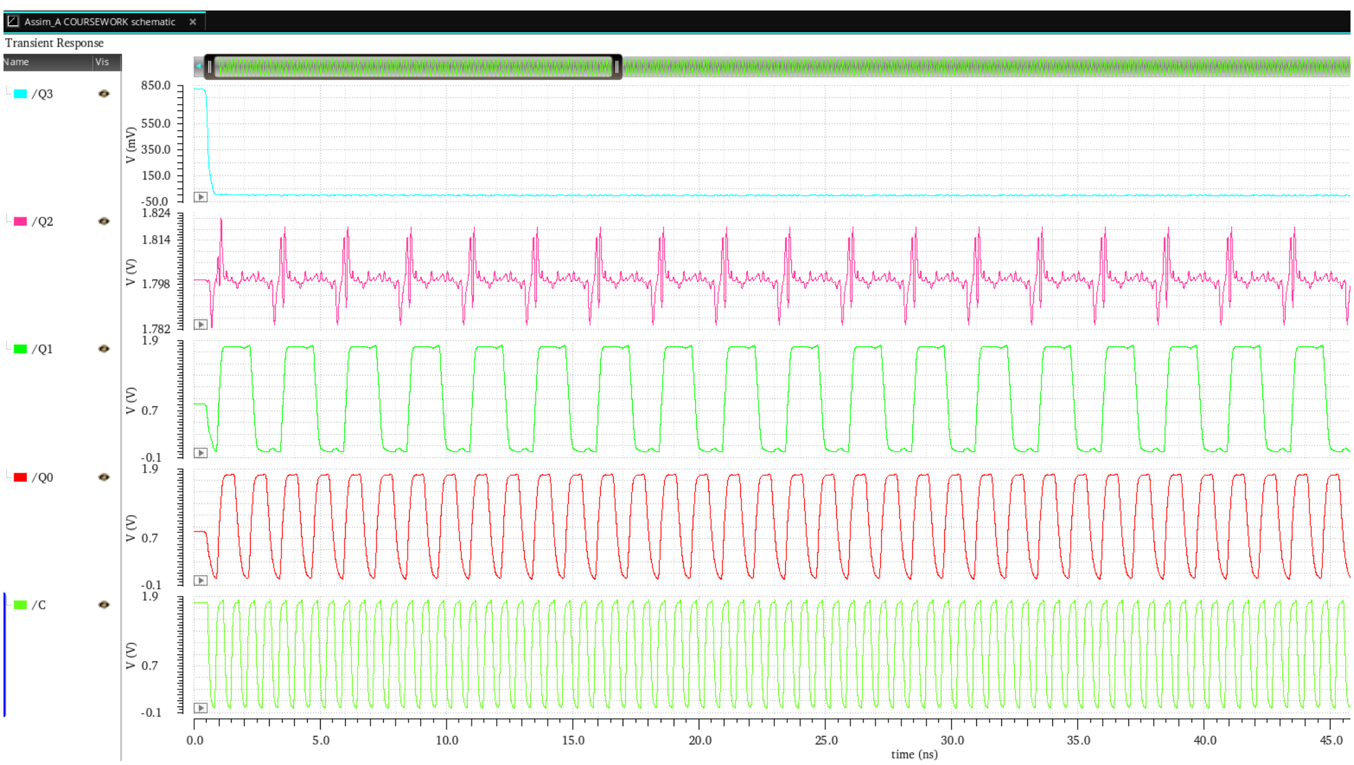

Fig 2.13 Results at clock frequency = 1.6 GHz

2.6 Layout design

In section 2.6, the layouts are prepared for the previously proposed circuits. Layout is created for each element separately, then they are connected through metals.

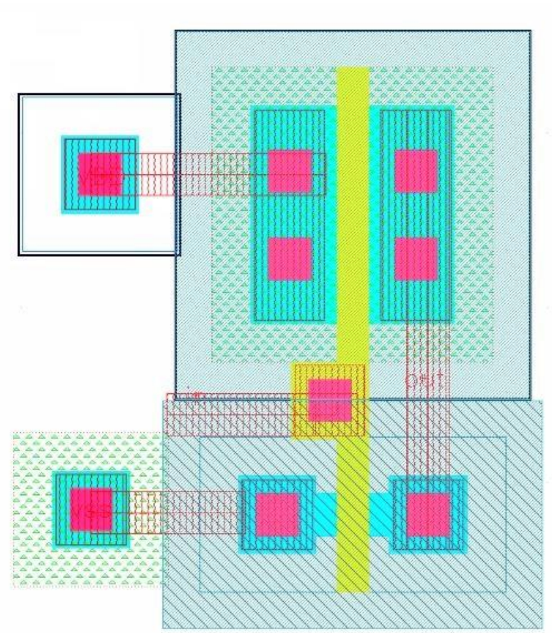

Fig 2.14 Inverter layout

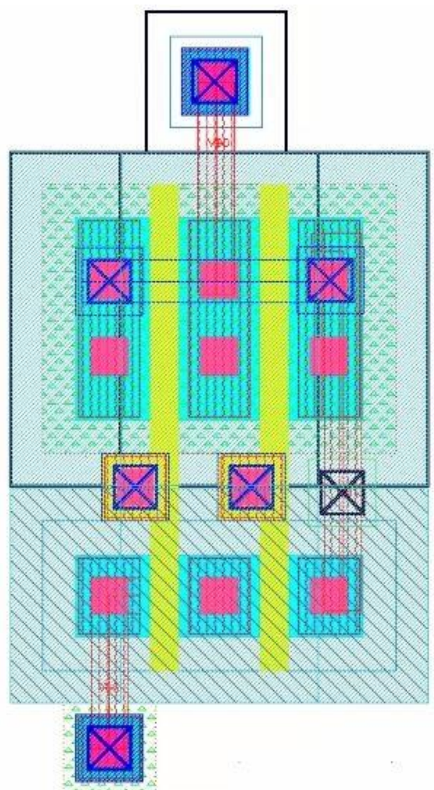

Fig 2.15 NAND2 layout

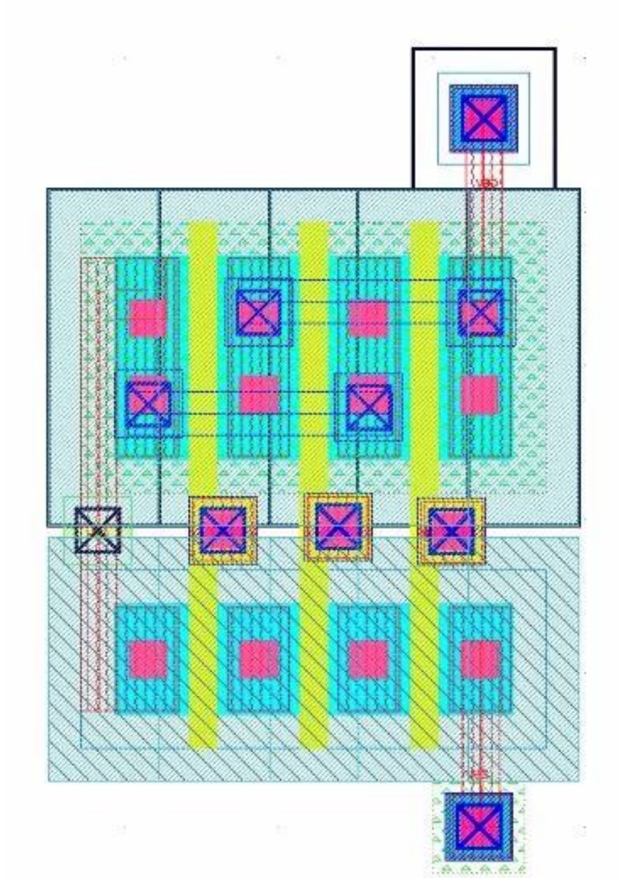

Fig 2.16 NAND3 layout

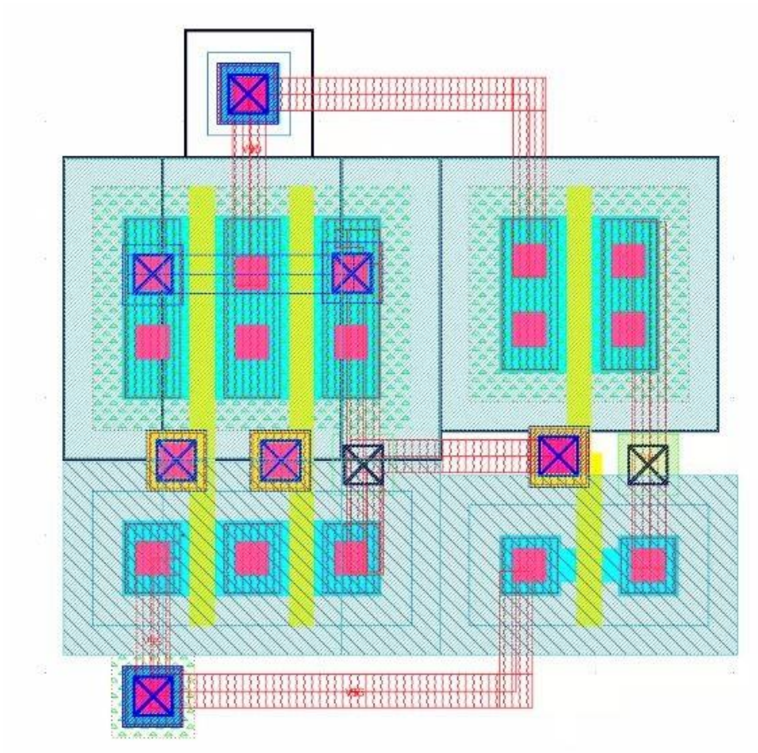

Fig 2.17 AND2 layout

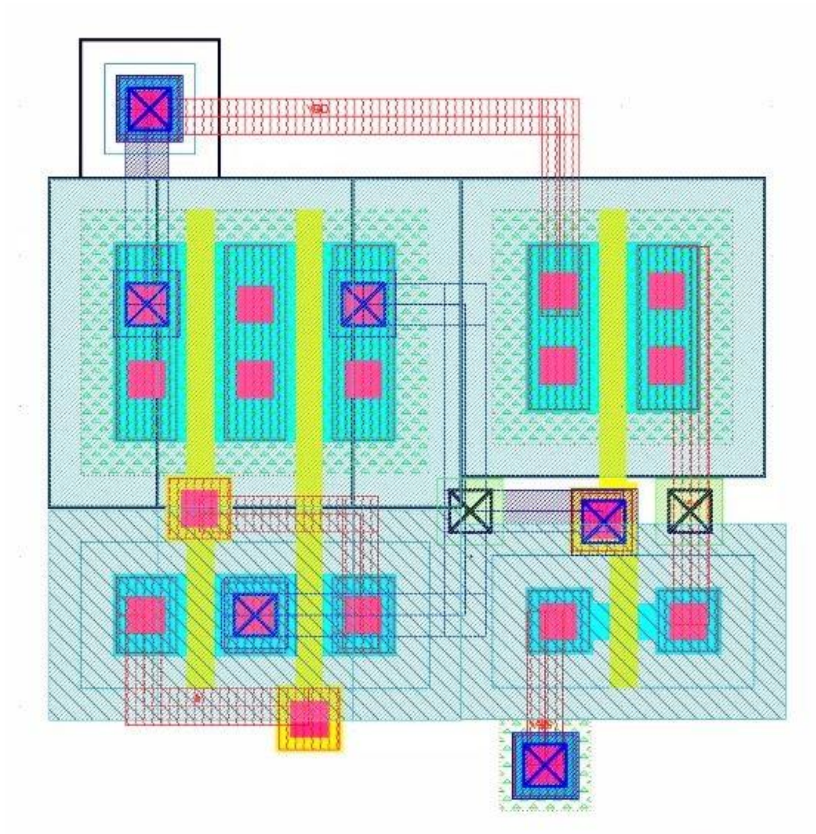

Fig 2.18 XOR layout

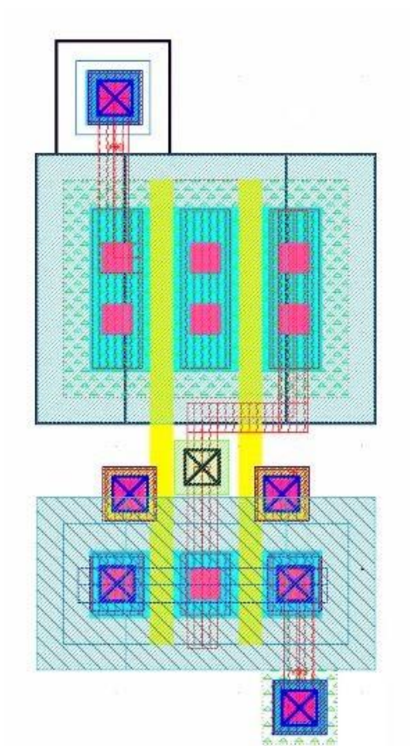

Fig 2.19 NOR2 layout

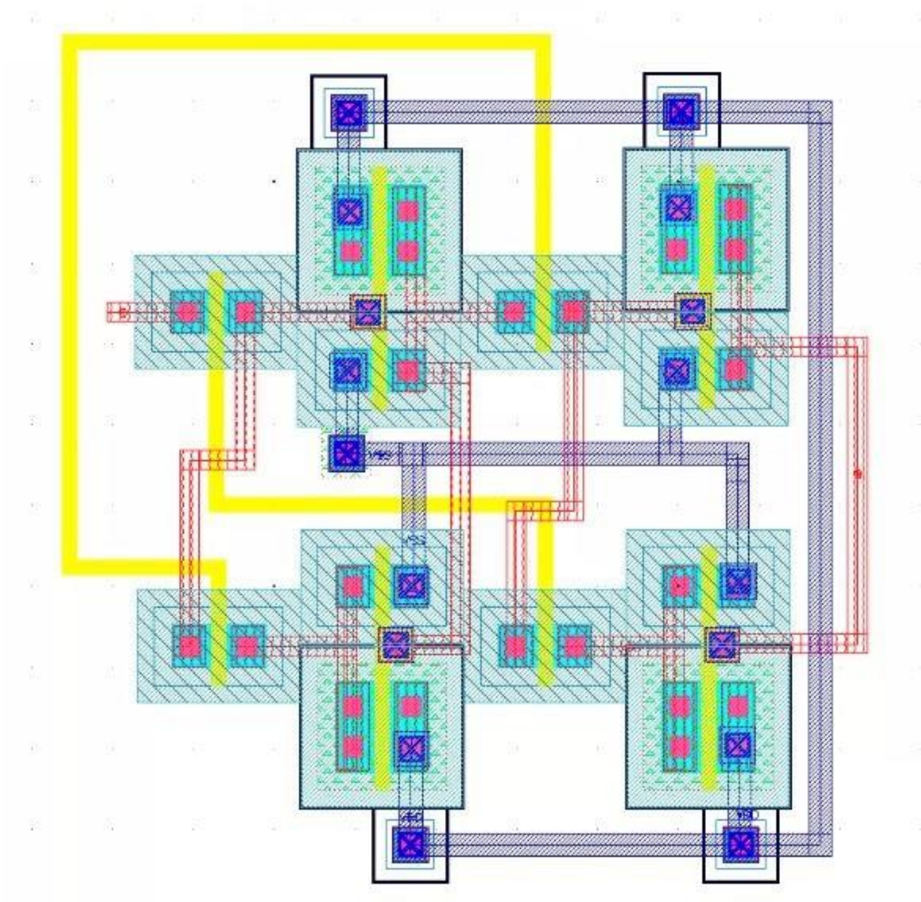

Fig 2.20 D-trigger layout

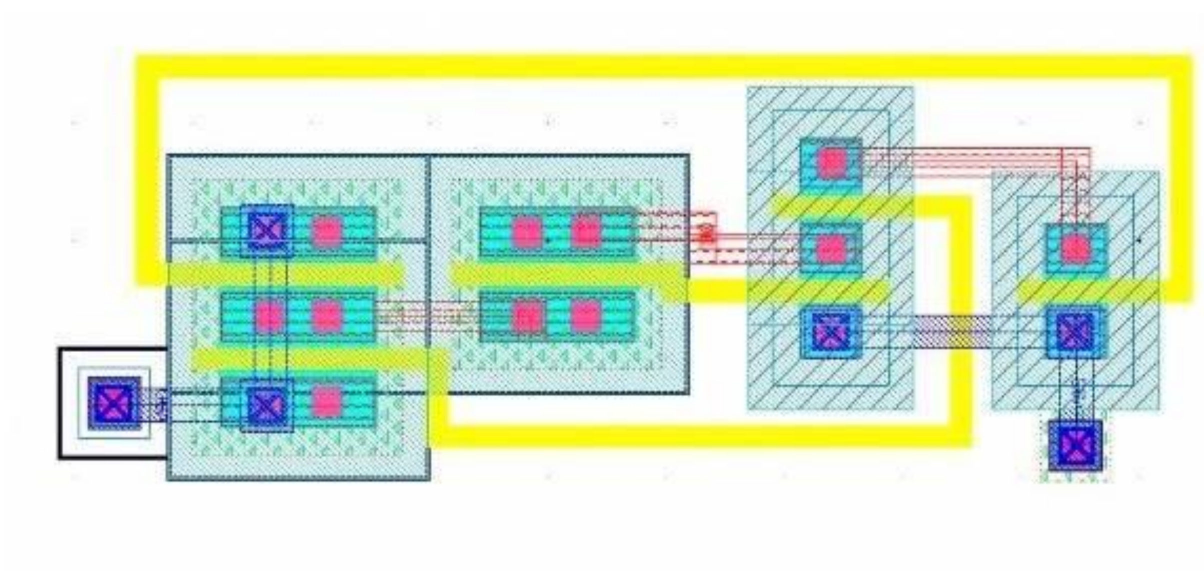

Fig 2.21 Layout of output D0

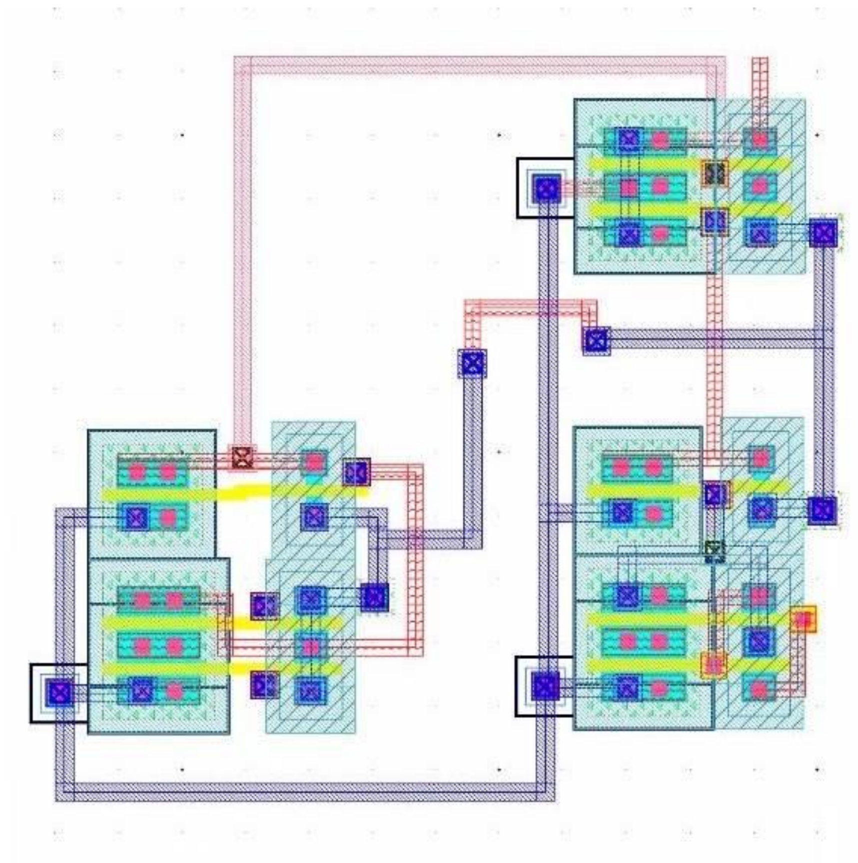

Fig 2.22 Layout of output D1

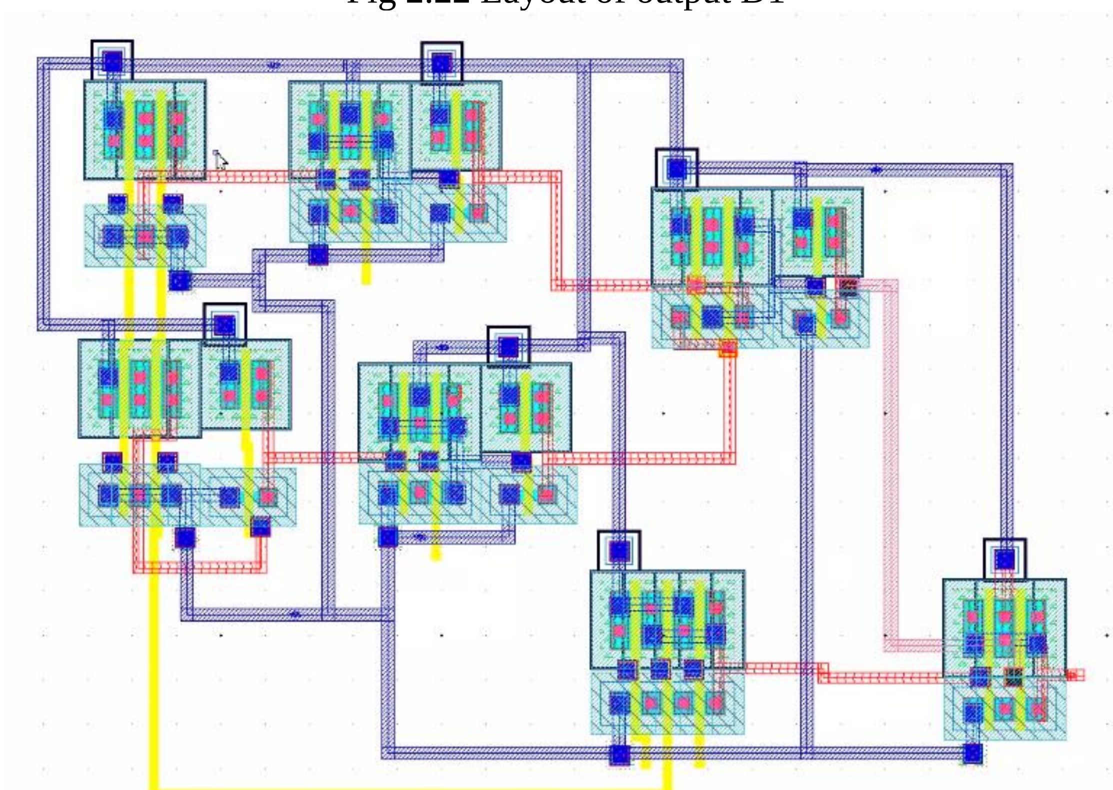

Fig 2.23 Layout of output D2

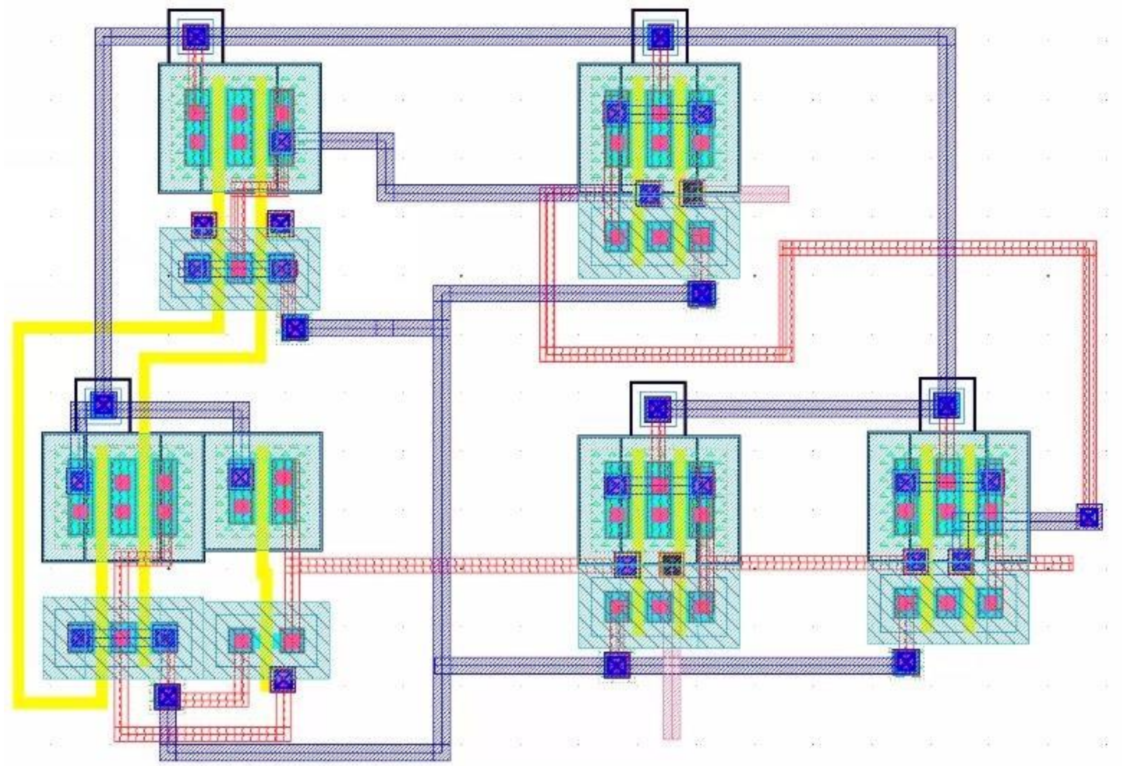

Fig 2.24 Layout f output D3

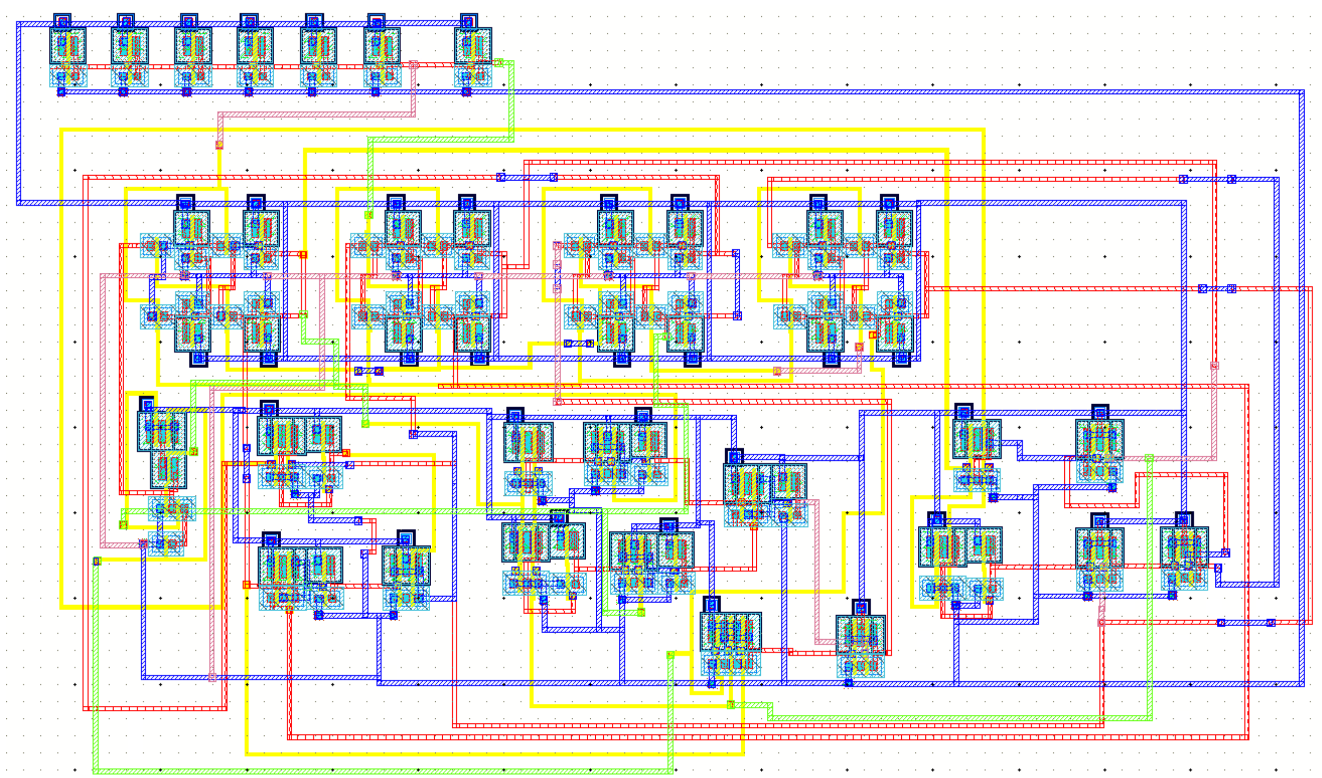

Fig 2.25 Layout of the counter

Figure 2.25 shows the complete layout of the MOD 13 counter, we may now run DRC and LVS checks to ensure everything works fine and there are no design violations.

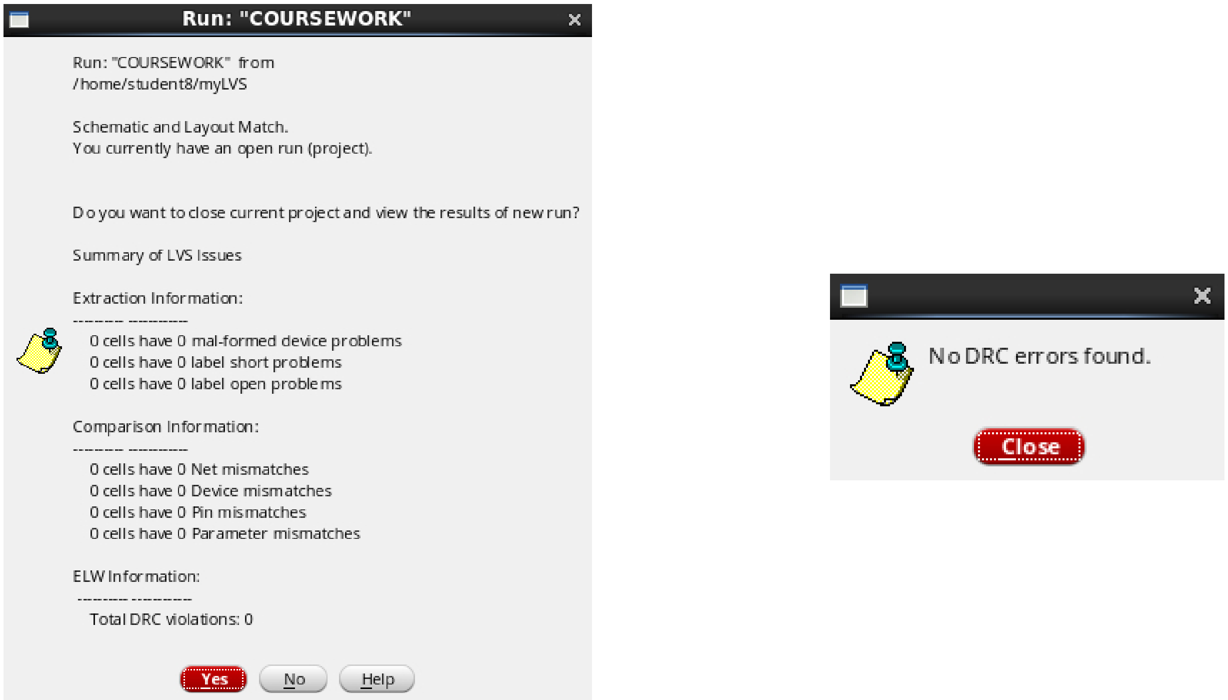

Fig 2.26 Results of DRC and LVS run

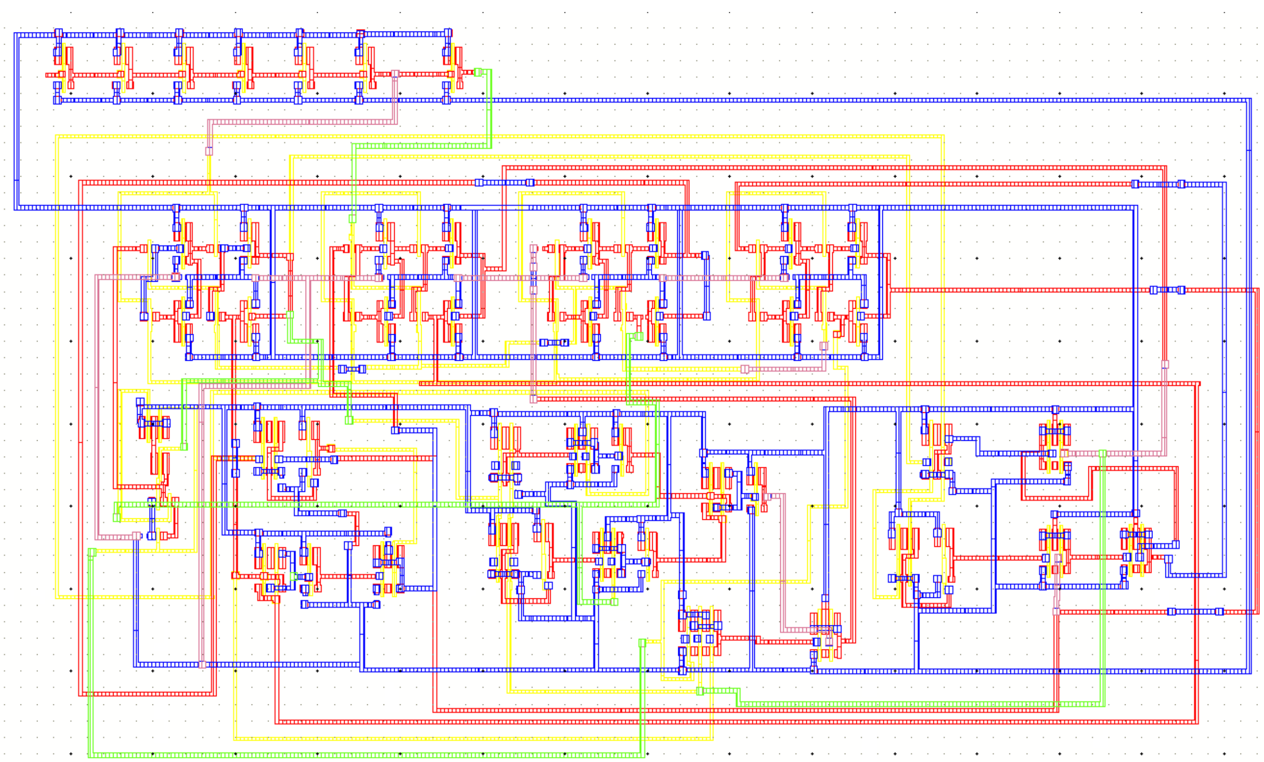

Fig 2.27 Av_extraction

Fig 2.28 Simulation at layout level (av_extracted) at clock frequency 900 MHz

Fig 2.29 Simulation at layout level (av_extracted) at clock frequency 1.4 GHz

3. Summary

The transistor sizes used in the designs are provided below:

	nMOS size	pMOS size
Inverter	180nm/240nm	180nm/1.13um
Gates	180nm/540nm	180nm/1.33um

The used VDD voltage for the entire system is 1.8 V, this is the recommended value for this type of technology.

Number of used transistors per each element after optimizing expressions are as following:

Element	Number of used transistors
Clock generator (inverters)	14
D trigger (per one)	16 x 4
D0 output	6
D1 output	16
D2 output	38
D3 output	22
Total	**160**

4. Conclusion

The design of the MOD-13 down counter was successfully implemented using UMC_CMOS 180nm technology in Cadence Virtuoso, the counter starts counting at 14 (1110_2) and ends at 2 (0010_2). The maximum operating frequency is 1.4 GHz, using clock frequency higher than this value isn't allowed because the triggers start to work improperly, and the output signals will get distorted.

Acknowledgement

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