OOC ADC: A Novel Three-Step Technique for Analog-to-Digital Conversion

Guo-Liu Zhang[1]

[1]Affiliation not available

April 29, 2024

Abstract

This paper explore the Off-on Cycle ADC (OOC ADC), an innovative analog-to-digital conversion (ADC) technique that significantly simplifies the analog-to-digital conversion process by accomplishing it through just three steps: inputting the analog signal, triggering the probe's dip-and-reset motion (PDR), and outputting the binary digital signal. Initially, the paper establishes a theoretical foundation for subsequent ADC design by introducing the Off-on Cycle principle (OOC principle) in binary encoding rules. Subsequently, it illustrates the design concepts and operational principles of the OOC ADC through the illustrative example of a 4-bit precision OOC ADC design. Finally, the paper compares the superior performance of the OOC ADC over existing ADCs in terms of conversion rate, resolution, process complexity, and power consumption. The research findings in this paper have the potential to drastically reduce the technical difficulties involved in analog-to-digital conversion, facilitate technological advancements in the realm of digital signal processing.

Introduction

Analog-to-digital converters (ADCs) occupy a pivotal position in digital technology applications, serving as the fundamental building block of modern digital systems.Despite the considerable progress made in analog-to-digital conversion technology over the past decades, incorporating technological breakthroughs such as Flash ADC(Lotfi et al., 2023), SAR ADC(Bodnar et al., 2024), Sigma-Delta ADC(Li et al., 2023), Pipeline ADC(Zhang et al., 2023), and Time-Interleaved ADC(Martens et al., 2024), among others, existing ADC methods still struggle to attain both high conversion rate and resolution due to their intricate multistep processes, protracted procedures, and demanding technical specifications. To address these limitations, this paper introduces a groundbreaking technical solution—the OOC ADC.

The OOC ADC leverages the off-on cycle principles of binary encoding rules. By harnessing this principle, the OOC ADC simplifies the analog-to-digital conversion process into three straightforward steps, significantly reducing the complexity and difficulty of the conversion. Remarkably, it manages to accomplish this simplification while simultaneously enhancing both the conversion rate and resolution.

This paper provides a detailed exploration of the technical principles, design concepts, and performance advantages of the OOC ADC, offering a fresh perspective in the field of analog-to-digital conversion. By introducing the OOC ADC, we are hopeful in overcoming the difficulty of achieving both high conversion rate (exceeding GSPS levels) and high resolution (above 24 bits) in ADC technology, and driving rapid advancements in the field of digital signal processing.

Off-on Cycle Principle

We introduce the off-on cycle principle using a 4-bit binary digital code as an illustrative example.

A 4-bit binary digital code is capable of encoding 16 distinct values, and Fig.1 presents these values sorted in ascending order of their numerical magnitude.

value	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Binary code	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
bit4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
bit3	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
bit2	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
bit1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

Figure 1: 16 Values of a 4-bit Binary Digital Code

By isolating and individually observing the numerical distributions of each bit position in Fig.1, we derive Fig.2:

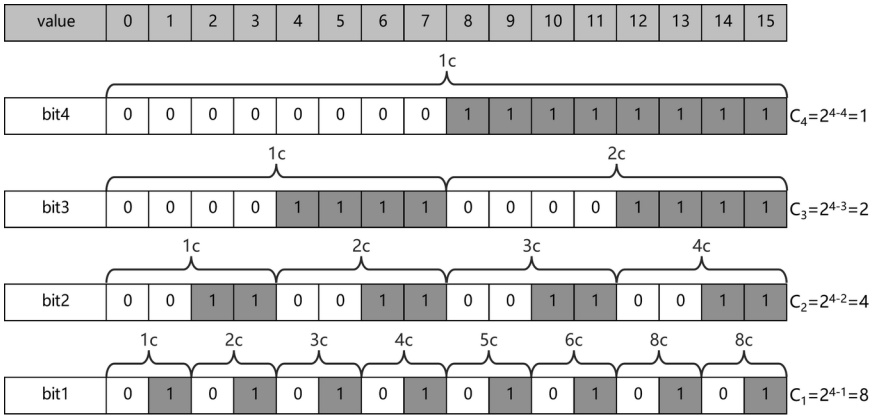

Figure 2: Off-on Cycle Pattern in Binary Encoding Rules

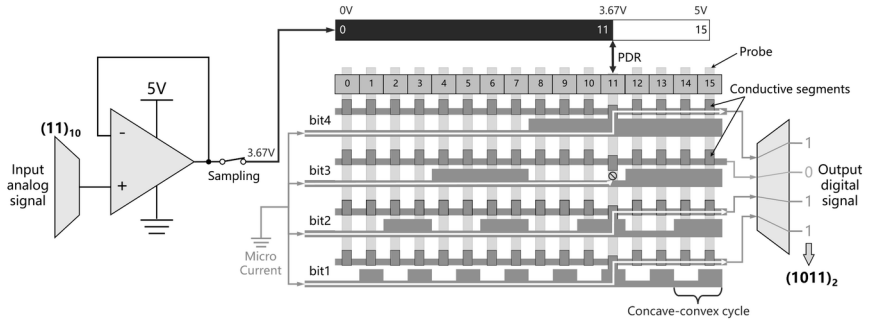

Figure 3: Circuit Diagram of OOC ADC

From Fig.2, we can observe the following patterns in the distribution of 0 and 1 values for each bit position under binary encoding rules:

1)The intervals of 0 and 1 values for each bit position alternate cyclically, and all intervals of 0 values and 1 values are equal in length for the same bit position;

2) Taking one interval of 0 values plus one interval of 1 values as one off-on cycle, the number of off-on cycles C_i for a bit position i follows the formula:

$$C_i = 2^{n-i} \tag{1}$$

where n is the total number of bits in the binary digital code.

I name the aforementioned patterns the Off-on Cycle Principle, abbreviated to OOC Principle.

OOC ADC

By leveraging the OOC Principle, we can devise an ADC capable of performing analog-to-digital conversion within just three steps. I name this type of ADC the Off-on Cycle ADC, abbreviated as OOC ADC. The design steps for the OOC ADC are as follows:

Arranging Parallel Branch Circuits

To meet the precision requirement of n bits for the OOC ADC, n parallel branch circuits need to be configured, with each circuit responsible for encoding the bit value (0 or 1) of a specific bit position.

For example, to meet the precision requirement of 4 bits, 4 parallel branch circuits are configured, as shown in Fig.3.

Setting the Number of off-on cycles for Each Branch Circuit

Each branch circuit divides the value range of the input signal into 2^{n-i} off-on cycles based on the encoded bit position i.

Fig.3 demonstrates a viable method for setting the number of off-on cycles: Each branch circuit comprises two parallel, non-contacting conductive sheets, with the lower sheet featuring alternating concavities and convexities. Each sequential pairing of a concavity and a convexity constitutes a concave-convex cycle. The number of concave-convex cycles present on the lower sheet of each branch circuit directly corresponds to the bit position it encodes.

For example, the number of concave-convex cycles for branch circuits corresponding to bits 1 to 4 are 8, 4, 2, and 1, respectively, as shown in Fig.3.

Installing the PDR Mechanism

At each encoding value position, a probe is installed, each equipped with n conductive segments, where n corresponds to the number of branch circuits. Initially, the conductive segments of the probes maintain contact solely with the upper conductive sheets of their respective branch circuits, avoiding contact with the lower sheets. Integrated within the system is a probe dip-and-reset (abbreviated as PDR) mechanism.

Upon application of a specific voltage, this PDR mechanism activates the corresponding probe to execute a dip-and-reset motion, which entails the probe's initial downward motion followed by an instantaneous return to its original position upon touching the lower conductive sheet.

For example, upon the application of a voltage of 3.67V, the PDR mechanism triggers a dip-and-reset motion of Probe 11, as depicted in Fig.3.

Each branch circuit determines its binary value (0/1) based on its electrical conduction status.

Microcurrent is supplied to the lower conductive sheet of each branch circuit, while the upper conductive sheet is linked to the circuit terminal. During the PDR, if the lower conductive sheet exhibits a convex structure at the probe's location, the branch circuit becomes electrically conductive due to the connection between the upper and lower sheets. Conversely, if the lower conductive sheet exhibits a concave structure, the branch circuit remains electrically insulated as the sheets do not connect. Activation of the terminal for a conductive branch circuit indicates an encoding value of 1, while the non-activation of the terminal for a non-conductive branch indicates an encoding value of 0.

For example, in Fig.3, the lower conductive sheets of branch circuits 1, 2, and 4 exhibit convex structures at the location of probe 11, resulting in the electrical conductivity of these branch circuits, activation of their terminals, and an output encoding value of 1. Conversely, the lower conductive sheet of branch circuit 3 exhibits a concave structure at the location of probe 11, leading to the non-conductivity of the branch circuit, non-activation of its terminal, and an output encoding value of 0.

Output the bit values of each branch circuit in bit order.

Sequentially output the bit values (0 or 1) determined for each branch circuit in Step D, adhering to their bit order. The resulting digital code constitutes the binary digital representation of the analog signal, thus marking the completion of the analog-to-digital conversion process.

For example, when the bit values of the four branch circuits in Fig.3 are output in bit order, the resulting digital code is 1011. This code corresponds precisely to the binary representation of the analog signal $(11)_{10}$, thus indicating the successful completion of the analog-to-digital conversion.

After configuring the settings as described, the OOC ADC can perform analog-to-digital conversion with the following three steps:

1. Input the voltage corresponding to the intensity of the analog signal.
2. Trigger the dip-and-reset motion of the probe that corresponds to the input voltage.
3. Each branch circuit determines its bit value based on whether it is energized and sequentially outputs the encoded bits. The resulting sequence of bits represents the binary encoding of the analog signal. The analog-to-digital conversion is then completed.

This is what is referred to as "completing analog-to-digital conversion within three steps".

Superior Performances

Compared to the currently mainstream ADC technology solutions, such as Flash ADC, SAR ADC, Sigma-Delta ADC, Pipeline ADC, and Time-Interleaved ADC,etc., the OOC ADC exhibits the following superior performances:

Possessing high conversion rates

The OOC ADC requires only the time of a single PDR for each analog-to-digital conversion, which is extremely short and can even eliminate the need for circuit holding procedures. Therefore, it can theoretically achieve a higher conversion rate than existing ADCs.

The resolution of the OOC ADC is dependent on the number of its branch circuits, and increasing the number of branch circuits does not impact the execution time of a single PDR. Therefore, enhancing the resolution of the OOC ADC does not compromise its conversion rate.

Possessing High Resolution

The OOC ADC is capable of achieving high resolution. The upper limit of its resolution is determined by the number of concave-convex cycles that can be etched onto the branch circuit for the least significant bit position. Given the current advancements in nanotechnology, the OOC ADC is theoretically capable of achieving a resolution exceeding 24 bits and even higher.

Low Process Complexity

In comparison to existing ADCs, the OOC ADC exhibits a significant advantage in terms of process complexity. Distinct from previous solutions, it does not involve intricate logical operations, thereby leading to a highly simplified logical circuit design. This simplicity not only facilitates the fabrication process but also promotes a more reliable and cost-effective manufacturing approach.

Low Power Consumption

The OOC ADC accomplishes each analog-to-digital conversion solely through a single PDR, resulting in exceptionally low energy consumption. Each branch circuit of the OOC ADC necessitates only the bare minimum power to ascertain its energized status, rendering its power draw virtually immaterial. Consequently, the OOC ADC boasts significantly low overall power consumption.

Conclusion

This paper introduces a novel ADC technology approach, namely the OOC ADC, which enables swift analog-to-digital conversion with remarkable simplicity. It offers high conversion rate, fine resolution, low process complexity, and low power consumption. The proposed scheme is poised to significantly simplify analog-to-digital conversion, ushering in technological advancements in the field of ADCs and smoothing the transition between analog and digital environments. In the future, we envision the widespread application of this technology in various fields. Furthermore, we eagerly await researchers' exploration of its potential for performance optimization and expansion into numerous additional scenarios, thereby further propelling the ADC industry forward.

References

The Fastest CMOS Single-Channel 5-bit Flash ADC Operating at 18.5 GS/s in 22 nm FD-SOI. (2023). *2023 18th European Microwave Integrated Circuits Conference (EuMIC)*, 121–124. https://doi.org/10.23919/EuMIC58042.2023.10289098

9.8 A 9.3nV/rtHz 20b 40MS/s 94.2dB DR Signal-Chain Friendly Precision SAR Converter. (2024). *2024 IEEE International Solid-State Circuits Conference (ISSCC)*, *67*, 182–184. https://doi.org/10.1109/ISSCC49657.2024.10454329

A Novel 16-bit ADC Based on Third-order - Modulator with Zero Optimization. (2023). *2023 IEEE 15th International Conference on ASIC (ASICON)*, 1–4. https://doi.org/10.1109/ASICON58565.2023.10396379

A 1-GS/s 12-bit Single-Channel Pipelined ADC in 28-nm CMOS With Input-Split Fully Differential Ring Amplifier. (2023). *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *31*(12), 1931–1938. https://doi.org/10.1109/TVLSI.2023.3323568

22.5 A 42GS/s 7b 16nm Massively Time-Interleaved Slope-ADC. (2024). *2024 IEEE International Solid-State Circuits Conference (ISSCC)*, *67*, 396–398. https://doi.org/10.1109/ISSCC49657.2024.10454361