# A Direct Current-Synchronization Control for Voltage Source Converter with Enhanced Fault Ride-Through Capability

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**Abstract**

While grid-forming (GFM) technology has gained increased attention for voltage-source converters (VSC) connected to low-inertial AC systems, there exists a gap in addressing their fault ride-through (FRT) capability under large grid disturbances. Specifically, the challenge lies in resolving the resynchronization issue of GFM-VSCs under current-limitation mode without relying on a phase-locked loop (PLL). To bridge this gap, this article proposes a novel approach called direct current-synchronization control (DCSC), which directly regulates the VSC current for synchronization. The validity of DCSC is substantiated by establishing equivalent relationships between current and power, as well as power and phase angle. Thus, achieving synchronization by controlling the VSC phase angle is made possible through the direct control of the VSC current. The stability boundary of DCSC is theoretically analyzed, concluding that DCSC has the same stability boundary as power synchronization control (PSC) with reactive power regulation in continued normal operations but a 90-degree stability boundary under large grid disturbances, irrespective of voltage magnitude. Additionally, boundary conditions for system stability assessment during large grid disturbances are established, and a control gain self-adaptability (CGSA) scheme is introduced to accelerate resynchronization after faults. Therefore, the DCSC scheme exhibits identical control dynamics to PSC with reactive power regulation in continued normal operations, while offering enhanced FRT performance under large grid disturbances. Experimental results validate the theoretical findings, affirming the effectiveness of the proposed control method.

# A Direct Current-Synchronization Control for Voltage Source Converter with Enhanced Fault Ride-Through Capability

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***Abstract*—While grid-forming (GFM) technology has gained increased attention for voltage-source converters (VSC) connected to low-inertial AC systems, there exists a gap in addressing their fault ride-through (FRT) capability under large grid disturbances. Specifically, the challenge lies in resolving the resynchronization issue of GFM-VSCs under current-limitation mode without relying on a phase-locked loop (PLL). To bridge this gap, this article proposes a novel approach called direct current-synchronization control (DCSC), which directly regulates the VSC current for synchronization. The validity of DCSC is substantiated by establishing equivalent relationships between current and power, as well as power and phase angle. Thus, achieving synchronization by controlling the VSC phase angle is made possible through the direct control of the VSC current. The stability boundary of DCSC is theoretically analyzed, concluding that DCSC has the same stability boundary as power-synchronization control (PSC) with reactive power regulation in continued normal operations but a 90-degree stability boundary under large grid disturbances, irrespective of voltage magnitude. Additionally, boundary conditions for system stability assessment during large grid disturbances are established, and a control gain self-adaptability (CGSA) scheme is introduced to accelerate resynchronization after faults. Therefore, the DCSC scheme exhibits identical control dynamics to PSC with reactive power regulation in continued normal operations, while offering enhanced FRT performance under large grid disturbances. Experimental results validate the theoretical findings, affirming the effectiveness of the proposed control method.**

***Index Terms*—Grid-forming, voltage-source converters, fault ride-through, synchronization, overcurrent protection, stability boundary.**

## I. Introduction

With the increasing integration of renewable energy sources (RES), conventional grid-following (GFL) controlled voltage-source converters (VSCs) are encountering instability issues as the power grid weakens, while grid-forming (GFM) technology is deemed a more promising solution for establishing a robust connection to a low-inertia AC grid [1],[2]. Within the realm of GFM converters, various control schemes have been proposed, including droop control [3], power-synchronization control (PSC) [4], virtual synchronous machine [5], synchronverter [6], and synchronous power controller [7]. However, existing research predominantly focuses on GFM control under continued normal operating conditions, the requirement for its fault ride-through (FRT) capability has not been thoroughly analyzed in these studies. Due to current-sensitive semiconductor devices, power-electronic-based VSCs exhibit limited overcurrent capability compared to traditional synchronous generators [8],[9]. Therefore, ensuring effective overcurrent protection under fault conditions becomes crucial for GFM converters. Besides, with the increasing installed capacity, grid-tied VSCs must remain connected to a faulted grid for a specified period, as required by various grid codes [10],[11]. This necessitates their rapid resynchronization ability with the faulted grid voltage. In essence, achieving fast resynchronization while guaranteeing that the current stays within a safety range emerges as the key requirement for the FRT capability of GFM converters under large grid disturbances.

To realize FRT capability, two aspects need attention: overcurrent protection and resynchronization. Regarding overcurrent protection, three different current-limiting methods for GFM inverters are reviewed in [12], including current limiter [13], virtual impedance [14], and voltage limiter [15]. Among them, the current limiter is the most intuitive and simplest for achieving overcurrent protection because it directly acts on current references. In contrast, the performance of the virtual impedance is sensitive to grid impedance, and designing appropriate control parameters for the voltage limiter applicable to different operating conditions is challenging [12]. Concerning the resynchronization of GFM converters with a faulted grid voltage, a typical approach is to switch the control mode from GFM to GFL when the grid fault occurs [16]. This method utilizes a current limiter for overcurrent protection and a phase-locked loop (PLL) for resynchronization [16]. However, extensive research has identified a poor stability margin of the PLL in weak grid connections, particularly during fault scenarios when obtaining the grid phase angle becomes more challenging [17]-[19]. Moreover, the wind-up issue of the integrator within control loops potentially worsens

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transient performance during the fault recovery process [20].

Aside from the approach, [21] proposed a method to synthetically modify converter power references according to the faulted grid voltage, while [22] suggested directly limiting the phase angle of the converter terminal voltage instead of current references. These methods aim to artificially create a stable equilibrium operating point during the fault, ensuring the power-synchronization mechanism still remains effective for resynchronization purposes. However, the method in [21] requires detecting the faulted grid voltage to adjust power references and involves switching power control loops between normal and fault conditions. This switching process may introduce transient disturbances and lack accuracy across various fault scenarios. Furthermore, [22] still partly relies on the PLL to acquire the phase angle of the voltage at the point of common coupling (PCC).

As discussed above, employing a current limiter stands out as the optimal approach for overcurrent protection. Simultaneously, it is advantageous for VSCs to maintain synchronization with a low-inertial AC grid without depending on the PLL. However, achieving these objectives presents a challenge for conventional GFM converters, which predominantly rely on power for synchronization [3]-[7]. This reliance can lead to a loss of synchronization under large disturbances when current references are restricted because the proportional relation between active power and power angle is destroyed [22]. To address this conflict, this article proposes a direct current-synchronization control (DCSC) law that operates directly on current for synchronization. The validity of this law is established by establishing equivalent relationships between current and power, as well as power and phase angle. Thus, a direct correlation between the converter's current and phase angle is established. In other words, synchronization through control of the VSC phase angle becomes feasible by directly regulating the VSC output current. The key contributions of this article are outlined below:

1) The control concept and structure of DCSC are proposed to address the resynchronization issue of GFM converters under current-limitation mode without utilizing a PLL.
2) The theoretical stability boundaries of DCSC under both continued normal operations and large grid disturbances are derived.
3) The stability boundary conditions to ensure a stable DCSC-based VSC-grid system are established after large grid disturbances.
4) A control gain self-adaptivity (CGSA) scheme is proposed to speed up resynchronization after large grid disturbances, which has minimal effects in continued normal operations.

In essence, the proposed DCSC scheme demonstrates identical small-signal control dynamics to the PSC scheme with reactive power regulation in continued normal operations, while exhibiting enhanced FRT performance under large grid disturbances. The effectiveness of the approach is validated through EMT simulation results.

The remainder of this article is structured as follows: Section II introduces the control concept and structure of DCSC. Section III presents the small-signal modeling of the DCSC-based VSC-grid system. Theoretical stability boundaries under both continued normal operations and large grid disturbances, along with the stability boundary condition to ensure a stable system after the fault, are derived in Section IV. Simulation results are provided in Section V, and finally, Section VI concludes the article.

## II. Control of Direct Current-Synchronization

This section introduces the control concept of DCSC, revealing the inherent relationship between the VSC current and its phase angle, as well as the control structure of the DCSC scheme.

For clarity, hereafter, boldface letters denote complex space vectors. The subscripts $abc$ and $s$ denote a vector referred to the stationary $abc$ and $\alpha\beta$ reference frames, accordingly. The subscript $dq$ represents variables in the converter reference frame, while $DQ$ represents variables in the grid reference frame. Italic letters stand for scalar variables and real transfer functions. The reference for a controlled variable is denoted by appending the subscript $r$, and a steady-state equilibrium operating point is denoted with subscript $0$. The Laplace variable $s$ is to be considered as the operator $s = \frac{d}{dt}$, where appropriate.

### A. Control Concept of Direct Current-Synchronization

To address the conflict between power-synchronization and current-limitation inherent in conventional GFM-VSCs [22], the DCSC scheme directly controls current for synchronization instead of power. This approach enables the seamless integration of a current limiter for overcurrent protection. In simpler terms, the current-synchronization law remains effective even under current-limitation mode. The validity of the DCSC can be demonstrated through the following analysis.

When operating in the VSC reference frame, the VSC current references, denoted as $i_{dr}$ and $i_{qr}$, and actual currents, denoted as $i_d$ and $i_q$, can be calculated below [23].

$$\begin{aligned} i_{dr} &= \frac{2}{3}\cdot\frac{P_r}{V}, i_{qr} = -\frac{2}{3}\cdot\frac{Q_r}{V} \\ i_d &= \frac{2}{3}\cdot\frac{P}{V}, i_q = -\frac{2}{3}\cdot\frac{Q}{V} \end{aligned} \tag{1}$$

where $P_r$ and $Q_r$ are the references for active and reactive power, respectively, and $P$ and $Q$ are the actual active and reactive power outputs from the VSC. $V$ represents the generated converter voltage magnitude.

Equation (1) plays a pivotal role in establishing the fundamental connection between current and power, aligning current references with power references and actual currents with actual powers. Leveraging this relationship allows for the regulation of active power by manipulating the current variables $i_{dr}$ and $i_d$. Besides, [4] has theoretically validated an intrinsic link between the active power of VSC and its phase angle. That is, the VSC phase angle can be controlled by regulating its active power output, which is the fundamental working principle of PSC [4]. Therefore, by bridging these relationships, the VSC phase angle can also be regulated through direct control of $i_{dr}$ and $i_d$. As a result, achieving synchronization between the VSC and an AC grid becomes feasible by directly influencing the current variables of VSC.

### B. Control Structure of Direct Current-Synchronization

The basic control loop of DCSC is depicted in Fig. 1 (a). After implementing the relationships in (1), current control loops can be established behind. Here, a circular current limiter is employed to restrain the calculated current references $i_{dr}$ and $i_{qr}$. This current limiter restricts only the magnitude of current references to $i_{dr,\text{sat}}$ and $i_{qr,\text{sat}}$ while keeping the phase angle of the current vector invariable.

$$\mathbf{i_{r,sat}} = \begin{cases} \mathbf{i_r}, |\mathbf{i_r}| \le I_m \\ \mathbf{i_r} \times (I_m / |\mathbf{i_r}|), |\mathbf{i_r}| > I_m \end{cases} \tag{2}$$

where $I_m = \sqrt{i_{dr,\text{sat}}^2 + i_{qr,\text{sat}}^2}$ represents the maximum allowable steady-state current magnitude.

In continued normal operations, the circular current limiter is transparent; it exerts effects only when the magnitude of the current vector exceeds $I_m$. The $d$-axis current error, $\Delta i_d$, is used to generate the converter phase angle $\theta$, designating the upper loop in Fig. 1 (a) as the phase angle loop (PAL). Meanwhile, the $q$-axis current error, $\Delta i_q$, determines the converter voltage magnitude $V$, thus labeling the lower loop in Fig. 1 (a) as the voltage magnitude loop (VML).

It is worth noting that only large grid disturbances that trigger the current limiter are considered as fault conditions in this article. More specifically, current-limitation mode, where $i_{dr}$ and $i_{qr}$ are saturated to $i_{dr,\text{sat}}$ and $i_{qr,\text{sat}}$ as constants. Small grid disturbances where the current limiter remains transparent, and continued normal operations, are deemed as normal conditions in this article as converter currents are still determined by (1) in both scenarios.

There is an additional term $\frac{1}{V}$ inserted into the PAL, highlighted by the red dotted line in Fig. 1 (a), named as PAL gain adapter to distinguish the denominator $\frac{1}{V}$ in (1). This gain adapter minimally affects system performance under normal conditions but brings about significant enhancements in the FRT process. The specific role of this term will be theoretically proven in Section III (B). The basic control law of DCSC is given by

$$\begin{aligned} \theta &= \left(\frac{k_p}{V}\left(i_{dr} - i_d\right) + \omega_r\right) \cdot \frac{1}{s} \\ &= \left(\frac{k_p}{V}\left(\frac{P_\text{r}}{V} - i_d\right) + \omega_r\right) \cdot \frac{1}{s} \\ V &= -k_q\left(i_{qr} - i_q\right) \cdot \frac{1}{s} + V_r \\ &= -k_q\left(-\frac{Q_\text{r}}{V} - i_q\right) \cdot \frac{1}{s} + V_r \end{aligned} \tag{3}$$

where $k_p$ and $-k_q$ represent controller gains. It is worth noting that the VML controller gain is negative. This stems from the negative nature of the transfer function $J_{iqV}(s)$ in (14), which is the AC system transfer function from $\Delta i_q$ to $\Delta V$. Within the frequency range smaller than the fundamental grid frequency $\omega_0$, $J_{iqV}(s)$ indicates that an increase in $i_q$ leads to a decrease in $V$.

Besides the basic control loop, two supplementary control blocks are incorporated: the virtual resistance (VR) block in Fig. 1 (b) and the overcurrent limitation (OCL) block in Fig. 1 (c). A high-pass filter with the gain $R_\text{vr}$ and the cutoff

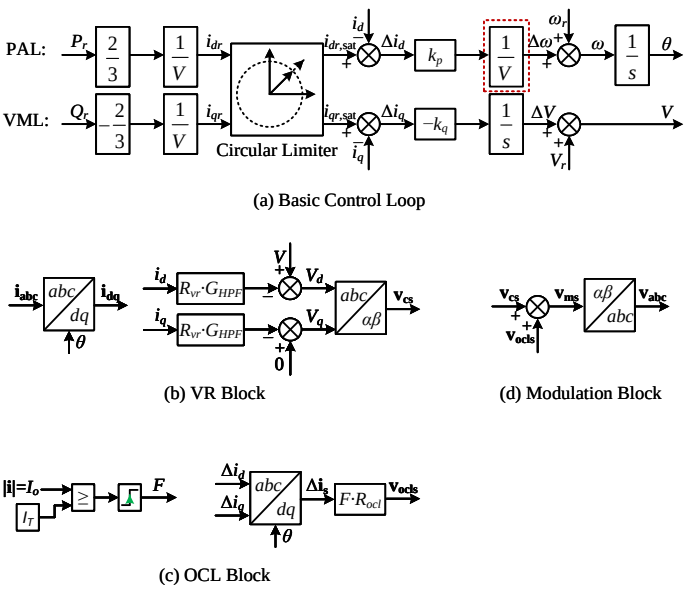



Fig. 1. Control Structure of DCSC Controller

frequency $\omega_\text{HPC}$ ($G_\text{HPF} = \frac{R_\text{vr} \cdot s}{s+\omega_\text{HPC}}$) is employed as VR to enhance system damping effect without consuming real power [4], while the OCL block is utilized to restrain transient fault overcurrent, with detailed explanations in Section II (C). The modulation block, shown in Fig. 1 (d), is used to generate the final modulation voltage vector $\mathbf{v_{abc}}$ for controlling the VSC.

### C. Overcurrent Limitation Scheme

Although the implemented current limiter can effectively bring the steady-state fault current within permissible limits, it fails to restrain transient fault overcurrent as $V$ cannot change instantaneously. This leads to a large voltage difference between the converter terminal and the grid at fault-inception and fault-clearing points, resulting in considerable transient current overshoot. As analyzed in [20], this transient overcurrent is primarily caused by a DC-bias component. Hence, a transient resistor is proven to be effective in attenuating this DC-bias component, thereby limiting transient overcurrent [20].

To safeguard power electronic devices at fault-inception and clearing points, an OCL block in Fig. 1 (c) is applied, as described in (4).

$$\mathbf{v}_\text{ocls} = F \cdot R_\text{ocl} \cdot \Delta\mathbf{i}_\text{s} \tag{4}$$

Here, $F$ is the fault flag, set to 0 under normal conditions, and to 1 when the converter current magnitude surpasses a predefined threshold $I_T$. Consequently, the OCL voltage vector $\mathbf{v_{ocl}}$ remains at 0 under normal conditions but follows the expression in (4) when a large grid disturbance occurs. $R_\text{ocl}$ represents the OCL resistance, defined the same as in [20] and expressed as:

$$R_{ocl} = \begin{cases} k_{ocl} \cdot (I_o - I_T) & \text{if } I_o \ge I_T \\ 0 & \text{if } I_o < I_T \end{cases} \tag{5}$$

Here, $I_o = \sqrt{id^2 + iq^2}$ denotes the instantaneous current magnitude. $k_\text{ocl}$ is the proportional gain, and its value is

determined in the worst-case scenario of a three-phase bolted fault [20]. [20] reveals that the operation of $R_{\text{ocl}}$ does not impact system transient stability. As an improvement over [20], instead of using $\mathbf{i}$ as the input to generate $\mathbf{v_{ocl}}$, $\Delta\mathbf{i}$ is employed. This provides double assurance that $R_{\text{ocl}}$ will exit operation when a new equilibrium is reached during the fault ($\Delta\mathbf{i} = 0$). Therefore, the implementation of the OCL block does not affect the steady-state operating point during the fault but effectively constrains transient overcurrent.

## III. Modelling of Direct Current-Synchronization

This section delves into the modelling process of the DCSC-based VSC-grid system. In addition, the functionality of the PAL gain adapter is thoroughly explained.

### A. Small-signal Modelling of VSC-grid System

#### A.1. Transfer Functions of Control Plant

The equivalent circuit of the VSC-grid system is illustrated in Fig. 2, taking into account the grid voltage vector $\mathbf{E}$, VSC voltage vector $\mathbf{v}$, and VSC current vector $\mathbf{i}$. The grid impedance is represented by an inductor $L_g$, while the equivalent inductance at the converter terminal is represented by $L_c$. The virtual resistor $R_{\text{vr}}$ is moved to the VSC terminal, and the DC link voltage $V_{\text{dc}}$ is assumed to be constant.

When a small-signal perturbation is applied to $\mathbf{v}$, the resulting expression is given by

$$\begin{aligned}\mathbf{v}(t) &= (V_0 + \Delta V(t))\, e^{j(\theta_0+\Delta\theta(t))} \\ &\approx \underbrace{V_0 e^{j\theta_0}}_{\mathbf{v}_0} + \underbrace{\Delta V(t) e^{j\theta_0} + jV_0 e^{j\theta_0}\Delta\theta(t)}_{\Delta\mathbf{v}(t)}\end{aligned} \tag{6}$$

where the prefix $\Delta$ represents a small perturbation from equilibria.

Applying the Laplace transformation to (6), the expressions for $\mathbf{v}_0$ and $\Delta\mathbf{v}$ in the frequency domain are derived as:

$$\mathbf{v}_0 = V_0 e^{j\theta_0}, \Delta\mathbf{v}(s) = \Delta V(s) e^{j\theta_0} + jV_0 e^{j\theta_0}\Delta\theta(s) \tag{7}$$

Similarly, the expressions for the current vector in the grid frame $\mathbf{i}_{\text{DQ0}}$ and $\Delta\mathbf{i}_{\text{DQ}}$ can be derived as:

$$\mathbf{i}_{\text{DQ0}} = \frac{\mathbf{v}_0 - \mathbf{E}_0}{\mathbf{Z}_0}, \Delta\mathbf{i}_{\text{DQ}}(s) = \frac{\Delta\mathbf{v}(s)}{\mathbf{Z}(s)} \tag{8}$$

Where the expressions of steady-state grid voltage vector $\mathbf{E}_0$, grid impedances $\mathbf{Z}(s)$, and $\mathbf{Z}_0$ are given by:

$$\begin{aligned}\mathbf{E}_0 &= E_0 e^{j0} = E_0 \\ \mathbf{Z}(s) &= sL + R_{vr} + j\omega_0 L,\end{aligned} \tag{9}$$

$$\mathbf{Z}_0 = \mathbf{Z}(s)|_{s=0} = R_{vr} + j\omega_0 L \tag{10}$$

Here, $L = L_g + L_c$. Substituting (7), (9), and (10) into (8) and keeping only the deviation parts results in the linearized form

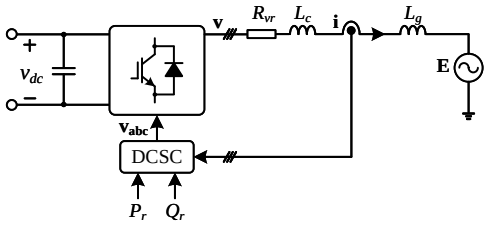



Fig. 2. Equivalent circuit of VSC-grid system for small-signal analysis.

of (8). The transfer functions of $\Delta i_D$ and $\Delta i_Q$ versus $\Delta\theta$, as well as $\Delta i_D$ and $\Delta i_Q$ versus $\Delta V$, are obtained as:

$$\begin{aligned}\Delta i_D &= V_0 \frac{\omega_0 L\cos\theta_0 - (sL + R_{vr})\sin\theta_0}{(sL + R_{vr})^2 + (\omega_0 L)^2}\Delta\theta \\ \Delta i_Q &= V_0 \frac{\omega_0 L\sin\theta_0 + (sL + R_{vr})\cos\theta_0}{(sL + R_{vr})^2 + (\omega_0 L)^2}\Delta\theta \\ \Delta i_D &= \frac{\omega_0 L\sin\theta_0 + (sL + R_{vr})\cos\theta_0}{(sL + R_{vr})^2 + (\omega_0 L)^2}\Delta V \\ \Delta i_Q &= \frac{-\omega_0 L\cos\theta_0 + (sL + R_{vr})\sin\theta_0}{(sL + R_{vr})^2 + (\omega_0 L)^2}\Delta V\end{aligned} \tag{11}$$

Utilizing the rotation transformation in (12), the current dynamics in the grid frame can be converted into the converter frame. Therefore, the Jacobian transfer matrices that describe the dynamics of the DCSC control plant are given by (13), where the AC system transfer functions from $\Delta i_d$ to $\Delta\theta$, $\Delta i_q$ to $\Delta\theta$, $\Delta i_d$ to $\Delta V$, and $\Delta i_q$ to $\Delta V$ are expressed as $J_{id\theta}(s)$, $J_{idV}(s)$, $J_{iq\theta}(s)$, and $J_{iqV}(s)$ in (14), accordingly.

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_D \\ i_Q \end{bmatrix} \tag{12}$$

$$\begin{bmatrix} \Delta i_d \\ \Delta i_q \end{bmatrix} = \underbrace{\begin{bmatrix} J_{id\theta}(s) & J_{idV}(s) \\ J_{iq\theta}(s) & J_{iqV}(s) \end{bmatrix}}_{\mathrm{J}(s)} \begin{bmatrix} \Delta\theta \\ \Delta V \end{bmatrix} \tag{13}$$

$$\begin{aligned}J_{id\theta}(s) &= I_{q0} + \frac{\omega_0 L V_0}{(sL + R_{vr})^2 + (\omega_0 L)^2} \\ J_{iq\theta}(s) &= -I_{d0} + \frac{(sL + R_{vr})\, V_0}{(sL + R_{vr})^2 + (\omega_0 L)^2} \\ J_{idV}(s) &= \frac{sL + R_{vr}}{(sL + R_{vr})^2 + (\omega_0 L)^2} \\ J_{iqV}(s) &= \frac{-\omega_0 L}{(sL + R_{vr})^2 + (\omega_0 L)^2}\end{aligned} \tag{14}$$

#### A.2 Transfer Functions of Controller

Depending on whether $i_{dr}$ and $i_{qr}$ are constrained under normal and fault conditions, the transfer functions of the DCSC controller differ. In fault scenarios, where the fault current magnitude exceeds $I_m$, $i_{dr}$ and $i_{qr}$ are saturated to constant values $i_{dr,\text{sat}}$ and $i_{qr,\text{sat}}$. Conversely, during normal conditions, $i_{dr}$ and $i_{qr}$ are determined by (1), no longer treated as constant values. The presence of the denominator $\frac{1}{V}$ in (1) introduces additional control dynamics to the DCSC

performance. For simplifying the analysis, we first derive the transfer functions of the DCSC controller assuming constant $i_{dr}$ and $i_{qr}$. Subsequently, we adapt these transfer functions for normal conditions based on the form developed for fault conditions.

In the event of large grid disturbances, the dynamic relations between $\Delta i_d$ versus $\Delta\theta$ and $\Delta i_q$ versus $\Delta V$ are described by:

$$\begin{aligned}\Delta\theta &= -\frac{k_p}{V_0}\cdot\frac{1}{s}\cdot\Delta i_d = -G_{id}(s)\cdot\Delta i_d \\ \Delta V &= k_q\cdot\frac{1}{s}\cdot\Delta i_q = -G_{iq}(s)\cdot\Delta i_q\end{aligned} \tag{15}$$

However, when the current limiter is transparent during normal conditions, $i_{dr}=\frac{P_r}{V}$ and $i_{qr}=-\frac{Q_r}{V}$. Consequently, the dynamics of the $d$-axis and $q$-axis controller loops are given by:

$$\begin{aligned}\Delta\theta &= -\frac{k_p}{V_0}\cdot\frac{1}{s}\cdot\Delta i_d - \frac{k_p}{V_0}\cdot\frac{1}{s}\cdot\frac{P_0}{V_0^2}\cdot\Delta V \\ &= -G_{id}(s)\cdot\Delta i_d - G_{id}(s)\cdot G_{\theta V}\cdot\Delta V \\ \Delta V &= k_q\cdot\frac{1}{s}\cdot\Delta i_q - k_q\cdot\frac{1}{s}\cdot\frac{Q_0}{V_0^2}\cdot\Delta V \\ &= -G_{iq}(s)\cdot\Delta i_q + G_{iq}(s)\cdot G_{VV}\cdot\Delta V\end{aligned} \tag{16}$$

where $G_{\theta V}=\frac{P_0}{V_0^2}$ and $G_{VV}=\frac{Q_0}{V_0^2}$ are coupling factors of $\Delta V$ between PAL and VML loops.

Comparing (16) with (15), it is evident that the controller dynamics under normal conditions are not only related to current errors ($\Delta i_d$ and $\Delta i_q$) but also influenced by $\Delta V$. This, in turn, increases the coupling between PAL and VML loops.

### B. Functionality of the Gain Adapter

To speed up the resynchronization with a faulted grid voltage, the PAL gain adapter, as highlighted by the red dotted line in Fig. 1 (a), is introduced. As indicated in (15), the presence of the gain adapter does not introduce additional small-signal control dynamics to the controller performance but only alters the final controller gain of PAL to $\frac{k_p}{V_0}$, which can be simply compensated by adjusting the $k_p$ value considering the narrow variations of $V_0$ under normal conditions.

To attain an equivalent PAL gain under normal conditions, the proportional gain $k_{p1}$ of the PAL controller without the gain adapter, $G_{id1}(s)=k_{p1}\cdot\frac{1}{s}$, and the proportional gain $k_{p2}$ of the PAL controller with the $\frac{1}{V}$ term, $G_{id2}(s)=k_{p2}\cdot\frac{1}{V_0}\cdot\frac{1}{s}$, should satisfy the equation:

$$k_{p2}=V_{n0}\cdot k_{p1} \tag{17}$$

Here, the subscript $n_0$ indicates a steady-state operating point under normal conditions.

In the event of an AC-side fault causing a grid voltage sag, the new converter voltage magnitude after the fault $V_{f0}$ becomes smaller than $V_{n0}$ during normal conditions. The PAL controller with the gain adapter is then adjusted to $G_{id2}(s)=k_{p1}\cdot\left(\frac{V_{n0}}{V_{f0}}\right)\cdot\frac{1}{s}$, with its equivalent loop gain significantly larger than that of $G_{id1}(s)=k_{p1}\cdot\frac{1}{s}$ due to the $\frac{V_{n0}}{V_{f0}}$ term. Moreover, as the severity of the grid voltage dip increases, the equivalent controller gain of $G_{id2}(s)$ becomes larger, resulting in faster resynchronization with a lower faulted grid voltage value.

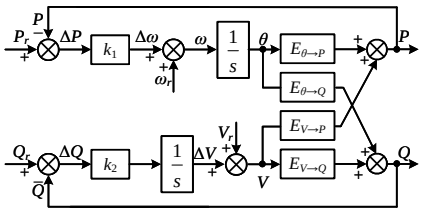



Fig. 3. Large-signal flow diagram of PSC-based VSC-grid system.

The gain adapter is a component of the PAL controller, exhibiting minimal effects under normal conditions due to the narrow variation of $V_0$, but it significantly increases the PAL loop gain during a voltage dip disturbance. This characteristic of the gain adapter is referred to as control gain self-adaptability (CGSA).

## IV. Stability Boundary of Direct Current-Synchronization

After introducing the direct current-synchronization control, it is crucial to assess its synchronization capability. [24] has revealed that the presence of right-half-plane (RHP) transmission zeros in the PSC control plant substantially affects its control bandwidth, primarily owing to the time delays introduced by the RHP zeros. Therefore, this section focuses on analyzing the stability boundaries of DCSC under both normal and fault conditions, considering the impacts caused by RHP zeros in the DCSC control plant.

### A. Stability Boundary of Power-Synchronization Control with Reactive Power Regulation

Let's begin by reviewing the conventional PSC scheme with reactive power regulation. The large-signal flow diagram of the PSC-based VSC-grid system is shown in Fig. 3. Here, $k_1$ and $k_2$ are the controller gains of PSC. $E_{\theta\to P}$, $E_{\theta\to Q}$, $E_{V\to P}$, and $E_{V\to Q}$ symbolize the large-signal equations describing the relationships from the converter phase angle and voltage magnitude to its output active power and reactive power, respectively. The small-signal control diagram of the PSC-based VSC-grid system is depicted in Fig. 4, where $G_P(s)=k_1\cdot\frac{1}{s}$ and $G_Q(s)=k_2\cdot\frac{1}{s}$ represent transfer functions of the PSC controller, while $J_{P\theta}(s)$, $J_{PV}(s)$, $J_{Q\theta}(s)$, and $J_{QV}(s)$ denote the Jacobian transfer matrices of the PSC control plant.

To obtain the transmission zeros of the PSC control plant, we can simply compute the determinant of square matrix $J_{PQ}(s)$ using (18), with solutions provided by (19) [24]. The stability boundary of the PSC-based VSC-grid system is reached when the RHP zero crosses the origin. It is evident that when $E_0=V_0=1$ p.u. and $\theta=60^\circ$, the RHP zero intersects the origin, resulting in an unstable system [24].

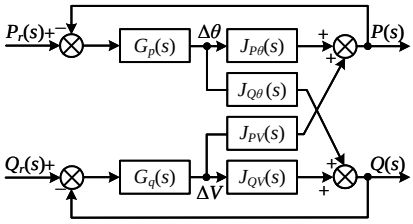



Fig. 4. Small-signal control diagram of PSC-based VSC-grid system.

$$\begin{bmatrix} \Delta P \\ \Delta Q \end{bmatrix} = \underbrace{\begin{bmatrix} J_{P\theta}(s) & J_{PV}(s) \\ J_{Q\theta}(s) & J_{QV}(s) \end{bmatrix}}_{\mathbf{J}_{\mathrm{PQ}}(s)} \begin{bmatrix} \Delta\theta_v \\ \Delta V \end{bmatrix} \tag{18}$$

$$\det\left[\mathbf{J}_{\mathrm{PQ}}(s)\right] = J_{P\theta}(s)J_{QV}(s) - J_{PV}(s)J_{Q\theta}(s) = 0$$

$$z_{1,2} = \pm\omega_0\sqrt{\frac{2E_0V_0\cos\theta_0 - E_0^2}{E_0^2 + V_0^2 - 2E_0V_0\cos\theta_0}} \tag{19}$$

### *B. Stability Boundary of Direct Current-Synchronization under Normal Conditions*

For the DCSC-based VSC-grid system, the large-signal flow diagram under normal conditions is shown in Fig. 5, where $E_{\theta\to id}$, $E_{\theta\to iq}$, $E_{V\to id}$, and $E_{V\to iq}$ describe the relationships from the converter phase angle and voltage magnitude to its output d-axis and q-axis current, respectively. For simplicity, the PAL gain adapter is omitted from the subsequent analysis in this part, as it solely adjusts the equivalent control gain PAL under normal conditions, as discussed in Section III (B).

Simplifying the original large-signal flow diagram of the DCSC-based VSC-grid system in Fig. 5 (a) yields the equivalent flow diagram depicted in Fig. 5 (d). It's important to note that except for the red-marked area, the remainder of Fig. 5 (d) mirrors the large-signal flow diagram in Fig. 3. However, the inclusion of the factor $\frac{2}{3}$ and the additional term $\frac{1}{V}$ in the red-marked area doesn't introduce additional small-signal control dynamics to the DCSC-based VSC-grid system. Rather, it only indirectly modifies the equivalent values of $k_p$ and $k_q$, considering the term $\frac{1}{V}$ as $\frac{1}{V_0}$ in small-signal modeling. Consequently, it's straightforward to achieve equivalent controller gains in both PSC and DCSC schemes by setting $k_p = \frac{3}{2}\cdot V_r \cdot k_1$ and $k_q = \frac{3}{2}\cdot V_r \cdot k_2$, assuming $V_0 = V_r$ under normal conditions.

As a result, the stability boundary of the DCSC-based VSC-grid system under normal conditions equals that of the PSC-based VSC-grid system since their control plant transfer functions remain identical. Thus, during normal conditions, the RHP zero location of the DCSC control plant is also determined by (19). For instance, if $E_0 = V_0 = 1$ p.u., the phase angle boundary of the DCSC-based VSC-grid system is $60^\circ$. Moreover, both systems exhibit similar small-signal control dynamics with proper control parameter settings.

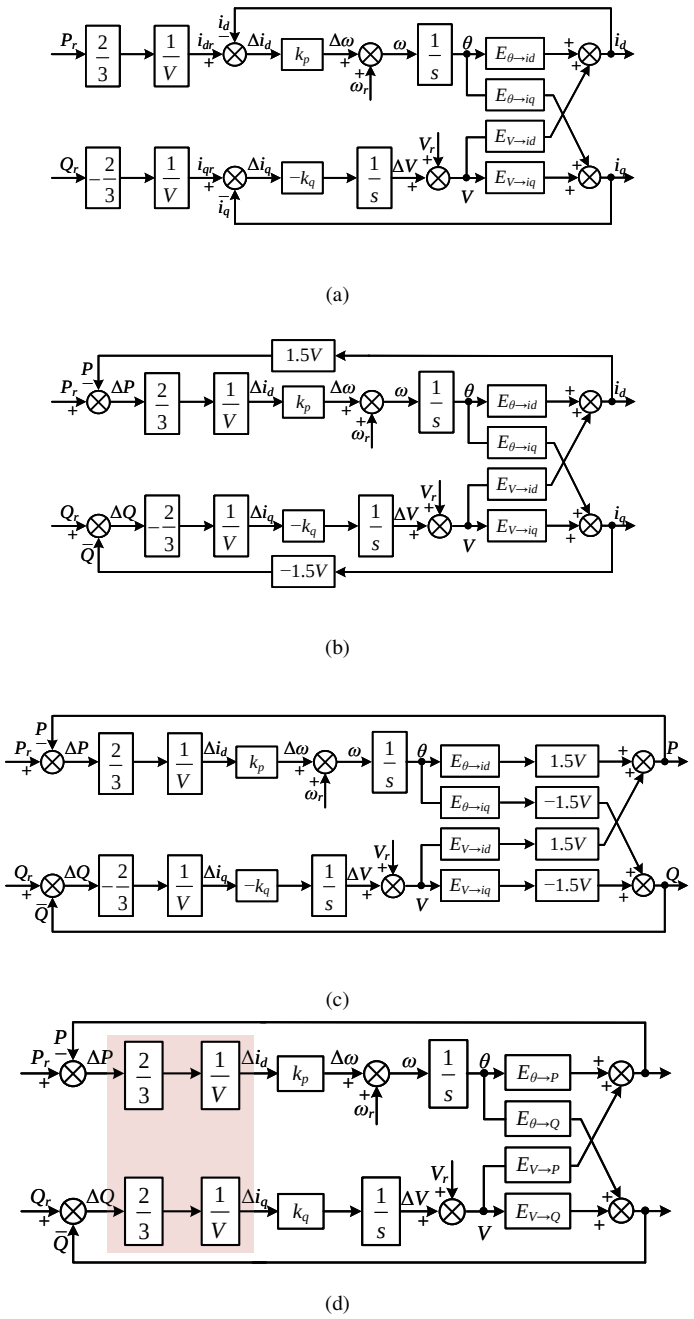



Fig. 5. Large-signal flow diagram of DCSC-based VSC-grid system under normal conditions.

### *C. Stability Boundary of Direct Current-Synchronization under Fault Conditions*

In case of large grid disturbances, $i_{dr}$ and $i_{qr}$ are saturated to constant values; thus, the large-signal flow diagram of the DCSC-based VSC-grid system under fault conditions is depicted in Fig. 6, while its small-signal model is shown in Fig. 7. The transmission zeros of the DCSC control plant $\mathbf{J}_{\mathrm{i}}(s)$ in (13) can be obtained simply by its determinant in (20), and the expression of its RHP zero is given by (21).

$$\det\left[\mathbf{J}_{\mathrm{i}}(s)\right] = J_{id\theta}(s)J_{iqV}(s) - J_{idV}(s)J_{iq\theta}(s) = 0 \tag{20}$$

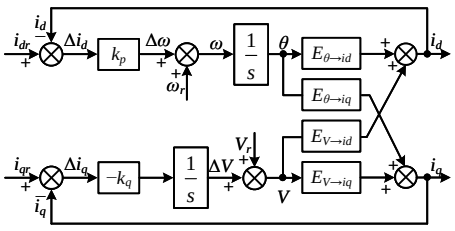



Fig. 6. Large-signal flow diagram of DCSC-based VSC-grid system under fault conditions

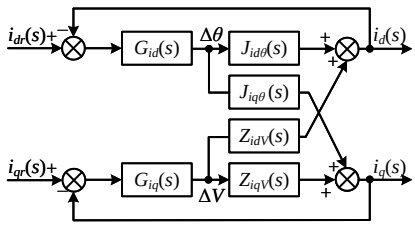



Fig. 7. Small-signal control diagram of DCSC-based VSC-grid system under fault conditions.

$$z = \omega_0 \cot\theta_0 \tag{21}$$

Upon comparing (21) with (19), it is notable that the location of the RHP transmission zero of $\mathbf{J}_{\mathrm{i}}(s)$ is solely related to the phase angle, independent of VSC and grid voltage magnitude. In contrast, the location of the transmission zero of $\mathbf{J}_{\mathrm{PQ}}(s)$ is significantly influenced by the voltage magnitude. This characteristic of $\mathbf{J}_{\mathrm{i}}(s)$ is highly advantageous for fault scenarios, where the voltage variations of VSC and grid become more significant. Consequently, the achievable control bandwidth of DCSC remains unaffected by voltage magnitude variations under fault conditions.

Moreover, according to (21), the RHP zero of $\mathbf{J}_{\mathrm{i}}(s)$ intersects the origin when $\theta = 90°$, regardless of voltage magnitude. Therefore, the phase angle boundary of the DCSC-based VSC-grid system under fault conditions is $\theta = 90°$.

### *D. Stability Boundary Condition of Direct Current-Synchronization under Fault Conditions*

As discussed above, the theoretical stability boundary of the DCSC-based VSC-grid system under fault conditions is $90°$, namely $\theta_{\max} = 90°$, regardless of voltage magnitude. This allows us to establish the stability boundary condition to ensure a consistently stable system under fault conditions. While the working control references are $i_{dr,\mathrm{sat}}$ and $i_{qr,\mathrm{sat}}$, the setting control references are $P_r$ and $Q_r$; thus, the stability boundary condition should be established to determine $P_r$ and $Q_r$.

The classic power-angle relationship in steady-state is expressed as follows:

$$P = \frac{3}{2}\frac{EV\sin\theta}{\omega_0 L} \tag{22}$$

Substituting (1) into (22) yields the expression of d-axis current under fault, $i_{df}$:

$$i_{df} = \frac{E_f}{\omega_0 L}\sin\theta \tag{23}$$

where $E_f$ represents the faulted grid voltage magnitude (peak value of phase voltage).

Since $i_{df}$ increases monotonically with $\theta$, the maximum d-axis current under fault is given by:

$$i_{df,\max} = \frac{E_f}{\omega_0 L} \tag{24}$$

Notably, $i_{df,\max}$ is solely dependent on the faulted grid voltage level $E_f$. Once a voltage dip occurs, $E_f$ is determined, so $i_{df,\max}$ is also established. Additionally, during the fault steady-state, $i_{dr} = i_{df}$ and $i_{qr} = i_{qf}$; thus, the maximum d-axis current reference $i_{dr,\max} = i_{df,\max}$. Consequently, as long as $i_{dr}$ during the fault is set lower than $i_{dr,\max}$, $\theta$ remains below $90°$, indicating a stable system. Conversely, if $i_{dr}$ is set larger than $i_{dr,\max}$, synchronization is compromised.

However, with a high short circuit ratio (SCR) value, corresponding to a low $\omega_0 L$ value, and a medium voltage dip level, corresponding to a medium $E_f$ value, $\frac{E_f}{\omega_0 L}$ might exceed $I_m$. Therefore, $i_{dr,\max}$ should be set as the minimum value between $I_m$ and $\frac{E_f}{\omega_0 L}$, as expressed in:

$$i_{dr,\max} = \min\left\{I_m, \frac{E_f}{\omega_0 L}\right\} \tag{25}$$

Since a circular current limiter is employed to mitigate over-current, the corresponding q-axis current reference magnitude is calculated as:

$$|i_{qr}| = \sqrt{{I_m}^2 - {i_{dr}}^2} \tag{26}$$

The active and reactive power output during the fault steady-state, denoted as $P_f$ and $Q_f$ respectively, are determined as follows:

$$\begin{aligned} P_f &= \frac{3}{2}\cdot i_{dr}\cdot V_f \\ Q_f &= \frac{3}{2}\cdot\sqrt{{I_m}^2 - {i_{dr}}^2}\cdot V_f \end{aligned} \tag{27}$$

Here, $V_f$ represents the converter voltage magnitude during the fault steady-state. The ratio of active and reactive power output following a large grid disturbance is contingent upon the determination of $i_{dr}$. Therefore, we can derive the stability boundary condition under fault conditions: as long as equation (28) is satisfied, the DCSC-based VSC-grid system can always maintain synchronization with the faulted grid:

$$\frac{P_r}{Q_r} \le \frac{i_{dr,\ \max}}{\sqrt{{I_m}^2 - {i_{dr,\ \max}}^2}} \tag{28}$$

From (28), it is evident that the system remains stable regardless of $P_r$ and $Q_r$ setpoints when $\frac{E_f}{\omega_0 L} > I_m$ ($i_{dr,\ \max} = I_m$), as the boundary threshold becomes infinite. Specifically, in a stiff grid connection with a medium voltage dip level. Moreover, according to grid code requirements [10],[11], once the grid voltage drops below 0.5 p.u., the converter is solely supposed to output reactive power, which means $P_r = 0$ p.u. and $Q_r = 1.0$ p.u.. In this case, $\frac{P_r}{Q_r} = 0$, which can always satisfy the stability boundary condition to guarantee a stable system.

TABLE I
SYSTEM AND CONTROL PARAMETERS

| Symbol | Description | Value |
|---|---|---|
| $S_r$ | Rated capacity of VSC | 1000 kVA (1.0 p.u.) |
| $E$ | Grid voltage (peak value of phase-to-ground) | 286 kV (1.0 p.u.) |
| $f_g$ | Grid frequency | 50 Hz |
| SCR | Short circuit ratio | 1 |
| $V_{dc}$ | DC link voltage | 640 kV (1.0 p.u.) |
| $k_p$ | Controller gain of PAL | 2.0 p.u. |
| $k_q$ | Controller gain of VML | 2.0 p.u. |
| $R_{vr}$ | Virtual resistor | 0.245 p.u. |
| $I_T$ | Threshold current of OCL | 1.1 p.u. |
| $I_m$ | Maximum allowable steady-state current magnitude | 2.333 kA (1.0 p.u.) |

## V. SIMULATION VALIDATION

To validate the effectiveness of the proposed DCSC, we conducted simulation tests in PSCAD/EMTDC using the same circuit topology in Fig. 2 and parameters outlined in Table I. The simulation setup contains a grid-connected VSC sending power to a 350-kV AC system. The DC link voltage of VSC is assumed to be well controlled at the other end.

### *A. Comparison between Power-Synchronization and Direct Current-Synchronization*

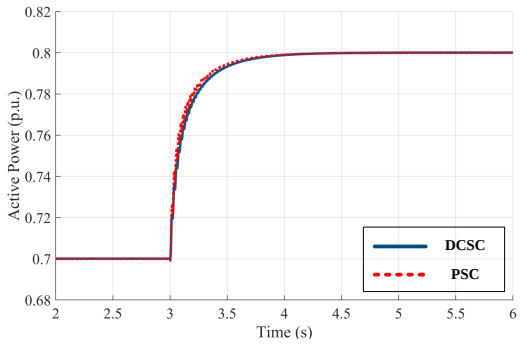
As discussed in Section IV (B), with appropriate control parameter settings, the DCSC scheme exhibits comparable control dynamics to the PSC scheme with reactive power regulation. Simulation tests are conducted to assess their dynamic responses when subjected to a step change in the active power reference.

A small step change in $P_r$, ranging from 0.7 p.u. to 0.8 p.u., was applied at the 3-second mark. The simulation results are depicted in Fig. 8. It is evident from the results that the dynamic responses of both DCSC and PSC schemes align closely, with only minor discrepancies observed at transients following the step input. These discrepancies arise from the slight variation in $V$, which dynamically alters the equivalent control gain of PAL and VML during transients.

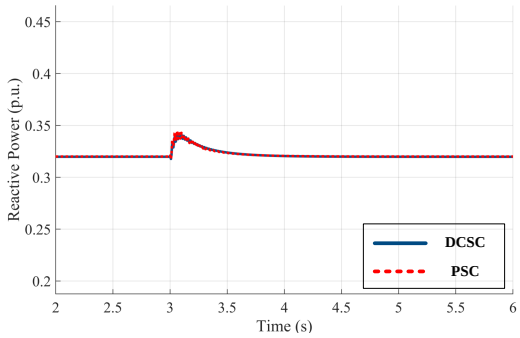
### *B. Verification of Stability Boundary under Normal Conditions*

The theoretical stability boundary of DCSC under normal conditions equals that of PSC with reactive power regulation, specifically $\theta = 60°$ when $\frac{V}{E} = 1$. To validate this boundary, we manually set $P_r = 0.857$ p.u and $Q_r = 0.485$ p.u. to ensure $\theta = 59°$ while $\frac{V}{E} = 1$ under normal conditions. Additionally, to assess the dynamic response of DCSC, we applied a step input of $P_r$ from 0.757 p.u. to 0.857 p.u. The simulation results are depicted in Fig. 9. It is clear to see that approximately 15 seconds are required for the phase angle to reach the target value of 59°. This is attributed to the time delays induced by the RHP zero, which is very close to the origin when $\theta = 59°$, indicating an extremely low control bandwidth. Nevertheless, the system remains at a critically stable condition.

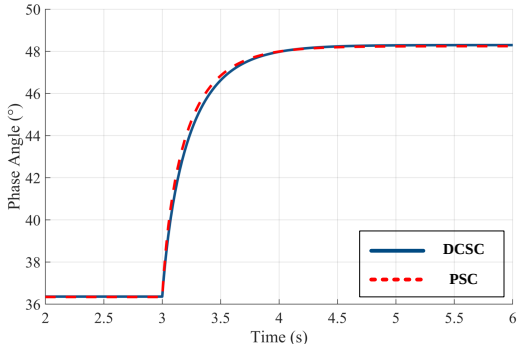
Next, a further small step input of $P_r$, increasing from 0.857 p.u. to 0.9 p.u., was applied, and the resulting phase angle response is illustrated in Fig. 10. Given that $\theta = 59°$ is near a critical stable operating point, even a slight increase in $P_r$ can induce system instability. Consequently, the phase angle



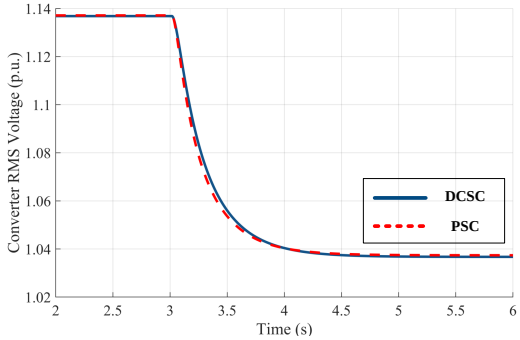

(a) Active power response




(b) Reactive power response

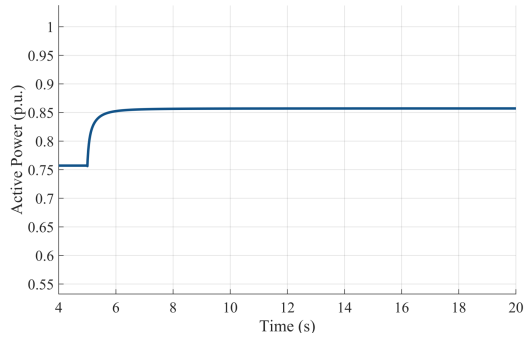



(c) Converter phase angle response

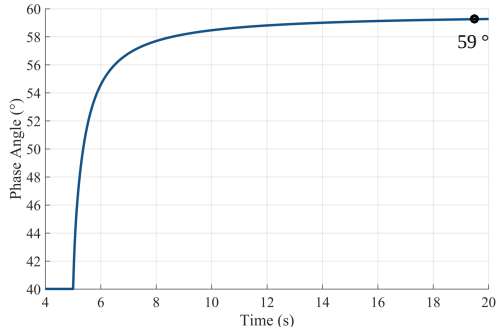



(d) Converter voltage magnitude response

Fig. 8. Comparison between DCSC and PSC when subjected to a step input of active power reference ($P_r$ changes from 0.7 p.u. to 0.8 p.u.).




(a) Active power response




(b) Converter phase angle response

Fig. 9. Stability boundary of DCSC under normal conditions when subjected to a step input of active power reference ($P_r$ changes from 0.757 p.u. to 0.857 p.u.).

fluctuates within the range of $-180°$ to $180°$.

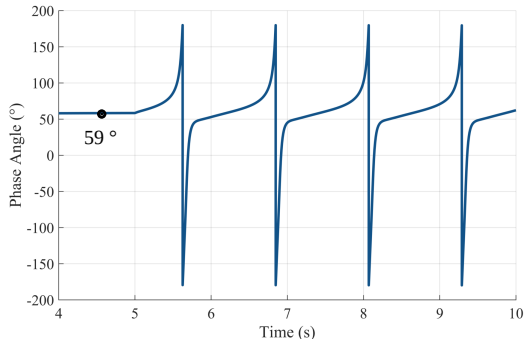
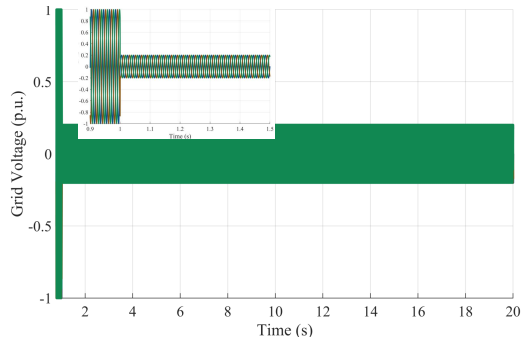


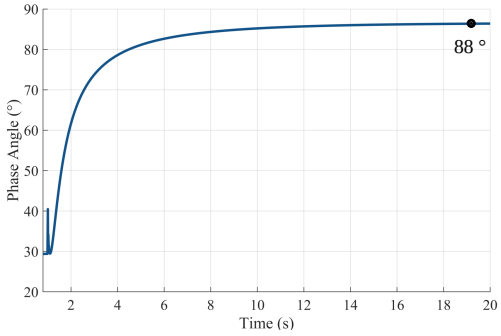

Fig. 10. Stability boundary of DCSC under normal conditions when subjected to a step input of active power reference (($P_r$ changes from 0.857 p.u. to 0.9 p.u.).

### *C. Verification of Stability Boundary under Fault Conditions*

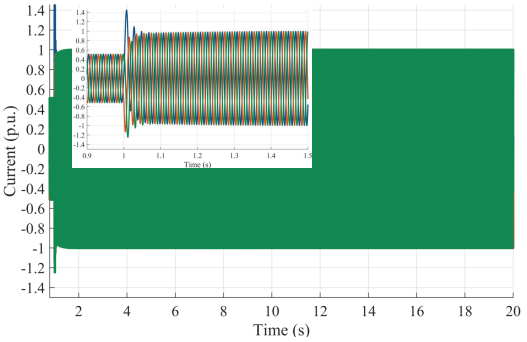
The theoretical stability boundary of DCSC under large grid disturbances is $\theta = 90°$, independent of voltage magnitude. To verify this boundary value, a severe voltage dip disturbance is emulated at the 1-second mark, causing $E$ to drop from 1.0 p.u. to 0.2 p.u. To attain $i_{dr,\max}$, we manually set $P_r = 0.466$ p.u. and $Q_r = 2.286$ p.u. during the fault. The simulation results are depicted in Fig. 11. After approximately 20 seconds, the phase angle approaches $88°$. This phenomenon is




(a) Grid voltage response




(b) Converter phase angle response




(c) Converter current response

Fig. 11. Stability boundary of DCSC under fault conditions ($P_r = 0.466$ p.u. and $Q_r = 2.286$ p.u. during the fault).

attributed to the RHP zero nearing the origin with $i_{dr,\max}$, resulting in significant time delays and an exceptionally low control bandwidth. Nevertheless, the system maintains stability even with $\theta = 88°$.

Furthermore, it is evident that the transient fault overcurrent at the fault-inception point is approximately 1.4 p.u. as the OCL scheme is deactivated to simplify the verification of the stability boundary. Additionally, a transient phase angle overshoot is observable at the fault-inception point due to the delayed control dynamics in adjusting to the new power reference values.

Next, $P_r$ is slightly raised from 0.466 p.u. to 0.5 p.u., and the resulting phase angle response is depicted in Fig. 12. It is obvious that the system becomes unstable as the required phase angle exceeds $90°$.

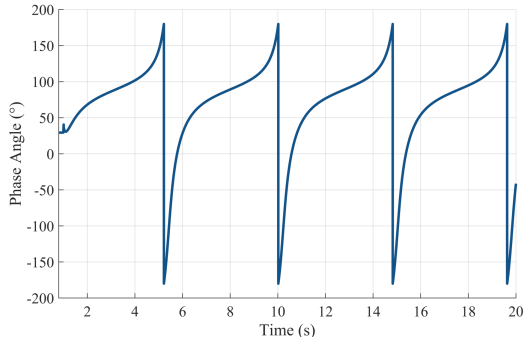



Fig. 12. Stability boundary of DCSC under fault conditions ($P_r = 0.5$ p.u. and $Q_r = 2.286$ p.u. during the fault).

### D. Verification of Fault Ride Through Process under Voltage Dip Disturbance

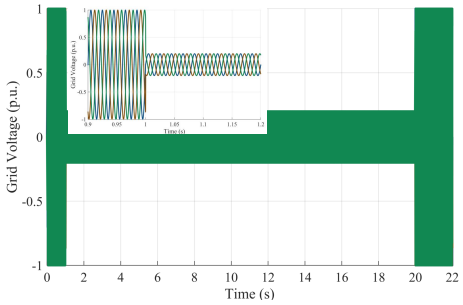
In this part, the entire FRT process of the DCSC-based VSC in the case of a voltage dip disturbance ($E_f = 0.2$ p.u.) was simulated. Two scenarios are tested: 1. The ratio between $P_r$ and $Q_r$ satisfies $i_{dr,\max}$ in (25) to achieve the stability boundary during the fault. 2. $Q_r = 1.0$ p.u. while $P_r = 0$ p.u. to comply with the grid code requirement. Besides, the OCL scheme is activated hereafter.

*1) $i_{dr,max}$ scenario:* The simulation results of the FRT process with the $i_{dr,\max}$ setting are plotted in Fig. 13. The voltage dip disturbance occurs at the 1-second mark and is cleared at the 20-second mark. The resulting steady-state fault current in Fig. 13 (b) stays within 1.0 p.u. due to the operation of the circular current limiter, while the transient fault overcurrent at fault-inception and -clearing points stay below 1.2 p.u. due to the operation of the OCL scheme. The converter phase angle can reach up to $88°$ after the fault occurrence and successfully returns to the pre-fault value after the fault disappears. Some overshoots can be observed in the phase angle at fault transients due to control delays. In summary, the DCSC-based VSC can ride through the voltage dip disturbance even under stability boundary conditions.

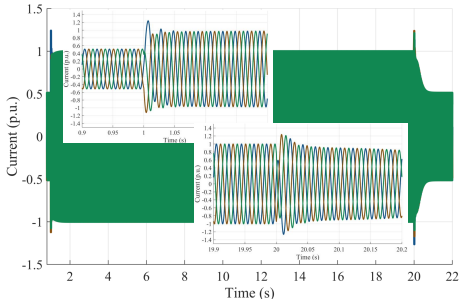
*2) $Q_r = 1.0$ p.u. scenario:* To comply with the grid code requirement, $Q_r$ is set to 1.0 p.u. during the fault. The same voltage dip disturbance was implemented at the 1-second mark and cleared at the 5-second mark. As the system control bandwidth is much faster than that with $i_{dr,\max}$ during the fault, the simulation duration can be shortened. Simulation results are plotted in Fig. 14. It is clear that the transient fault overcurrent can remain within 1.2 p.u. and the phase angle reaches zero during the fault as $P_r = 0$ p.u..

### E. Verification of Fault Ride Through Process under Phase Jump Disturbance

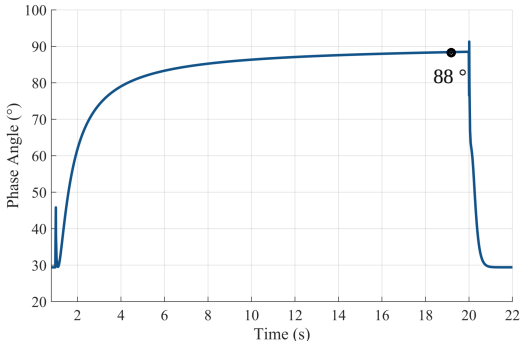
Another common grid disturbance is the phase jump. According to the grid code requirement, the GFM converter is supposed to remain connected to the grid under a $-60°$ phase jump disturbance [10]. Therefore, in this part, the performance of the DCSC is tested with a $-60°$ phase jump disturbance occurring at the 1-second mark. Simulation results are plotted in Fig. 15. It is clear to see that the converter phase angle




(a) Grid voltage response




(b) Converter current response



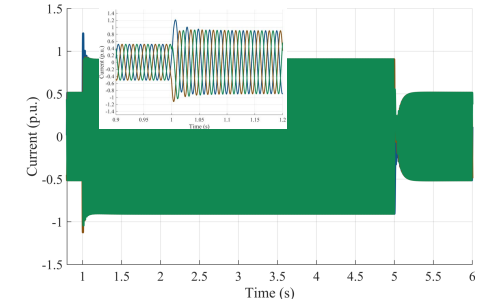

(c) Converter phase angle response

Fig. 13. FRT process of DCSC under the voltage dip with $i_{dr,\max}$.

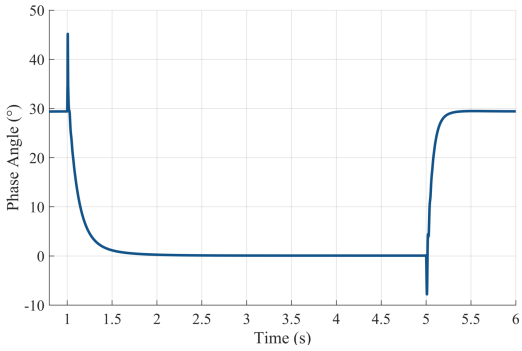
changes from $29.8°$ to $-30.2°$ under this disturbance, and the corresponding transient fault current can be well maintained below 1.3 p.u..

## VI. Conclusion

This article proposes a DCSC scheme to address the synchronization issue of GFM-VSCs operating under current-limitation mode, without relying on a PLL. The validity of the DCSC control concept is substantiated by establishing connections between the VSC current and its phase angle, with power serving as an intermediate variable. The theoretical stability boundaries of DCSC under both normal and fault conditions are derived, and stability boundary conditions are established to ensure a stable system under large grid disturbances. Additionally, a control gain self-adaptivity scheme is designed to accelerate resynchronization after the fault, with minimal effects on control performance under normal

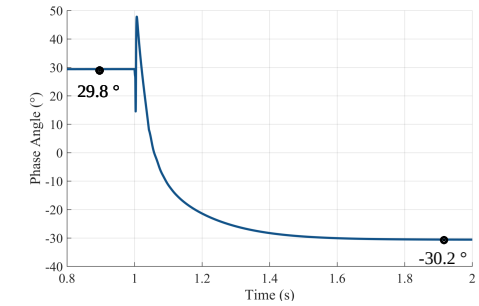



(a) Converter current response

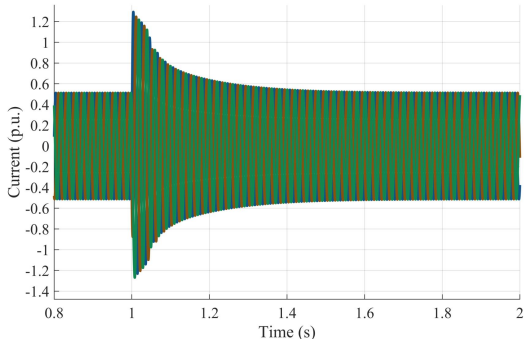



(b) (b) Converter phase angle response

Fig. 14. FRT process of DCSC under voltage dip with $Q_r = 1.0$ p.u.




(a) Converter phase angle response




(b) Converter current response

Fig. 15. FRT process of DCSC under the phase jump.

conditions. Essentially, the DCSC exhibits identical small-signal control dynamics to PSC with reactive power regulation under normal conditions but demonstrates enhanced FRT performance in the case of large grid disturbances. Finally, experimental results validate the control dynamic similarity between PSC and DCSC, the stability boundaries of DCSC under both normal and fault conditions, as well as the effectiveness of DCSC in riding through large grid disturbances.

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