Novel low-temperature interconnects for 2.5/3D MEMS integration: demonstration and reliability

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***Abstract*—In response to the evolving demands of microelectromechanical system (MEMS) integration, aiming to achieve high-performance electronic products, innovative interconnect solutions are becoming essential. The interconnects must possess key features, including the capability for miniaturization, low processing temperatures, and the ability to maintain a stable microstructure with optimized electrical, mechanical, and thermomechanical properties. To meet these demands, this study designed a novel Cu-Sn-based solid-liquid interdiffusion (SLID) interconnect. The study involved the implementation of a metallization stack, incorporating Co as a layer to interact with low-temperature Cu-Sn-In SLID and form intermetallic compounds (IMCs). Since $Cu_6(Sn,In)_5$ forms at a lower bonding temperature than other phases commonly observed in the Cu-Sn-In system, the study aimed to develop interconnects comprising a stable single-phase $(Cu,Co)_6(Sn,In)_5$. Bonding conditions were established for the Cu-Sn-In/Co system and the Cu-Sn/Co system as a reference. Thorough assessments of their thermomechanical reliability were conducted through high-temperature storage (HTS), thermal shock (TS), and tensile tests. The Cu-Sn-In/Co system emerged as a reliable low-temperature solution with the following key attributes: 1) a reduced bonding temperature compared to the Cu-Sn SLID interconnects, 2) the absence of the Cu_3Sn phase and resulting void-free interconnects, and 3) high thermomechanical reliability, particularly following thermal annealing after bonding.**

***Index Terms*— 3D integration, contact metallization, Cu-Sn SLID, electronics packaging, interconnects, MEMS, reliability**

I. INTRODUCTION

The next generation of microelectromechanical systems (MEMS) is needed in a variety of applications, ranging from low-power wireless sensor networks for the internet of things (IoT) to optical three-dimensional (3D) systems for object recognition [1], [2], [3]. In these applications, the performance of current MEMS devices must be vastly improved in the fields of latency, accuracy, sensitivity, energy efficiency, safety, reliability, and more [3]. To achieve such high-performance smart sensors, the 3D heterogeneous integration of components, miniaturized interconnect technologies, and the encapsulation of many MEMS components are required [4], [5], [6], [7]. Advanced miniaturized interconnects are needed to merge the MEMS sensors and transducers with application-specific integrated circuits (ASICs) and microcontroller units (MCUs) for edge processing [8], [9]. The hermetic encapsulation of MEMS is typically established by wafer bonding of a MEMS device wafer to a cap wafer [3], [10], [11], [12]. However, the pursuit of high-functional-performance electronic products necessitates reliable bonding methods with a low processing temperature and low residual stresses in both the sensitive MEMS elements and the entire package [7], [9]. Simultaneously, the low bonding temperature might not compromise the subsequent process steps, and therefore the newly formed interconnect areas should have a high remelting temperature [13], [14]. Additionally, the interconnect metallurgy must be designed such that unnecessary lithography processes and wet chemistry of device wafers can be avoided [15], [16], [17].

In response to these diverse challenges, Cu-Sn solid-liquid interdiffusion (SLID) bonding presents an attractive solution. It has the potential to simultaneously enable hermetic sealing for MEMS and high-density, short signal path electrical interconnects for the integration of MEMS and integrated circuits (ICs) [3], [7], [18], [19], [20]. However, the process temperature of Cu-Sn SLID bonding exceeds 250 °C, and the typical procedure involves electroplating Cu and Sn on both wafers to be bonded [15], [16], [17]. Consequently, achieving optimal performance with Cu-Sn SLID interconnects in high-performance smart sensor systems requires ongoing improvements in bonding material design. Given that the bonding temperature of the SLID system is directly linked to the melting point of the low-temperature metal [21], one potential approach is to replace Sn with low-temperature alloyed Sn to reduce the Cu-Sn SLID bonding temperature. In the development of lead-free solders, Bi, In, and Zn were found to be the most feasible alloying elements for Sn, effectively lowering the melting point of Sn [14], [22], [23], [24], [25]. Nevertheless, it has been found that Sn-Zn solders exhibit poor wettability and corrosion resistance [22], [26], [27], [28], while Sn-Bi solders suffer from low wettability and brittleness due to the inherent nature of bismuth [14], [29], [30], [31]. Furthermore, Cu-Sn-Bi SLID bonding fails to achieve fully formed intermetallic compounds (IMCs) interconnects, even

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after a bonding time of 24 hours, and notable Bi segregation occurs during the bonding process [32]. Consequently, Sn-Bi and Sn-Zn alloys may not be the most suitable substitutes for pure Sn. However, In does not present the aforementioned problems as it is thermodynamically very close to Sn [33]. Sn-In alloys have emerged as a viable option for addressing the considerations in MEMS integration for the following reasons.

Overall, Sn-In alloys offer good soldering properties. With excellent wetting properties on glass, quartz, and ceramic materials, they could be ideal for metal-to-non-metal joining [30]. Furthermore, the bonding temperature can be as low as 150 °C [34], and the remelting temperature exceeds 600 °C [21], as the bonding results in a fully formed IMC bond-line without any traces of unreacted low melting point material [34], [35], [36]. Two IMCs ($Cu_3(In,Sn)$ and $Cu_6(In,Sn)_5$) have been reported to form in reactions of InSn alloys with Cu at temperatures between 150 °C and 400 °C [37]. These phases have the same crystal structures as the well-known Cu_3Sn and Cu_6Sn_5 compounds with In atoms occupying the Sn sublattices [14]. In addition, O. Golim et al. have successfully manufactured fine pitch Cu-Sn-In microbumps, demonstrating the possibility of Cu-Sn-In SLID bonds being as small as 10 µm [34]. Despite the numerous positive properties exhibited by Cu-Sn-In SLID, process integration for MEMS and the interconnect reliability have not been reported. Hence, the utilization of Cu-Sn-In for MEMS/MOEMS integration necessitates a physical vapor deposition (PVD)-deposited contact metallization layer on the wafers/chips housing these devices.

Previous studies have demonstrated that cobalt (Co) is a plausible contact metallization for a Cu-Sn SLID system [16], [17], [38], [39]. Our prior investigations [40] have also shown that when a Co foil is in contact with Cu-Sn-In electroplated chips, it demonstrates favorable wettability, In participates in IMC formation, and a full IMC joint can be achieved within the standard bonding timeframe. Furthermore, utilizing Co as a contact metallization in Cu-Sn-In SLID bonding has additional positive impacts. Specifically, it effectively prevents the formation of $Cu_3(Sn,In)$ during the bonding process at temperatures ranging from 160 °C to 250 °C. Consequently, the microjoints consist of a void-free single phase, $(Cu,Co)_6(Sn,In)_5$ [16], [40]. However, in a pure Cu-Sn-In system, Cu_3Sn still forms at 250 °C [35]. Additionally, research has shown that $(Cu,Co)_6(Sn,In)_5$ exhibits the highest Ei/H value compared to $Cu_6(Sn,In)_5$ and Cu_6Sn_5, indicating superior plasticity [40]. Therefore, the reliability of Cu-Sn-In in contact with Co seems promising when Co is involved in IMC formation. However, it is essential for further studies to design the metallization stack containing Co and to ensure the reliability of Cu-Sn-In/Co SLID interconnects. Taking this into consideration and drawing upon our previous studies [15], [40], [41], we have designed the SLID metallization stacks for Cu-Sn-In. In addition, we assessed the reliability of the Cu-Sn-In/Co SLID interconnects, using this novel SLID system, through a high-temperature storage (HTS) test, a thermal shock (TS) test, and tensile tests, comparing the results with Cu-Sn/Co SLID interconnects as a reference.

II. Materials and methods

A. Specimen preparation

Wafer preparation

All samples were prepared on thermally oxidized (300 nm SiO2), double side polished 100 mm Si 〈100〉 wafers with a thickness variation (TTV) below 2 µm. Bonded wafers were categorized into two distinct types: wafers intended to house MEMS devices, referred to as device wafers, and wafers designated for bonding to the device wafers, named cap wafers. The preparation of cap wafers began by sputtering a 60 nm thick TiW adhesion layer on the Si wafer, followed by sputtering a 100 nm thick copper seed layer. Subsequently, a thick photoresist mask featuring ring structures was developed through the lithography process, utilizing AZ15nXT photoresist. For the Cu-Sn/Co system, a 4 µm layer of copper was electroplated into the resist openings using the NB Semi plate Cu 100 bath, followed by the electroplating of 2 µm of tin using the NB Semi plate Sn 100 solution from NB technologies. In the case of the Cu-Sn-In/Co system, a 5 µm copper layer was electroplated into the resist openings using the NB Semi plate Cu 100 bath, followed by the sequential electroplating of 1.7 µm tin using the NB Semi plate Sn 100 solution and 1.7 µm indium using an indium sulfamate plating bath. For the device wafers, a photoresist mask with a ring structure was formed via lithography using AZ 5214 E Image Reversal Photoresist. In the Cu-Sn/Co system, a 60 nm thick Ti adhesion layer was sputtered onto the Si wafer, succeeded by the deposition of a 200 nm thick Mo barrier layer and an 80 nm Co layer using sputtering. Similarly, for the Cu-Sn-In/Co system, a 60 nm thick Ti adhesion layer was sputtered onto the Si wafer, followed by a 400 nm thick Co layer. At the end, for both the Cu-Sn/Co and Cu-Sn-In/Co systems, a protective thin layer of Au (10 nm) was sputtered onto the Co layer to prevent oxidation. Prior to the bonding, the metallization stack on the device wafers was patterned using a lift-off process, while the cap wafers were patterned by removing the photoresist and etching away the Cu seed layer and TiW adhesion layer. **Fig. 1** provides a schematic illustration of the process flow for the cap and handle wafers used in Cu/Sn/Co and Cu/Sn-In/Co samples.

Bonding process

The bonding process was carried out using an AML wafer bonder. The interconnects were aligned and pre-heated to 150 °C and 100 °C in the Cu-Sn/Co and Cu-Sn-In/Co systems, respectively, before bringing the cap and device wafers into contact. The wafers were brought into contact using a 5 kN uniaxial contact force from the bottom plate and then heated to 250 °C and 200 °C in the Cu-Sn/Co and Cu-Sn-In/Co systems, respectively, at a heating rate of 10 °C/min. After holding the temperature at 250 °C for 0.5 hours in the Cu-Sn/Co system and at 200 °C for 1 hour in the Cu-Sn-In/Co system, the contact force was released. The temperature was gradually reduced to 65 °C at a cooling rate of 1 °C/min before the bonded pair was removed from the chamber. Subsequently, the bonded wafers were diced into 10 mm × 10 mm chips containing one ring

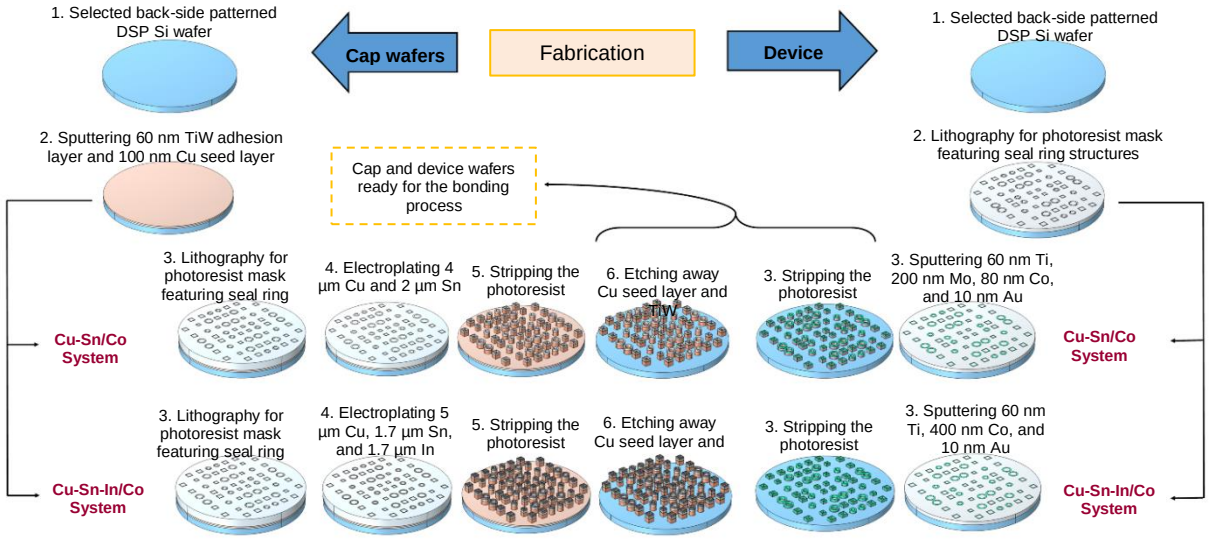

Fig. 1. Schematic illustration depicting the fabrication process of wafers for Cu-Sn/Co and Cu-Sn-In/Co systems.

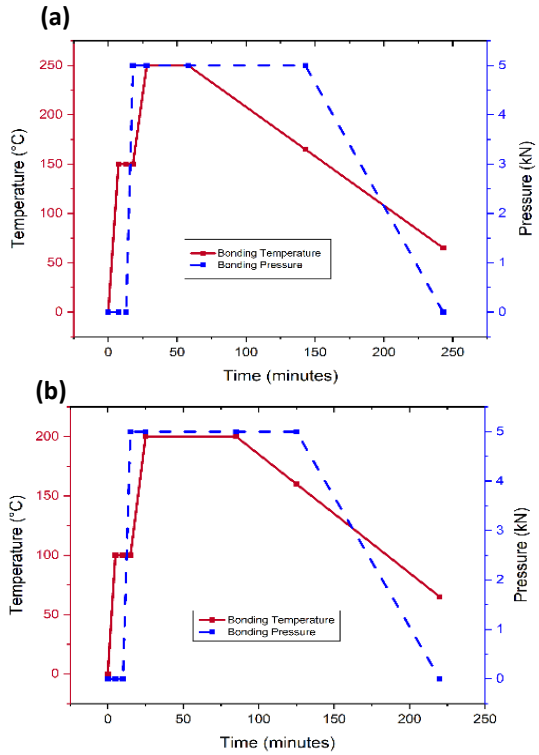

Fig. 2. A schematic illustration of the temperature and pressure profile during bonding for (a) Cu-Sn/Co sample and (b) Cu-Sn-In/Co sample

interconnect, which were used in tensile and thermal aging tests, and in cross-sectional analysis. **Fig. 2** depicts a schematic illustration detailing the temperature and pressure profiles during bonding for both Cu-Sn/Co and Cu-Sn-In/Co systems.

B. Thermal treatments

High-temperature storage (HTS)

The HTS test was carried out on a minimum of 10 chips for both Cu-Sn/Co and Cu-Sn-In/Co interconnects. The testing was conducted using a Heraeus Instruments oven for a duration of 1000 hours at a temperature of 150 °C.

Thermal shock (TS)

The TS test was conducted using the ESPEC TSA-71 S TS chamber system. The TS test was performed according to the JEDEC JESD22-A104D standard, with test condition G and soak mode 3. The TS test parameters were as follows: an operational temperature range of −40 °C to +125 °C, a ramp rate of 33 °C/min, a 10 min dwell time applied to both high and low temperatures, and a total cycle time of 30 min. A minimum of 10 samples were subjected to 1000 cycles.

C. Tensile test

The tensile strength of the interconnects for all as-bonded (AB), thermal-shocked, and HTS tested samples was evaluated using a stud pull approach. An MTS 858 Table System, which was equipped with a Flex Test 40 Digital controller and an MTS Silent Flow HPU system, was employed. The samples were affixed to 10 mm-diameter brass studs using high-strength epoxy glue (Loctite Power Epoxy Universal). These brass studs were then linked to machined brass holders featuring 10 mm holes using steel screws. Steel wires were mechanically fixed to the brass holders and were subsequently connected to the central positions of the hydraulic clamps within the MTS 858 Table system. A strain rate of 0.1 mm/s was applied during testing. A minimum of 10 samples of the AB specimens were evaluated. Furthermore, at least three samples from each group of thermally shocked and HTS-tested specimens were tested as well.

D. SEM/EDX analysis

The samples were prepared for cross-sectional analysis using standard metallographic methods. The cross-sections and fracture surfaces were analyzed using a JEOL JSM-7500FA and JEOL JSM-6330F field emission scanning electron microscope (SEM) equipped with Oxford Instruments INCA X-sight energy-dispersive X-ray spectroscopy (EDX) equipment. EDS analysis was performed on at least five separate locations for every phase.

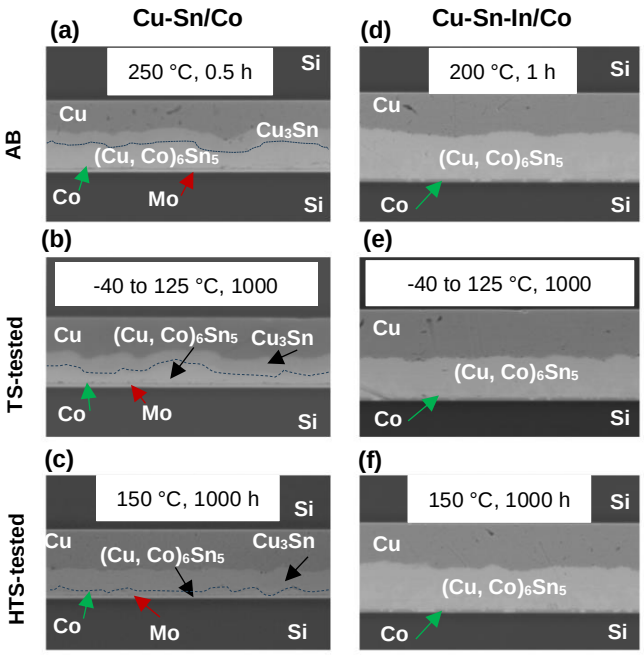

Fig. 3. BSE-SEM micrographs of Cu-Sn-In/Co bonded samples (a) as-bonded (AB), (b) after thermal shock (TS) test, and (c) after high-temperature storage (HTS) test; Cu-Sn/-Co bonded samples (d) AB, (e) after TS test, and (f) after HTS test.

III. RESULTS AND DISCUSSION

A. *Cross-sectional analysis*

Fig. 3 shows BSE-SEM micrographs of Cu-Sn /Co and Cu-Sn-In /Co interconnects after bonding, TS testing, and HTS testing. Through EDX analysis, two phases, namely $(Cu,Co)_6Sn_5$ and Cu_3Sn, were identified at the bond-line of Cu-Sn/Co reference samples. The Cu_3Sn/Cu_6Sn_5 ratio increased after both TS and, more notably, HTS testing. This resulted in the composition of the bond-line shifting to $(Cu,Co)_3Sn$, with a thin layer of $(Cu,Co)_6Sn_5$, with high Co content, after HTS testing. Nearly half of the HTS-tested samples experienced detachment in the bond-line. In contrast, Cu-Sn-In/Co interconnects exhibited a single-phase composition, $(Cu,Co)_6(Sn,In)5$, with no phase transformation observed following both TS and HTS testing. The results of TS and HTS testing indicated that the low-temperature Cu-Sn-In/Co interconnects were microstructurally more stable than the reference Cu-Sn/Co interconnects.

B. *Tensile strength and fracture mode*

Fig. 4 summarizes the investigation of the mechanical properties and failure characteristics of the studied interconnects, presenting the tensile strengths, the fracture surfaces, and the fracture paths. According to the results, the TS test had an insignificant impact on the tensile strength of both the Cu-Sn/Co and Cu-Sn-In/Co interconnects. In both the AB and TS-tested samples, the Cu-Sn/Co interconnects exhibited a significantly higher tensile strength compared to the low-temperature Cu-Sn-In/Co interconnects. Conversely, when subjected to the HTS test, the tensile strength of the Cu-Sn-In/Co interconnects experienced a substantial improvement. The tensile strength of the Cu-Sn/Co interconnects showed a marginal increase, and some samples even detached during the HTS test, resulting in an effective tensile strength of zero.

The fracture surfaces of the tensile-tested samples were carefully examined using SEM-EDX, as demonstrated in **Fig. 4**. Within the Cu-Sn/Co interconnects, both AB and TS samples exhibited nearly identical fracture surfaces. One fracture surface primarily comprised $(Cu,Co)_6Sn_5$, while the other was composed of $(Cu,Co)_6Sn_5$, Co, and Mo. In contrast, the HTS sample exhibited a different fracture surface compared to the AB and TS-tested samples. On one fracture surface, $(Cu,Co)_6Sn_5$, Cu_3Sn, and Mo were identified; while on the other, $(Cu,Co)_6Sn_5$, Cu_3Sn, Co, Ti, and Mo were observed. However, since the subsequent fracture surface was in proximity to the metallization layer, and some of the EDX data could have originated from the metallization beneath it, there was some uncertainty about the accurate identification of the IMCs on this fracture surface. Therefore, a higher-resolution SEM-EDX analysis was employed to examine the cross-section of the samples before the tensile test, aiming to identify any additional phases near the Ti/Mo/Co metallization stack. The study validated the phase identification. In summary, the fracture path for AB and TS samples followed a pattern: within the $(Cu,Co)_6Sn_5$ phase, at the Mo/IMC and Co/IMC interface. Meanwhile, for the HTS sample, the fracture path exhibited the following pattern: within the $(Cu,Co)_6Sn_5$ phase, at the $Cu_3Sn/(Cu,Co)_6Sn_5$, $Co/(Cu,Co)_6Sn_5$, and $Mo/(Cu,Co)_6Sn_5$ interface, and the Ti/Mo interface.

The observed fracture paths and measured tensile strength values of the Cu-Sn/Co interconnects imply that Co might not be the most optimal choice as a contact metallization layer for Cu-Sn interconnects. This is compounded by the drawback of Sn solders, which have high melting points, requiring high-temperature assembly. A significant variation in the Co content within the Cu_6Sn_5 phase, rather than a gradual change in Co content along the bond-line, can lead to a weak interface. This observation can be rationalized by referring to isothermal sections of Cu-Sn-Co at 250 °C (the bonding temperature) and 150 °C (the storage temperature) presented in Fig. 5. The phase diagrams illustrate that $(Cu,Co)_6Sn_5$ and Co cannot be in thermodynamic equilibrium in direct contact, requiring the presence of some Co-Sn IMCs (CoSn, $CoSn_2$, or $CoSn_3$) in between. Depending on the Co-Sn IMCs formed adjacent to Cu_6Sn_5, the diffusion path must follow a particular Co content (indicated by tie lines). Similarly, a similar scenario arises considering Cu-side IMC equilibria; Cu_3Sn occurs 2between Cu and Cu_6Sn_5, with a distinct diffusion path and specific Co content. Transitioning from the Cu side to the Co side, Cu_6Sn_5 itself, with varying Co content, can only exist in thermodynamic equilibrium if the Co content increases continuously within the phase, as can be seen in the enlarged section of the isothermal sections for both temperatures in **Fig. 5**. This can be observed in the phase diagram, and possible reaction sequences are illustrated with dotted lines I–III in **Fig. 5**. This indicates the underlying reason for the plausible

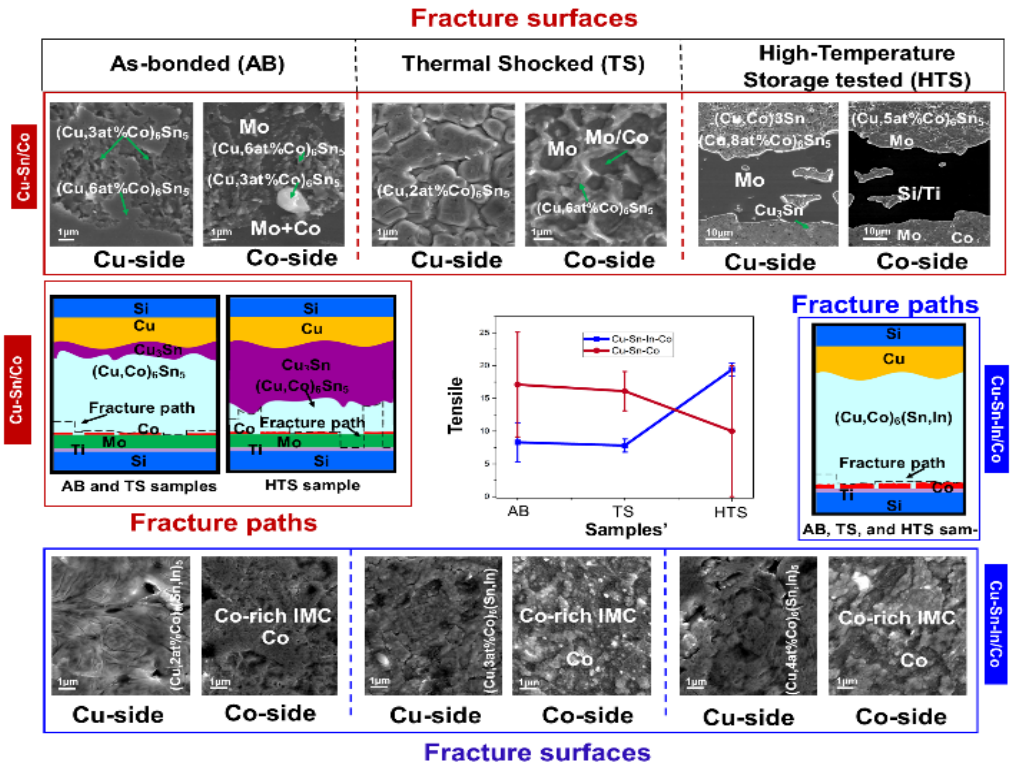

Fig. 4. Fracture surfaces, a schematic depicting fracture paths, and tensile strength values of Cu-Sn/Co and Cu-Sn-In/Co samples in their AB, TS, and HTS-tested states.

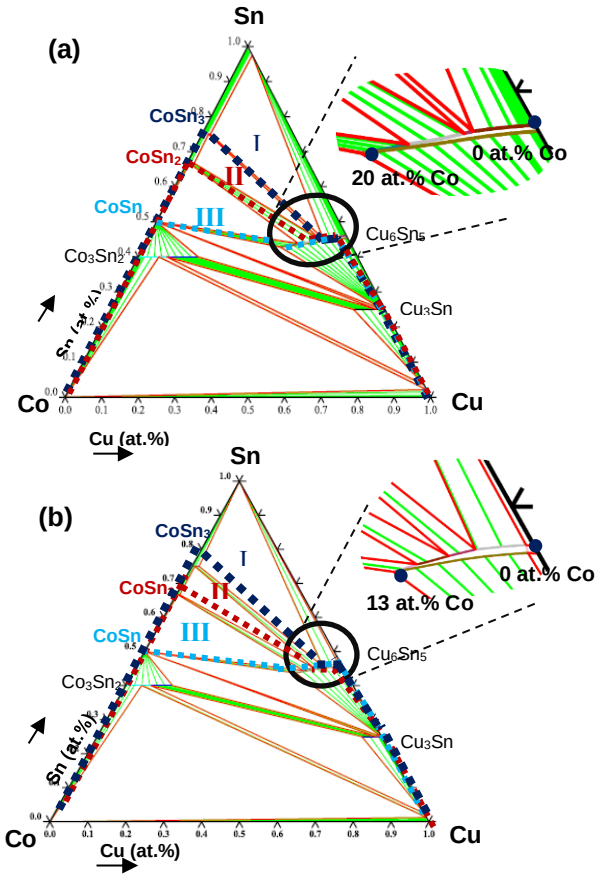

Fig. 5. Calculated isothermal section of Cu- Sn-Co at (a) 250 °C and (b) 150 °C.

inherent weakness in the Co/$(Cu,Co)_6Sn_5$ interface with evolving local phase equilibria. In general, while it is true that Co can hinder the formation of Cu_3Sn in the Cu-Sn system, Cu and $(Cu,Co)_6Sn_5$ react and form Cu_3Sn during the HTS test. This transformation results in a volumetric change in the system, potentially serving as a stress initiation point [42]. On the other hand, Co tends not to dissolve readily into the Cu_3Sn phase [16], [17]. Consequently, with more Cu_3Sn formation, more Co is dissolved into the remaining Cu_6Sn_5, potentially leading to a weaker interface between Cu_3Sn and $(Cu,Co)_6Sn_5$.

In the case of the low-temperature Cu-Sn-In/Co SLID interconnects, all examined samples (AB, TS, and HTS) showed identical fracture surfaces after the tensile test. One surface consisted of $(Cu,Co)_6(Sn,In)_5$, while the other surface was composed of Co with trace amounts of Cu, Sn, and In in localized areas of the fracture surface. It is plausible that these regions represent the same $(Cu,Co)_6(Sn,In)_5$ compound overlaying Co and, due to its extremely thin nature, EDX analysis can also collect data from the underlying Co layer. A closer examination of the microstructure near the Co side is required to determine the exact composition, which will be discussed below. In any case, the fracture path for the Cu-Sn-In/Co interconnects is consistent, occurring at the interfaces of Co/$(Cu,Co)_6(Sn,In)_5$ and the unidentified IMC/$(Cu,Co)_6(Sn,In)_5$.

Fig. 6 presents the results of the EDX mapping for Cu-Sn-In/Co interconnects for AB, TS-, and HTS-tested samples, in close proximity to the Co metallization layer, where the tensile fractures occurred. Additionally, two line scans were performed: one in the area where all of the Co metallization was

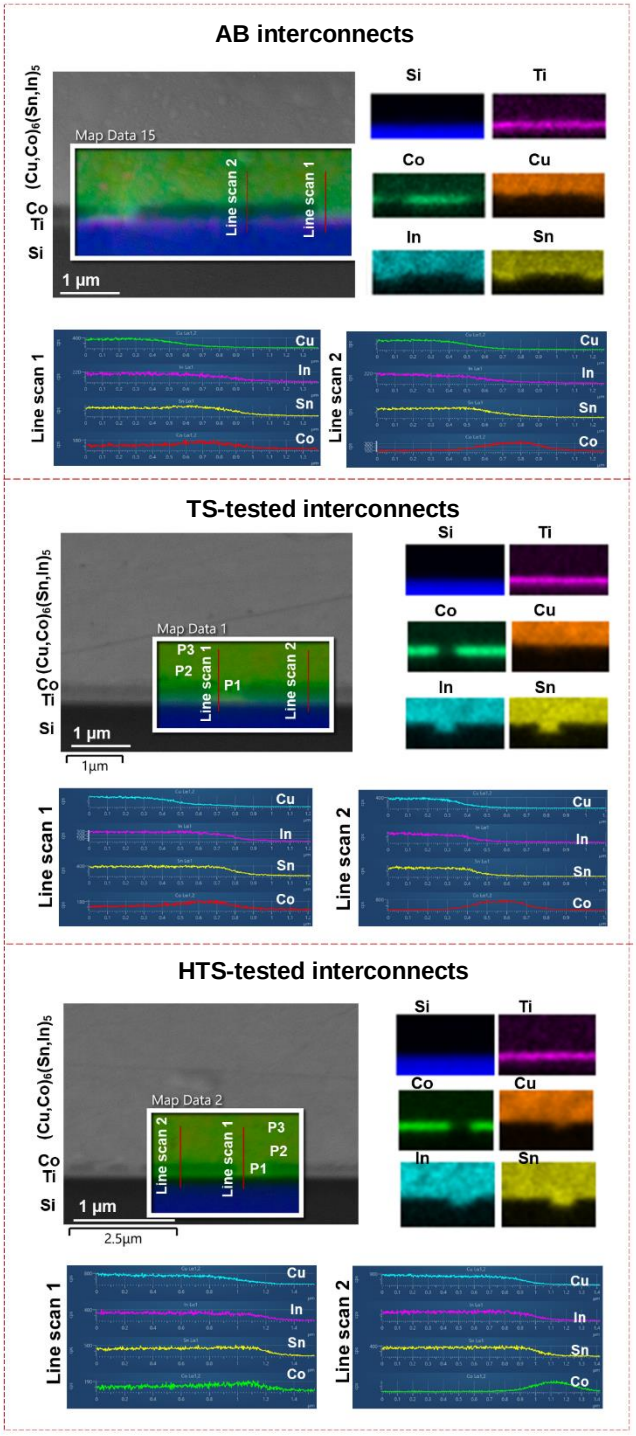

Fig. 6. EDX analysis of the region near the Co metallization layer in Cu/Sn-In/Co interconnects.

consumed, and another in an area where the Co metallization layer remained partially intact (presented in **Fig. 6**). The results showed that the concentration of Co in the IMCs was notably higher near the Co metallization layer or in areas where all of the Co was consumed, in comparison to other regions. In contrast, the concentration of Cu in these IMCs was lower in these specific areas compared to others. However, this difference is less prominent in the case of HTS samples. Approaching the Co metallization layer, the content of Cu, Sn,

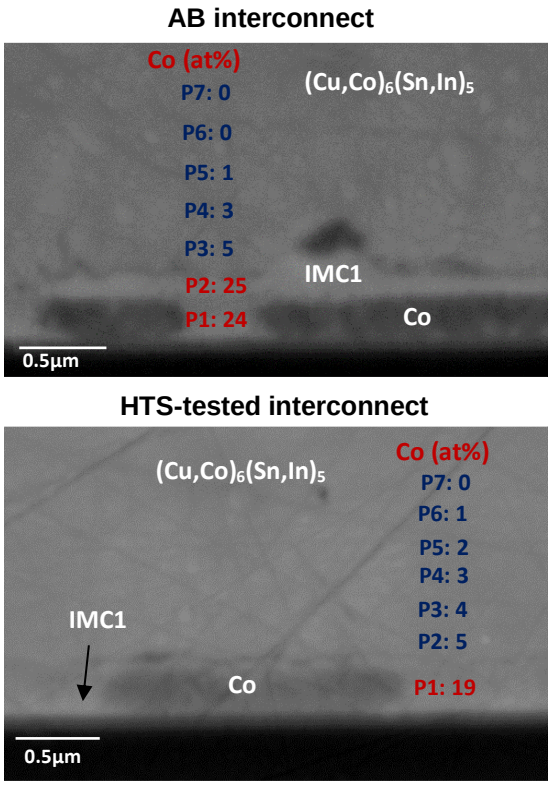

Fig. 7. High-magnification SEM image with EDX point analysis for Cu/Sn-In/Co interconnects after bonding and HTS testing in the vicinity of the Co metallization layer.

and In in the IMCs decreased simultaneously, while the Co content steadily increased from the initial scanning point to the Co metallization layer. A small Co peak was observed in the region where complete Co metallization consumption occurred. These findings suggest that HTS processing leads to a more uniform distribution of all elements across the bond-line.

To obtain a clearer understanding of the IMCs and changes in Co element content across the bond, a high magnification SEM and EDX point analysis was conducted for AB and HTS-tested Cu-Sn-In/Co interconnects in the area close to the Co metallization layer (see **Fig. 7**). The analyzed points p1 to p7 and the corresponding Co content for both AB and HTS-tested samples are presented in Fig. 7. From the SEM image, it was evident that two distinct phases exist: one, $(Cu,Co)_6(Sn,In)_5$, with Co content ranging from 5 at% to 0 at% from the Co side to the Cu side within the bond-line, and the other, a Co-rich phase, appearing brighter in color and situated near the Co metallization layer. For the analyzed p2 in the AB sample, the element atomic percentages are as follows: 53 at% Cu, 25 at% Co, 11 at% Sn, and 11 at% In. This suggests the formation of a new IMC during the bonding process between Co and $(Cu,Co)_6(Sn,In)_5$, with a weak interface with both $(Cu,Co)_6(Sn,In)_5$ and the Ti adhesion layer, as observed through the fracture path in the tensile test. This IMC layer is quite thin, measuring less than 200 nm in thickness above the Co metallization layer and less than 500 nm in regions where all of the Co is fully consumed. However, after the HTS test, this

layer either disappeared or was reduced to less than 50 nm in thickness above the Co metallization layer and less than 300 nm in regions where all of the Co was consumed. Furthermore, there were changes in the atomic percentages of the elements in these regions, with 20 at% Cu, 19 at% Co, 38 at% Sn, and 23 at% In. On the other hand, the Co content in $(Cu,Co)_6(Sn,In)_5$ along the bond-line still ranged from 5 at% to 0 at%, but with a less-steep variation across the bond-line. Co diffused further away from the Co metallization layer and toward the Cu side when compared to the AB sample. These observations suggest that low-temperature Cu-Sn-In/Co bonded samples exhibit a metastable phase near the Co metallization layer, resulting in a weak interface with the adjacent layers. This weak interface can be fully or partially eliminated through the HTS process, making the bond stronger, as observed in the tensile test.

IV. Conclusion

A novel low-temperature Cu-Sn-based SLID interconnect was designed to meet the requirements of 2.5/3D MEMS integration. The utilization of the designed SLID stack (Cu-Sn-In/Co) for 2.5/3D MEMS integration was successfully demonstrated and the thermomechanical reliability of the interconnects was examined. Our findings showed that Cu-Sn-In/Co interconnects primarily consist of $(Cu,Co)_6(Sn,In)_5$, along with a thin Co-rich IMC layer near the Co metallization region. This novel low-temperature interconnect outperforms the Cu-Sn/Co SLID interconnects, which were considered as a reference in this work. In contrast to the Cu-Sn/Co SLID system, no Cu_3Sn phase formation nor voids were observed in the Cu-Sn-In/Co interconnects. The microstructure of low-temperature Cu-Sn-In/Co remains stable, except for a thin layer of a metastable phase near the Co metallization layer, which can be effectively eliminated through extended aging at 150 °C. Furthermore, the tensile strength of the Cu-Sn-In/Co interconnects was adequate, considering the minimum requirement from MIL-STD. While Cu-Sn/Co interconnects initially showed higher tensile strength compared to Cu-Sn-In/Co, the situation reversed during HTS testing. As a result, the novel low-temperature Cu-Sn-In/Co interconnects passed reliability tests involving TS, HTS, and tensile testing. Thus, designing interconnects using the Cu-Sn-In SLID system in contact with the Co metallization layer is a promising approach. The results also highlight the complete Co consumption in certain areas during IMC formation, suggesting potential concerns such as ion migration; therefore, addressing this issue might involve considering a thicker Co metallization layer. Additionally, given that Sn-In has a melting point of 120 °C, it is worth considering lower temperatures, below 200 °C, for Cu-Sn-In/Co SLID interconnects given the successful literature examples of Cu-Sn-In SLID bonding at temperatures as low as 150 °C.

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