A Computationally Efficient Compact Model for Ferroelectric FinFETs Switching with Asymmetric Non-Periodic Input Signals

Shubham Sahay [1], Amol Gaidhane [2], Yogesh Singh Chauhan [2], Raghvendra Dangi [2], and Amit Verma [2]

[1]Indian Institute of Technology Kanpur
[2]Affiliation not available

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Abstract

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Amol D. Gaidhane, *Student Member, IEEE*, Raghvendra Dangi, *Student Member, IEEE*, Shubham Sahay, *Member, IEEE*, Amit Verma, *Member, IEEE* and Yogesh Singh Chauhan, *Fellow, IEEE*

***Abstract*—In this paper, we develop a Verilog-A implementable compact model for the dynamic switching of ferroelectric FinFETs (Fe-FinFETs) for asymmetric non-periodic input signals. We use the multi-domain Preisach Model to capture the saturated $P-E$ loop of the ferroelectric capacitors. In addition to the saturation loop, we model the history dependent minor loop paths in the $P-E$ by tracing input signals' turning points. To capture the input signals' turning points, we propose an $R-C$ circuit based approach in this work. We calibrate our proposed model with the experimental data, and it accurately captures the history effect and minor loop paths of the ferroelectric capacitor. Furthermore, the elimination of storage of each turning point makes the proposed model computationally efficient compared with the previous implementations. We also demonstrate the unique electrical characteristics of Fe-FinFETs by integrating the developed compact model of Fe-Cap with the BSIM-CMG model of 7nm FinFET.**

***Keywords*—Ferroelectric, Compact Model, Fe-FET, Fe-FinFET, Multi-domain, SPICE, Switching, Minor loops**

I. Introduction

Ferroelectric materials are widely used for memory applications due to their non-centro-symmetric structure, which leads to hysteresis in its electrical polarization (P) vs electric field (E) characteristics [1]–[3]. The ferroelectric material transits through an unstable region during the polarization switching, where it exhibits a negative capacitance. This negative capacitance may be stabilized by connecting a resistor or a capacitor in series and harnessed to provide voltage amplification effect when used in the gate stack of FETs [4]–[8]. Such engineered ferroelectric gated transistors offer a steep sub-threshold slope and a higher *ON*-current compared to the conventional FETs and could be a promising candidate for the ultra-low power logic applications [4], [9]–[11]. The high endurance exhibited by the ferroelectric films makes them a promising candidate for storage and emerging applications such as neuromorphic computing, where a large number of history-dependent synaptic weights need to be tuned during the training process [12]–[16]. Further, the recent observations of ferroelectricity in the doped hafnium oxide (HfO_2) materials have attracted much attention for the application in memory devices for neuromorphic applications [12], [17]–[20]. The HFO_2 based ferroelectric FETs exhibit a limited endurance of $\sim 10^5 - 10^7$ cycles which may limit their application for neuromorphic training accelerators. However, FeFETs with such endurance are suitable for memory and inference accelerators. Thus, it is essential to have a computationally efficient compact model of the ferroelectric capacitor (Fe-Cap) for such large scale synaptic devices by accurately capturing the history-dependent minor loops. The physics based models for ferroelectric capacitors has been developed to capture the accurate physical behavior of the Fe-Cap [21], [22]. The compact model of Fe-Cap has already been developed in the literature [23], [24], which captures history dependent minor loops. The model was also based on tracing the evolution of turning points, where each turning point is stored in the form of array. The model further uses the memory wipe-out method [24] to reduce the storage of turning points to improve the computational efficiency of the model. However, for certain combination of asymmetric input signals where the minor loops of $P-E$ look like as a spiral hysteretic curve i.e, the upper and lower voltage turning points keep reducing in magnitude, the model requires large storage of each turning point, which is highly undesirable for large circuit simulation of neural network training.

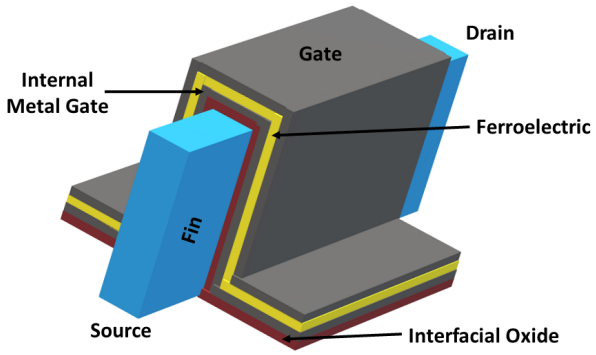

Fig. 1: Schematic of a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) type ferroelectric FinFET (Fe-FinFET).

In this work, we develop a computationally efficient compact model for Fe-Cap with the history-dependent minor loops, which eliminates the stringent requirement of a storage array for any combination of asymmetric input signals. To switch the polarization vs voltage (P-V) loop from forward sweep to reverse sweep or vice-versa, model requires to trace the

A. D. Gaidhane, R. Dangi, S. Sahay, A. Verma and Y. S. Chauhan are with the Department of Electrical Engineering, Indian Institute of Technology Kanpur, Kanpur 208016, India. Email: amold@iitk.ac.in, chauhan@iitk.ac.in.

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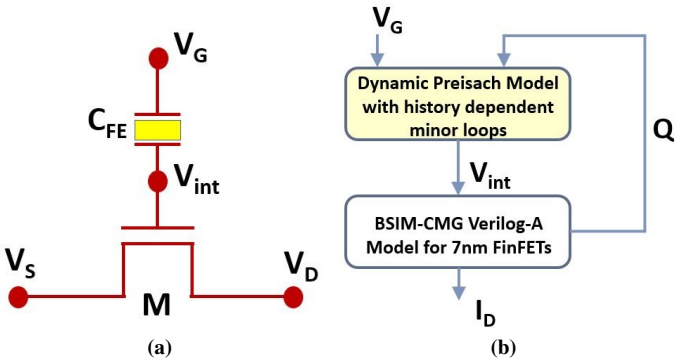


Fig. 2: (a) The presence of internal metal gate in gate stack of Fe-FinFET as shown in Fig. 1 helps to consider two different circuit entities for the model development i.e, Fe-Cap ($C_{\rm FE}$) and underneath baseline FinFET (M). (b) The dynamic Preisach model with history dependent minor loops for Fe-Cap solves self-consistently with the BSIM-CMG model for 7nm FinFET.

turning points in the input signal. In this work, we propose an R-C network to capture the turning points in the input signals. We make the approximations while developing the Fe-Cap model which is discussed in later section, which eliminates the requirement of a storage array for any combinations of asymmetric input signals. The approximation made in the model works very well and accurately captures the experimental results for the complicated input signals. Finally, we demonstrate the Fe-FinFET characteristics by solving the self-consistent solution of the proposed model of Fe-Cap with the industry standard BSIM-CMG model for 7nm FinFET.

II. Model Development of Fe-FinFET

A schematic of metal-ferroelectric-metal-insulator-semiconductor (MFMIS) type of Fe-FinFET is shown in Fig. 1. The internal metal gate present in the gate stack of Fe-FinFET forms an equi-potential surface between the interfacial oxide and the ferroelectric layer, which helps to consider the two different circuit entities i.e, the ferroelectric capacitor ($C_{\rm FE}$) and the underneath conventional FinFET (M) for the modeling of Fe-FinFET as shown in Fig. 2(a). $V_{\rm int}$ is the internal metal gate voltage, and V_G, V_S and V_D are the gate, source and drain terminal bias, respectively. As shown in Fig. 2(b), for the underneath baseline FinFET, we use the industry standard BSIM-CMG Verilog-A model [25], which accurately considers the short channel effects and the quantum mechanical effects into account. We utilize a 7nm open source predictive Process Design Kit (PDK) for the model parameters of conventional FinFET [26]. For the ferroelectric capacitor ($C_{\rm FE}$), we propose a Verilog-A based dynamic Preisach model including the history dependent minor loops, which we discuss in the next section in detail. For each applied gate bias, SPICE simulator solves self-consistently for the gate charge of the underneath FinFET (Q_G) i.e, $Q_G = Q_{\rm FE}$ for each V_G to obtain the electrical characteristics of Fe-FinFET.

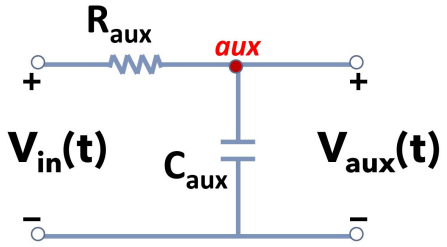


Fig. 3: An R-C circuit to obtain an auxiliary voltage across the ferroelectric layer. The $R_{\rm aux}$ and $C_{\rm aux}$ contributes to the relaxation time ($\tau_v = R_{\rm aux}C_{\rm aux}$) for the auxiliary voltage of Fe-Cap.

III. Model Development of Fe-Cap

A. Modeling of Switching Dynamics in Fe-Cap

To implement the switching dynamics in Fe-Cap, we first calculate the auxiliary voltage ($V_{\rm aux}(t)$) to which the ferroelectric dipoles respond. The SPICE model to obtain ($V_{\rm aux}(t)$) across the ferroelectric layer is shown in Fig. 3. The $V_{\rm aux}(t)$ can be expressed in terms of R-C delay [22], [27] given by

$$V_{\rm aux}(t) = V_{\rm in}(t) - \tau_v \frac{d}{dt} V_{\rm aux}(t) \tag{1}$$

where $V_{\rm in}(t)$ is the applied voltage across the ferroelectric layer, τ_v is the relaxation time for the auxiliary voltage. For the quasi-stationary case, the auxiliary voltage equals to the applied input voltage i.e., $V_{\rm aux} = V_{\rm in}$. To solve the above transcendental equation in a circuit simulator, we define an extra internal node named "*aux*" in the Verilog-A code. The right-hand side (RHS) of (1) is assigned to voltage at node "*aux*" which is solved self-consistently in the circuit simulator resulting in the actual auxiliary voltage $V_{\rm aux}(t)$.

Now, using the auxiliary voltage ($V_{\rm aux}$), we calculate the auxiliary polarization ($P_{\rm aux}$) using the Preisach model [24]. For the forward loop, $P_{\rm aux\uparrow}$ is given by

$$P_{\rm aux\uparrow} = m_\uparrow P_s \times \tanh\left(w(V_{\rm aux} - V_c)\right) + P_{\rm off\uparrow} \tag{2}$$

where V_c and P_s are the coercive voltage and the saturated polarization value of the ferroelectric material, respectively. $m_\uparrow$ is the slope and $P_{\rm off\uparrow}$ is the offset polarization value for the forward sweep. Both $m_\uparrow$ and $P_{\rm off\uparrow}$ are required to obtain the forward sweep minor loops and for the forward sweep saturated loop $m_\uparrow = 1$ and $P_{\rm off\uparrow} = 0$. The forward paths obtained from (2) are indicated by the green arrows in Fig. 5. w in (2) is given as

$$w = \frac{t_{\rm fe}}{2V_c} \ln\left(\frac{P_s + P_r}{P_s - P_r}\right) \tag{3}$$

where $t_{\rm fe}$ is the ferroelectric thickness and P_r is the remnant polarization of the ferroelectric material.

Similarly, for the reverse sweep, the auxiliary polarization $P_{\rm aux\downarrow}$ is written as,

$$P_{\rm aux\downarrow} = m_\downarrow P_s \times \tanh\left(w(V_{\rm aux} + V_c)\right) + P_{\rm off\downarrow} \tag{4}$$

Again $m_\downarrow$ and $P_{\rm off\downarrow}$ are required for the backward sweep minor loops and become $m_\downarrow = 1$ and $P_{\rm off\downarrow} = 0$ for the saturated backward sweep loop. The backward paths obtained from (2)

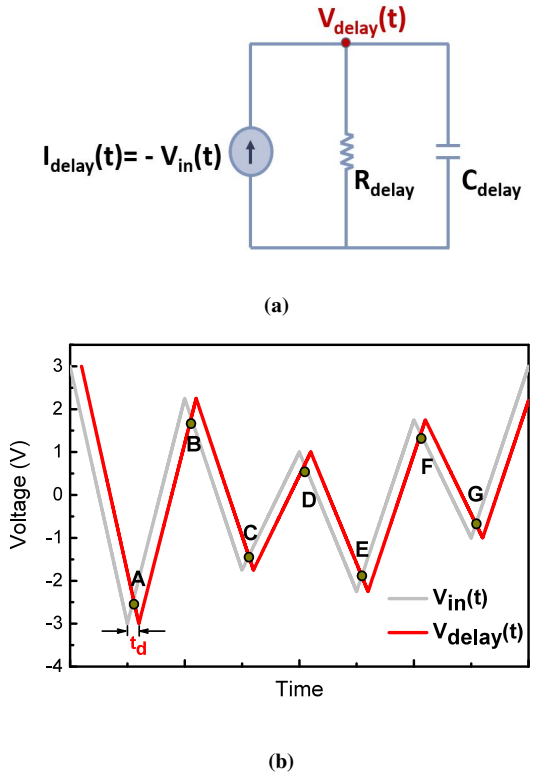


Fig. 4: (a) Proposed R-C circuit to obtain the delayed form of the applied input signal across the ferroelectric capacitor. (b) Tracing the turning points by comparing the delayed voltage from the R-C circuit with the applied input signal.

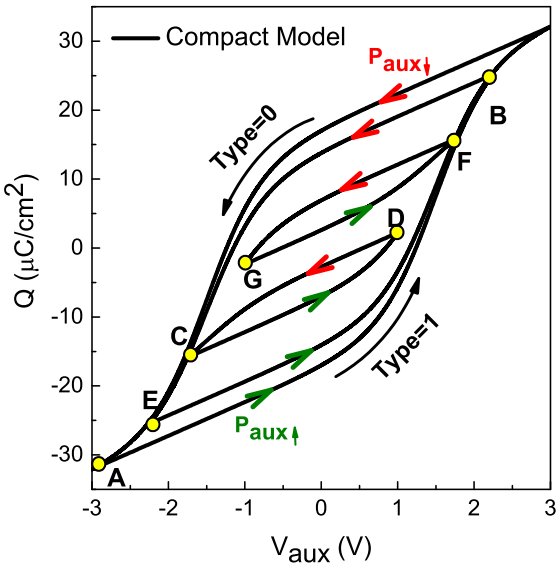


Fig. 5: Simulated Q-$V_{\rm aux}$ from the developed compact model of fe-Cap for the bias scheme shown in Fig. 4(b).

are indicated by the red arrows in Fig. 5. Both $m_{\uparrow}/m_{\downarrow}$ and $P_{\rm off\uparrow}/P_{\rm off\downarrow}$ are calculated using polarization history of the material which is discussed later in this section.

Now the actual ferroelectric charge density($Q(t)$) expression with the inclusion of background permittivity of the ferroelectric material [22], [27] is rearranged as

$$Q(t) = P_{\rm aux} - \tau_p \frac{dP(t)/dt}{1 + \frac{k_n}{t_{\rm fe}}\left|\frac{dV_{\rm aux}(t)}{dt}\right|} + \frac{\varepsilon_{\rm o}\varepsilon_{\rm fe}V_{\rm aux}}{t_{\rm fe}} \qquad (5)$$

where τ_p is the relaxation time of polarization, k_n is the coupling coefficient, and $\varepsilon_{\rm fe}$ is the background permittivity of the ferroelectric material. For the quasi-stationary case, the actual ferroelectric charge in the Fe-Cap is equal to the auxiliary polarization in addition to the dielectric charge component caused due to the internal field. Still, to obtain the complete Q-$V_{\rm aux}$ loop, the model needs to switch the polarization from forward sweep to backward sweep or vice-versa whenever the turning points appear in the input signal.

B. Tracing Turning Points

We propose an R-C circuit to trace the turning points in the input signals as shown in the Fig. 4(a). We define an internal node $delay$ in the Verilog-A code with an aim to find out voltage at node $delay$, where $R_{\rm delay}$ and $C_{\rm delay}$ are the circuit elements which are required to produce delayed version of input voltage at node $delay$. To achieve the delayed input signal, the input voltage at each bias point is fed to the RC circuit in the form of current as shown in the Fig. 4(a). The current source is voltage dependent current source with the proportionality constant α i.e $I_{\rm delay} = -\alpha V_{\rm in}$. The unit of α is Ω^{-1}. After solving Kirchhoff's Current Law (KCL) and differential equation in the R-C circuit, we obtain the voltage $V_{\rm delay}(t)$ at node $delay$ as

$$V_{\rm delay}(t) = I_{\rm delay}(t)R_{\rm delay}(e^{-t/t_d} - 1) \qquad (6)$$

We need the delayed version of the input voltage at node "delay", thus we fed the same input voltage through the current source with $\alpha = 1\Omega^{-1}$. The voltage at node $delay$ (shown by a solid red line) is delayed by $t_d = R_{\rm delay}C_{\rm delay}$ from the actual applied voltage signal (shown by solid gray line) as shown in Fig. 4(b). In this work, we keep $R_{\rm delay} = 1\Omega$ and $C_{\rm delay} = 1fF$, which provides a very small value of t_d in the order of fs. However, to understand the topology, we have shown an exaggerated difference in the input and delayed voltages in Fig. 4(b), which is not the case during the real simulations. Note that the value t_d is very small compared to the relaxation time or domain switching time of the ferroelectric material. Thus, the RC network approach does not lead to significant change in the simulated characteristics from the actual results.

Now, to obtain the turning points, we set the condition during the backward sweep as $V_{\rm delay}(t) < V_{\rm in}(t)$. Whenever this condition is satisfied, we store the input voltage values (pointed by A, C, E, and G) as the lower turning point of the backward sweep. Similarly, we set the condition during the

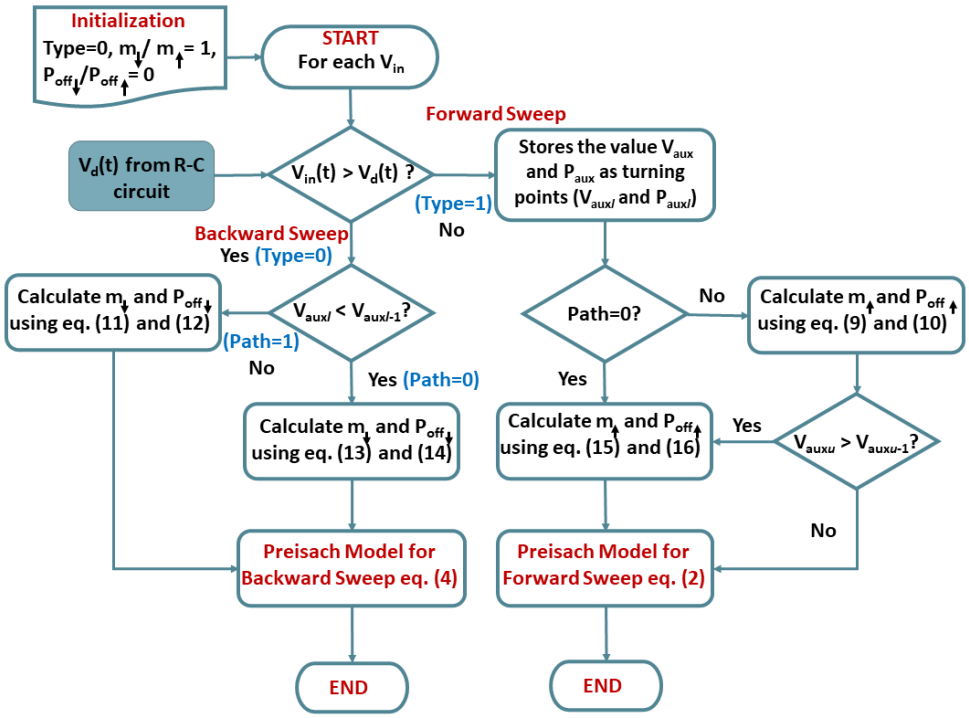


Fig. 6: Complete modeling flowchart of Fe-Cap during the forward and backward sweep.

forward sweep as $V_{\text{delay}}(t) > V_{\text{in}}(t)$ and when the condition becomes true, we store the input voltage values (pointed by B, D and F) as the upper turning points for the forward sweep.

C. Calculation of $m_{\uparrow}/m_{\downarrow}$ and $P_{\text{off}\uparrow}/P_{\text{off}\downarrow}$

In this sub-section, we calculate the $m_{\uparrow}/m_{\downarrow}$ and $P_{\text{off}\uparrow}/P_{\text{off}\downarrow}$ using the turning points obtained in the previous sub-section, which are essential to achieve the history dependent minor loops. The upper and lower voltage turning points are denoted by V_{aux_u} and V_{aux_l} and the corresponding polarization values are denoted by P_{aux_u} and P_{aux_l}, respectively.

In the forward bias, we write the polarization expression at the upper turning point as

$$P_{\text{aux}_{\text{u}}\uparrow} = m_{\uparrow} P_s \times \tanh\left(w(V_{\text{aux}_{\text{u}}\uparrow} - V_c)\right) + P_{\text{off}\uparrow} \quad (7)$$

Similarly, at the lower turning point in forward sweep, we write the polarization as

$$P_{\text{aux}_l\uparrow} = m_{\uparrow} P_s \times \tanh\left(w(V_{\text{aux}_l\uparrow} - V_c)\right) + P_{\text{off}\uparrow} \quad (8)$$

Thus, using (7) and (8), we obtain $m_{\uparrow}$ and $P_{\text{off}\uparrow}$ as

$$m_{\uparrow} = \frac{P_{\text{aux}_u\uparrow} - P_{\text{aux}_l\uparrow}}{P_s\left(\tanh\left(w(V_{\text{aux}_u\uparrow} - V_c)\right) - \tanh(w(V_{\text{aux}_l\uparrow} - V_c)\right)} \quad (9)$$

$$P_{\text{off}\uparrow} = P_{\text{aux}_l\uparrow} - P_s m_{\uparrow} \tanh\left(w\left(V_{\text{aux}_l\uparrow} - V_c\right)\right) \quad (10)$$

Similarly using the backward sweep polarization expression at upper and lower turning points, we can obtain $m_{\downarrow}$ and $P_{\text{off}\downarrow}$ for the backward sweep as,

$$m_{\downarrow} = \frac{P_{\text{aux}_u\downarrow} - P_{\text{aux}_l\downarrow}}{P_s\left(\tanh\left(w(V_{\text{aux}_u\downarrow} + V_c)\right) - \tanh(w(V_{\text{aux}_l\downarrow} + V_c)\right)} \quad (11)$$

$$P_{\text{off}\downarrow} = P_{\text{aux}_u\downarrow} - P_s m_{\downarrow} \tanh\left(w\left(V_{\text{aux}_u\downarrow} - V_c\right)\right) \quad (12)$$

Note the values $m_{\uparrow}$ and $m_{\downarrow}$ are equal to 1 for the saturated loop and becomes less than 1 for the minor loops. And the values of $P_{\text{off}\uparrow}$ and $P_{\text{off}\downarrow}$ are equal to 0 for the saturated loop and become non-zero for the minor loops.

D. Modeling Flow for History Dependent Minor Loops

Fig. 6 describes working of the model at each bias point in both forward and backward sweeps. To explain the model flow, we consider an asymmetric input signal given in Fig. 4(b). The Q-V_{aux} characteristics obtained from the developed compact model is shown in Fig. 5. We initialize backward sweep ($Type = 0$), and $m_{\uparrow}/m_{\downarrow} = 1$ and $P_{\text{off}\uparrow}/P_{\text{off}\downarrow} = 0$ for the saturated loop. $Type = 0$ and $Type = 1$ in the model flowchart imply the backward and forward sweeps, respectively. So, when the applied input signal varies from 3V to -3V, $P_{\text{aux}\downarrow}$ is calculated from (4) with $m_{\downarrow} = 1$ and $P_{\text{off}\downarrow} = 0$ until the applied bias reaches to the first turning point A as shown in Fig. 4(b). Once the condition $V_{\text{delay}}(t) - V_{\text{in}}(t) < 0$ is satisfied during the backward sweep, model now switches to the forward sweep i.e. $Type = 1$. At this bias point, model will store the polarization as $P_{\text{aux}_1\uparrow}$ and voltage as $V_{\text{aux}_1\uparrow}$ as the turning points. Thus, $P_{\text{aux}\uparrow}$ is calculated from (2) using $m_{\uparrow}$ and $P_{\text{off}\uparrow}$ from (9) and (10) using the stored $P_{\text{aux}_1\downarrow}$ and

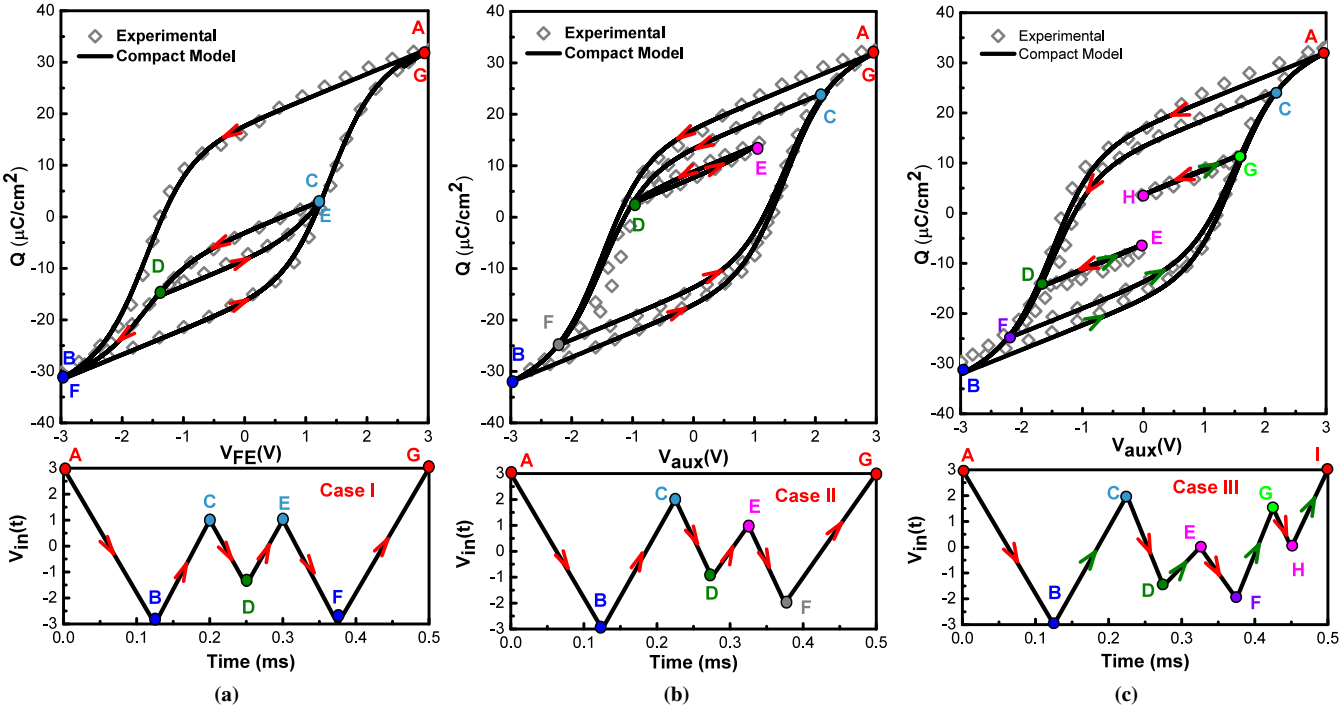


Fig. 7: Validation of simulated P_{aux}-V_{aux} with a 10nm HfO_2 based ferroelectric material experimental results [23] for three different non-periodic asymmetric input signals (a) case I, (b) Case II, and (c) case III.

$V_{\text{aux}_l\downarrow}$ at point A, and uses $P_{\text{aux}_u\uparrow}$ at $V_{\text{aux}_u\uparrow} = 3\text{V}$ as another turning point. The forward sweep continues till the next the turning point B. When the model recognized a turning point at B, it will wipe out the previously stored $P_{\text{aux}_u\uparrow}$ and $V_{\text{aux}_u\uparrow}$ and overwrite the new values of turning points obtained at B. As the polarization $P_{\text{aux}\uparrow}$ does not reach to the saturation polarization value during the forward sweep, thus for the next backward sweep, model works in the minor loop with $m_\downarrow < 1$ and non zero $P_{off_\downarrow}$. Next, model calculates the $m_\downarrow$ and $P_{off_\downarrow}$ using new turning points obtained at B and the previously stored $P_{\text{aux}_l\downarrow}$ and voltage as $V_{\text{aux}_l\downarrow}$ at point A till point C. Model further experiences the turning point at point C and works in the forward minor loop, where it overwrites the previous turning points as $P_{\text{aux}_l\downarrow}$ and $V_{\text{aux}_l\downarrow}$ stored at A. Next, for the forward loop between point C and D, it uses the recent turning points stored at points B and C. Similarly, for the backward loop starting at D uses the turning points stored at C and D and overwrites the previous turning points stored at B.

Now, when the bias takes a path between point D to E, model uses the turning points stored at C and D till it reaches to point C. Once, the bias reaches to point C, we flag the backward sweep as $path = 0$ and use the modified expression for $m_\downarrow$ and $P_{off_\downarrow}$ using (13) and (14), respectively. For the modified $m_\downarrow$ and $P_{off_\downarrow}$, model uses the turning points stored at C as one of the turning points. Further, model takes the second turning point as a maximum negative value of applied bias, since the polarization eventually converges at the saturation polarization at maximum negative value of applied bias. Thus, model changes slope for the downward sweep and follows the path between the points C and E. However, in the previous models, to calculate the slope of $path = 0$, it uses the turning point stored at A and B. Therefore, it requires the storage of multiple previous turning points in the form of array. Hence, using this approximation, we eliminate the need of storage of turning points while switching from inner loop to minor loop. The modified expressions of $m_\downarrow$ and $P_{\text{off}\downarrow}$ for $path = 0$ are given by

$$m_\downarrow = \frac{P_{\text{aux}_l\downarrow} - (P_s \times \tanh\left(w\left(-|V_{\max}| + V_c\right)\right))}{P_s\left(\tanh\left(w(V_{\text{aux}_l\downarrow} + V_c)\right) - \tanh(w(-|V_{\max}| + V_c)\right)} \tag{13}$$

$$P_{\text{off}\downarrow} = P_{\text{aux}_l\downarrow} - P_s m_\uparrow \tanh\left(w\left(V_{\text{aux}_l\uparrow} + V_c\right)\right) \tag{14}$$

At point E, the model enters in the forward loop and at this bias point model notices that the backward sweep for the last bias point was flagged as a $path = 0$. For $path = 0$ condition, model calculates the slope using the turning points stored at E and the second turning point predicts as maximum positive applied potential ($V_{\max}$). As mentioned earlier, the polarization has to converge the saturation polarization value for maximum positive applied bias. Thus, the modified definitions of $m_\uparrow$ and $P_{\text{off}\uparrow}$ for $path = 0$ are given by

$$m_\uparrow = \frac{P_{\text{aux}_l\downarrow} - (P_s \times \tanh\left(w\left(V_{\max} - V_c\right)\right))}{P_s\left(\tanh\left(w(V_{\text{aux}_l\downarrow} - V_c)\right) - \tanh(w(V_{\max} - V_c)\right)} \tag{15}$$

$$P_{\text{off}\uparrow} = P_{\text{aux}_l\downarrow} - P_s m_\uparrow \tanh\left(w\left(V_{\text{aux}_l\uparrow} - V_c\right)\right) \tag{16}$$

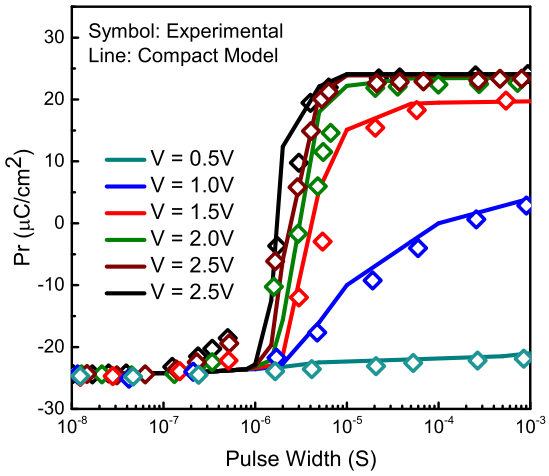


Fig. 8: The response of remnant polarization of the ferroelectric material (P_r) for different pulse widths and amplitudes.

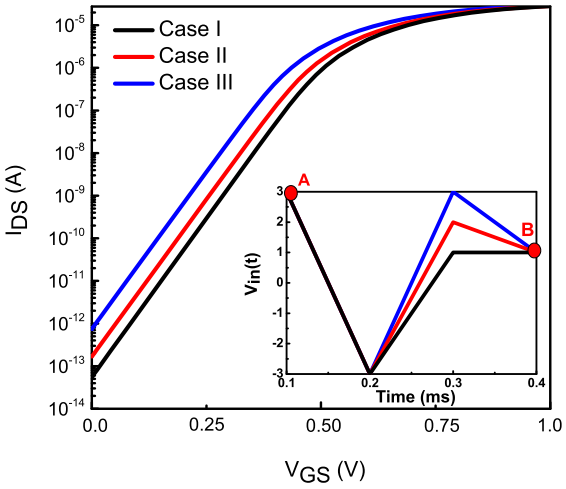
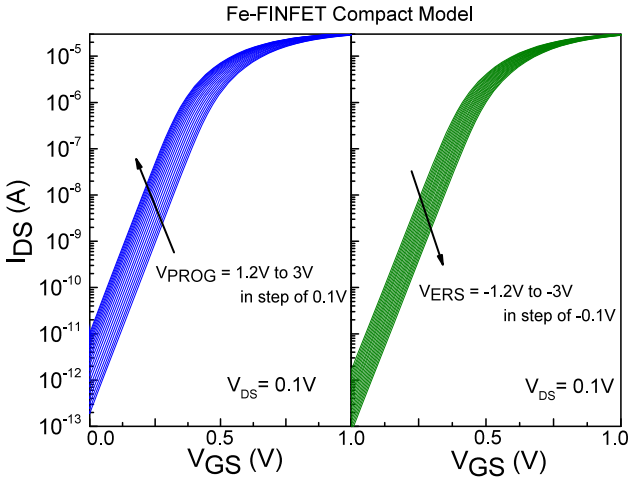
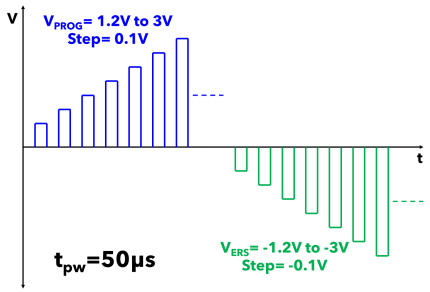


Fig. 9: History-dependent drain current characteristics of Fe-FinFET during the read process for the three different cases. The biasing scheme is shown in the inset figure, where the initial and final bias points are same, however all the three cases follow the different path.

The model uses the above definition of $m_{\uparrow}$ and $P_{\text{off}\uparrow}$ till the bias reaches to F. Again, at point F, model faces the turning point and enters in the backward sweep, it uses the turning points stored at point E and F to calculate $m_{\downarrow}$ and $P_{\text{off}\downarrow}$ till bias reaches at G. At G, model uses the stored turning points at F and G for the forward sweep till point F. After point F, model flagged as $path = 0$ and hence, uses the first turning point stored at F and second it predicts as maximum applied bias i.e. 3V.



(a)



(b)

Fig. 10: (a) The I_{DS}-V_{GS} characteristics obtained during the read process of Fe-FinFET for each polarization state during the programming and erasing voltages. (b) The biasing scheme for programming (shown in blue color) and erasing (shown in green color) cycles.

IV. Model Validation and Discussion

Now, the compact model developed for Fe-Cap in the last section is validated for the different complicated asymmetric input signals against the experimental results of the 10nm HfO_2 based Fe-Cap as shown in Fig. 7. We validate our model for three different input signals which are shown in Fig. 7. We consider the quasi-stationary case, where the relaxation time constants are much smaller compared to the applied input pulse width. The model shows excellent agreement with the experimental data for all three cases. Further, the response of remnant polarization of the ferroelectric material (P_r) for different pulse widths are demonstrated in Fig. 8. The simulated P_r response for different pulse widths and amplitudes shows good agreement with the experimental results [23]. For the validation purpose, we consider the relaxation time of auxiliary voltage (τ_v) as 1.5μs whereas we ignore the relaxation time of polarization (τ_p), since the dielectric relaxation in the HfO_2 layer dominates only at very high frequency of operation ($>$ 1GHz) [28], [29].

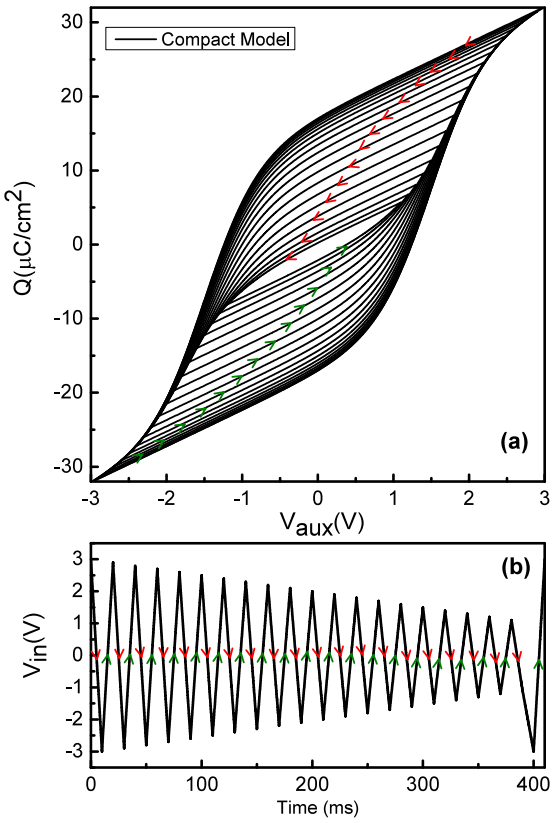


Fig. 11: (a) A spiral hysteretic Q-$V_{\rm aux}$ curve obtained from both the models (b) An asymmetric applied input pulse to obtain the spiral hysteretic curve.

Next, we demonstrate the transfer characteristics of Fe-FinFET by jointly solving the developed compact model of Fe-Cap with BSIM-CMG model of FinFET. To obtain the drain current characteristics of Fe-FinFET, we use the model parameters of 7nm conventional FinFET and keep $t_{\rm fe} = 3$nm. Fig. 9 shows the history dependent drain current characteristics of Fe-FinFET for three different cases. The biasing scheme is shown in the inset figure of Fig. 9. Each case has the same initial and final bias point, however it follows a different path to reach the final bias point. The drain current in Fig. 9 is obtained during the read process for all three different cases. The drain current of Fe-FinFET heavily depends on the history-dependent polarization states and shows significant difference for each case.

Fig. 10(a) shows the $I_{\rm DS}$-$V_{\rm GS}$ for the program and erase voltages at $V_{\rm DS} = 0.1$V. For programming voltages, we increase the amplitude of $V_{\rm PROG}$ from 1.2V to 3V with the increment of 0.1 V as shown by the blue color in Fig. 10(b). We keep the pulse width of each pulse as 50μs. The drain current for each polarization is read after each programming pulse and plotted in Fig. 10(a). Similarly, we apply the erase pulse from -1.2V to -3V in step of -0.1V shown by green color in Fig. 10(b). The drain current for each polarization state after each erasing pulse is shown in Fig. 10(a). In comparison to the erasing pulse, OFF current increases significantly for high programming pulse due to the gate induced drain leakage (GIDL) effect [25]. Also, the change in the drain current for subsequent programming pulses is higher as compared to the change with the erase pulses due to the GIDL effect.

Simulations	Computation Time	Memory Allocation
At device level [23]	5.21 sec	38.5 MB
At device level (This work)	2.05 sec	38.4 MB
At circuit level [23]	23 min 10 sec	1.02 GB
At circuit level (This work)	19 min 34 sec	404 MB

TABLE I: Computation Time and Memory allocation required for the circuit simulator. Our model is faster at the device level and consumes less memory especially at the circuit level.

Furthermore, to compare the efficiency of the proposed model in terms of memory requirement and computational time as compared to the prior implementation [23], we have performed device as well as circuit simulations. At the device level, we simulate the Fe-Cap model for the specific asymmetric input signal shown in Fig. 11(b). We consider the asymmetric input pulse for which the model produces the spiral hysteretic $Q - V_{\rm aux}$ curve. The obtained $Q - V_{\rm aux}$ from both the models are shown in Figure Fig. 11(a). For such input pulse, the model present in [23] requires the storage for each turning points which increases the computational time and the memory requirement. TABLE I shows the comparison of simulation time and memory allocation required for the applied input pulse for both the models. So, our model requires significantly less computational time compared to the model which required storage of turning points. However, we can not see any significant difference in memory allocation by the circuit simulator at the device level. Further, the performance gains while using the proposed model is more evident at the circuit level. We perform an array level simulation for a 100×100 crossbar array of Fe-FinFET to compare the computational time and memory requirement for both models. The comparison is shown in TABLE I. In view of the above, we believe that the proposed modeling approach leads to significant performance gains in terms of computational time and the memory requirement especially when handling large array-level circuit simulations.

V. Conclusion

We have formulated a computationally efficient compact model for Fe-Cap and implemented Fe-FinFET with the conventional FinFET in Verilog-A code for large scale circuit simulations. The proposed model is validated for the history dependent minor loops with the experimental results for the non-periodic asymmetric input signals. In comparison with the previous compact models, we eliminate the need of storage

of previous turning points. The model developed for the Fe-Cap further can be implemented with the other industry standard models of different FET structures and may serve as the platform for design exploration of FeFETs for several unconventional applications.

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