Ultra-Compact Neural Network ADC Exploiting Ferroelectric FET

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Abstract

Development of ultra-compact, low-to-medium precision analog-to-digital converters (ADCs) with unprecedented energy-efficiency is essential to meet the ever-increasing demand for data converters in advanced computing systems including neuromorphic accelerators based on emerging non-volatile memories. To this end, in this work, for the first time, we propose a feedforward neural network ADC based on a network of highly scalable, CMOS-compatible, and energy-efficient ferroelectric-FinFET (Fe-FinFET) synaptic elements. Our lower triangular neural network (LTNN) ADC design, implemented using 7-nm technology from ARM along with an experimentally calibrated compact model for Fe-FinFETs, consumes 5.44 μW of power, 1.03 μm^2 of area while operating at a speed of 1.23 megasamples per second for 4-bit precision. The proposed neural network ADC may pave the way for realization of highly efficient neuromorphic processing engines and neuro-optimizers based on cross-point array of emerging non-volatile memories.

Ultra-Compact Neural Network ADC Exploiting Ferroelectric FETs

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***Abstract*—Development of ultra-compact, low-to-medium precision analog-to-digital converters (ADCs) with unprecedented energy-efficiency is essential to meet the ever-increasing demand for data converters in advanced computing systems including neuromorphic accelerators based on emerging non-volatile memories. To this end, in this work, for the first time, we propose a feedforward neural network ADC based on a network of highly scalable, CMOS-compatible, and energy-efficient ferroelectric-FinFET (Fe-FinFET) synaptic elements. Our lower triangular neural network (LTNN) ADC design, implemented using 7-nm technology from ARM along with an experimentally calibrated compact model for Fe-FinFETs, consumes 5.44 µW of power, 1.03 µm^2 of area while operating at a speed of 1.23 megasamples per second for 4-bit precision. The proposed neural network ADC may pave the way for realization of highly efficient neuromorphic processing engines and neuro-optimizers based on cross-point array of emerging non-volatile memories.**

***Index Terms*—Hopfield neural network, Ferroelectric FinFET, ADC, Feedforward, Successive approximation.**

I. Introduction

ANALOG-to-digital converters (ADCs) form an integral part of the internet-of-things (IoT) ecosystem with a wide range of applications ranging from mobile IoT devices, wireless sensor nodes, communication systems including receivers and base stations, Ethernet, modems, DSL to video processing systems in HDTVs and CCD/ultrasonic medical imaging systems. Moreover, ADCs are inevitable while designing compute-in-memory primitives such as inference/multiply-accumulate (MAC) accelerators based on the cross-point array of emerging non-volatile memories [1]–[5]. ADCs are required at each column of the cross-point array and often dominate the area and energy landscape of such neuromorphic processing engines limiting their area- and energy-efficiency, and the computational precision [6]–[9]. Therefore, there is an urgent need for ultra-compact and energy-efficient ADCs to realize the true potential of the advanced computing and communication systems.

A neural circuit consisting of a (synaptic) network of analog processors (neurons/decision elements), also known as the Hopfield neural network, with capability of solving optimization problems including decision/decomposition problems and linear programming problems was proposed in [10]. Furthermore, a simple ADC design utilizing the Hopfield neural network was also proposed [10]. However, the Hopfield ADC output exhibits hysteresis if the inputs are not reset before each calculation and tends to settle at local minima leading to spurious states and degradation in the conversion accuracy [10], [11]. Moreover, the variations in the input capacitance and the delay of neurons may lead to oscillatory behavior in Hopfield ADCs [12]. To mitigate the spurious outputs and oscillations arising due to the feedback in Hopfield neural networks, a feedforward lower triangular neural network (LTNN) ADC based on the successive approximation technique was proposed [11]. The LTNN ADC can be considered as the neural circuit equivalent of the SAR ADC.

However, the number of synaptic elements in a LTNN ADC increases quadratically with the ADC resolution ($n(n-1)/2$ for n-bit LTNN ADC). Moreover, the synaptic elements must exhibit a high dynamic range ($O(2^n)$) and support precise conductance-state tuning. While the digital implementation of such synaptic elements incurs a significant area and energy overhead, the analog CMOS implementations are susceptible to mismatch and process variations [13]. The emerging analog-grade non-volatile memories such as phase change memory (PCM), resistive RAMs (RRAMs), etc. appear promising for implementation of synaptic elements owing to their low footprint, CMOS-compatibility, and ability to tune the conductance-state using program-verify algorithm. Therefore, Hopfield neural networks utilizing PCM devices and RRAMs as synaptic elements were proposed recently [12], [14]–[18]. However, while the PCM devices exhibit a large cell current degrading the energy-efficiency of the synaptic network, RRAM devices suffer from a large temporal and spatial variability and their dynamic range is limited [8], [19]. Moreover, large scale back-end-of-line (BEOL) CMOS-integration of these NVMs introduces significant fabrication complexity and poses a technological challenge.

The recent discovery of ferroelectricity in doped-hafnium oxide stacks has propelled the development of ferroelectric FET based memories for storage. Considering the high scalability, ease of large scale CMOS integration, polarization tuning capability utilizing gate and drain program/erase schemes and ultra-low power consumption of the ferroelectric memories [20]–[23], it becomes imperative to explore their application as synaptic elements in neural circuits. Moreover, although several Hopfield ADC implementations utilizing digital, thin film, metal interconnects and PCM/RRAM based synaptic elements have been explored [12], [18], to the best of our knowledge, the hardware implementation of a feedforward LTNN ADC is still elusive.

To this end, in this work, for the first time, we pro-

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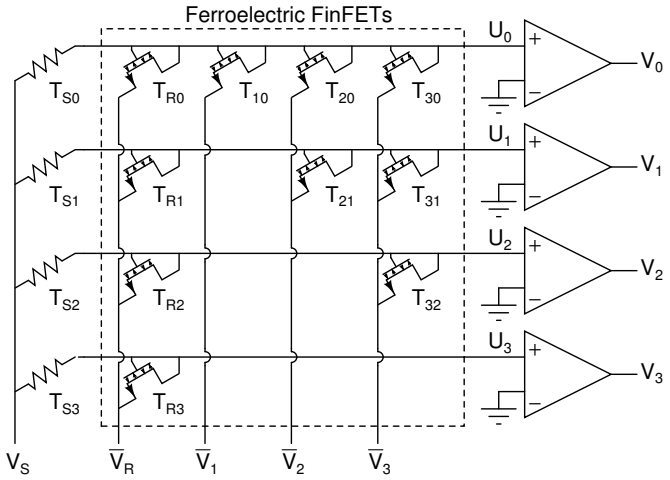

Fig. 1. Architecture of a 4-bit LTNN ADC using Fe-FinFET synapses.

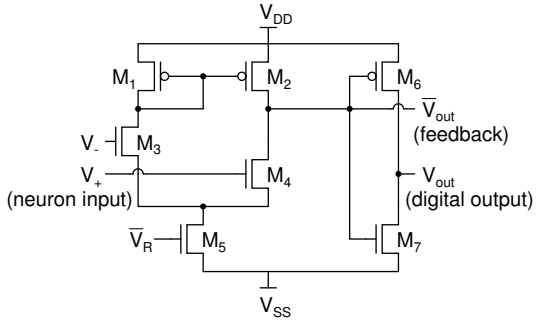

Fig. 2. The proposed neuron circuitry.

pose a feedforward neural network ADC with a network of ferroelectric-FinFET (Fe-FinFET) synapses based on doped-hafnium oxide stack. We also design a neuron circuit (decision element) to ensure data conversion without disturbing the pre-programmed polarization-state of the Fe-FinFETs in the proposed ADC. Our extensive analysis utilizing an experimentally calibrated compact model for Fe-FinFETs and the 7-nm ASAP PDK from ARM for CMOS neuron indicates that the proposed feedforward LTNN ADC consumes 5.44 μW of power and 1.03 μm^2 of area while operating at a speed of 1.23 megasamples per second for a 4-bit precision which is sufficient for practical neuromorphic inference accelerators [24].

The manuscript is organized as follows: the architecture of the feedforward LTNN ADC is discussed in section II. The structure and modeling approach for Fe-FinFETs are described in section III. The results of our extensive analysis of the proposed feedforward neural network ADC exploiting Fe-FinFETs for performance metrics such as area, speed and power consumption are presented in section IV and the conclusions are drawn in section V.

II. Feedforward LTNN ADC Architecture

The schematic view of a feedforward LTNN ADC is shown in Fig. 1. It consists of a grid of resistive elements $T_{S0,\ldots,3}$ and $T_{R0,\ldots,3}$, synapses (weights) $T_{10,\ldots,32}$ ($n(n+1)/2$ for n-bit ADC) and neurons (n decision elements for n-bit ADC). Each neuron is fed the analog voltage to be converted, V_S, via $T_{S0,\ldots,3}$, a negative reference voltage V_R via $T_{R0,\ldots,3}$, and the (complementary) outputs from other neurons V_1, V_2, V_3, V_4 through the synaptic elements $T_{10,\ldots,32}$. The input voltage V_S is converted to a digital output with V_0 as the LSB and V_3 as the MSB. The feedforward LTNN ADC implementation works on the principle of successive approximation [11], where the MSB is first determined and the information is then used to determine the lower significant bits. Since a lower significant bit does not influence a more significant bit, the synaptic elements are not used in the lower triangular portion of the grid. This results in a feedforward neural network which eliminates the issues with the Hopfield ADCs with feedback such as oscillations and metastability of the output.

The dynamics of the LTNN ADC can be described by

$$C\dot{U_j} = -\sum_{i=j+1}^{N-1} T_{ij}V_i - T_jU_j + I_j \tag{1}$$

where

$$I_j = T_{Sj}V_S - T_{Rj}V_R \tag{2}$$

$$T_j = T_{Sj} + T_{Rj} + \sum_{i=j+1}^{N-1} T_{ij} \tag{3}$$

$$V_j = g(U_j) \tag{4}$$

where C is the input capacitance of the neuron circuit, N is the number of bits of the ADC and $g(\cdot)$ represents the transfer function of the neuron. The optimal set of conductance values for the resistive elements and the synapses can be obtained as [12]:

$$T_{ij} = 2^i, \quad T_{Ri} = 2^i, \quad T_{Si} = 1. \tag{5}$$

It may be noted that the implementation of synapses is critical to the area and power consumption of the proposed ADC since the number of synapses scales as $O(n^2)$ for an n-bit ADC, compared to the number of neurons ($O(n)$). Therefore, we propose to implement the synapses (and resistive elements) using Fe-FinFETs with ultra-low area and high scalability.

Also, the update rule for the i-th neuron can be given as:

$$V_i = 1 \quad \text{if } \left(V_S - \sum_{j=i+1}^{3} 2^jV_j\right) \geq 2^i \tag{6}$$

$$= 0 \quad \text{otherwise.} \tag{7}$$

The neurons act as decision elements and generate a feedback voltage $\bar{V_i}$ which is applied to the synapses. We have designed a differential amplifier based neuron as shown in Fig. 2 to ensure data conversion without altering the pre-programmed polarization-state of the Fe-FinFETs in the proposed ADC. The final digital output is generated from $\bar{V_i}$ using a CMOS inverter.

III. Fe-FinFET Structure and Modeling Approach

The 3D view of the ferroelectric FinFET is shown in Fig. 3(a). It consists of an additional ferroelectric layer of doped-hafnium oxide ($HfZrO_x$) in the gate stack. The polarization-state of the ferroelectric layer dictates the threshold voltage

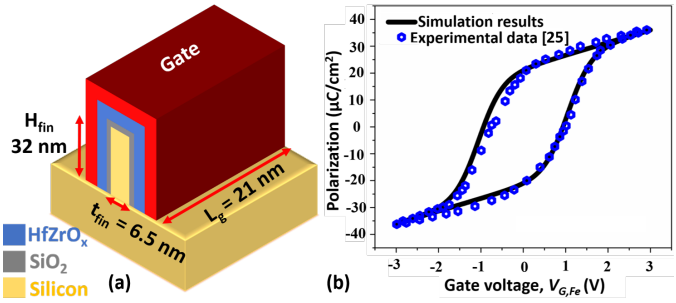

Fig. 3. (a) 3D-view of the Fe-FinFET with $HfZrO_x$ ferroelectric layer and (b) Calibration of compact model parameters by reproducing the experimental results of $HfZrO_x$ ferroelectric capacitor [25]

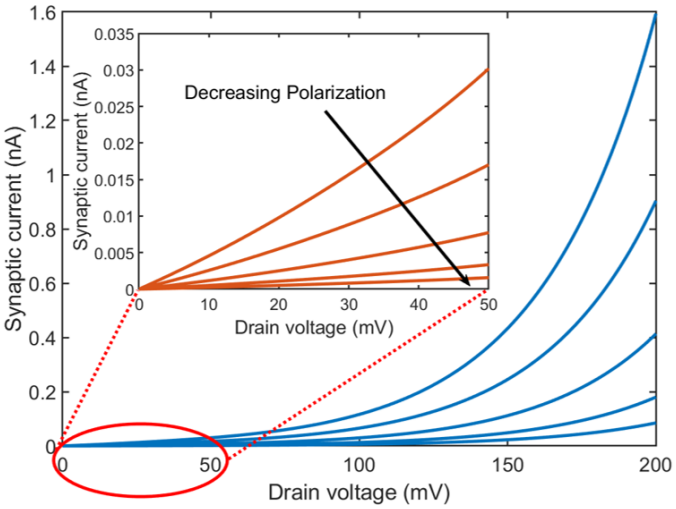

Fig. 4. Output characteristics of the Fe-FinFET synapse for different polarization-states.

and may be tuned with the help of electrical pulses applied at the gate and drain terminals [23], [26], [27]. $HfZrO_x$-based ferroelectric FETs with a capability of tuning the weights (conductance states) with more than 5-bit precision have already been experimentally demonstrated [25], [27]. In this work, we have utilized an experimentally calibrated compact model for Fe-FinFETs [28] which accurately captures the static polarization characteristics, program/erase behavior, temporal dynamics during transient analysis and the history effect of a $HfZrO_x$ stack [26]. The parameters of the compact model have been tuned to reproduce the experimental characteristics of the $HfZrO_x$-based ferroelectric capacitor reported in [25] and shown in Fig. 3(b).

The output characteristics of the proposed Fe-FinFET synapse (where Fe-FinFET is in the diode-connected configuration as shown in Fig. 1) for different polarization-states of the ferroelectric $HfZrO_x$ layer, obtained using the experimentally calibrated compact model [28], are shown in Fig. 4. As can be observed from Fig. 4, the output characteristics of the proposed Fe-FinFET synapse are highly linear for lower range of drain voltages ($V_D < 50$ mV) which facilitates the application of Fe-FinFETs as efficient synapses and resistive elements in the proposed LTNN ADC.

TABLE I
NONLINEARITY OF ADC OUTPUT

No. of bits	Max differential nonlinearity	Max integral nonlinearity
2	0.008 LSB	0.005 LSB
3	0.18 LSB	0.14 LSB
4	0.28 LSB	0.24 LSB
5	0.62 LSB	0.45 LSB
6	1.18 LSB	1.09 LSB

TABLE II
PERFORMANCE METRICS

No. of bits	Area (μm^2)	Speed (samples/s)	Energy/sample (pJ)
2	0.31	7.09×10^5	3.84
3	0.52	1.12×10^6	3.63
4	0.76	1.23×10^6	4.42
5	1.03	7.94×10^5	8.57
6	1.34	4.67×10^6	1.75

IV. RESULTS AND DISCUSSION

Utilizing the experimentally calibrated compact model for Fe-FinFETs [28] and the 7-nm technology PDK from ARM [29] for CMOS circuits, we have performed an extensive analysis of the proposed LTNN ADC (Fig. 1) based on the Fe-FinFET synapses and the neuron circuitry shown in Fig. 2. The polarization-state of the Fe-FinFET synapses (and resistive elements) are first tuned to program their conductance value to the desired values obtained from equation (5). The neuron circuit is designed such that the maximum voltage drop across the Fe-FinFETs is 50 mV. This ensures proper operation of the proposed ADC without changing the pre-programmed polarization-state and conductance of the Fe-FinFET synapses and resistive elements during data conversion. In addition, a low voltage across the Fe-FinFET synapses also leads to higher linearity in their output characteristics leading to an efficient ADC design. Low-to-medium precision LTNN ADCs based on Fe-FinFET synapses were designed following this approach.

The simulation results for the output of the proposed Fe-FinFET based LTNN ADC with different output-bit precision are shown in Fig. 5. As can be observed from Fig. 5, the outputs obtained via simulations deviate from the ideal ADC characteristics as the output-bit precision increases.

Furthermore, to quantify the accuracy of the proposed LTNN ADC, we have used two standard metrics: differential and integral non-linearity. While differential non-linearity (DNL) is the difference between the step width of the ADC output and the ideal ADC characteristics, the integral non-linearity (INL) is the deviation of the ADC transfer function from the transfer function of an ideal ADC i.e. a straight line. The maximum values of the differential and integral non-linearity for the proposed ADC are outlined in Table I. Both DNL and INL increase and the accuracy degrades for the proposed Fe-FinFET based LTNN ADC with an increase in the output-bit precision.

Moreover, we have also analysed important performance metrics such as area, speed and power consumption of the proposed LTNN ADC for different output-bit precisions (Table II) and compared them against state-of-the-art ADCs from

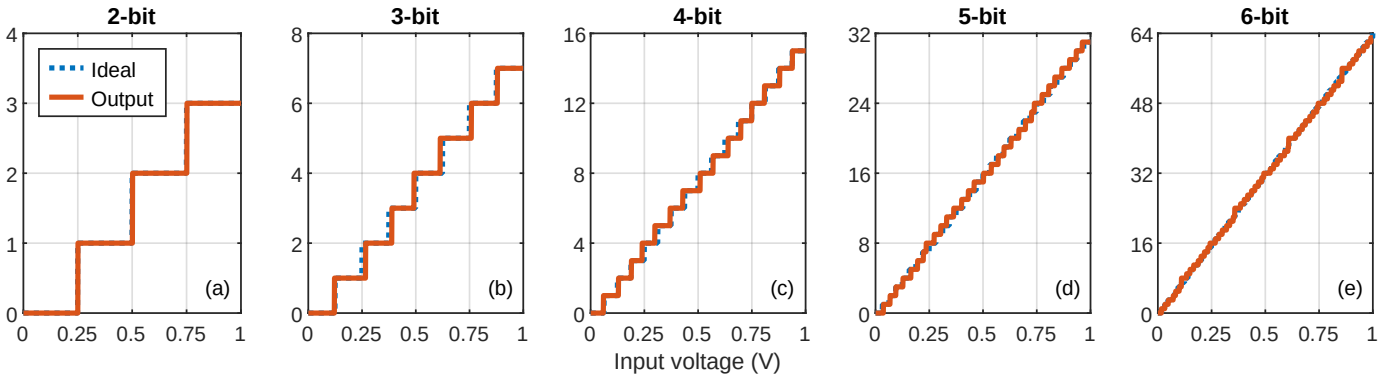

Fig. 5. The simulated ADC output for different output-bit precision: (a) 2-bit, (b) 3-bit, (c) 4-bit, (d) 5-bit, (e) 6-bit.

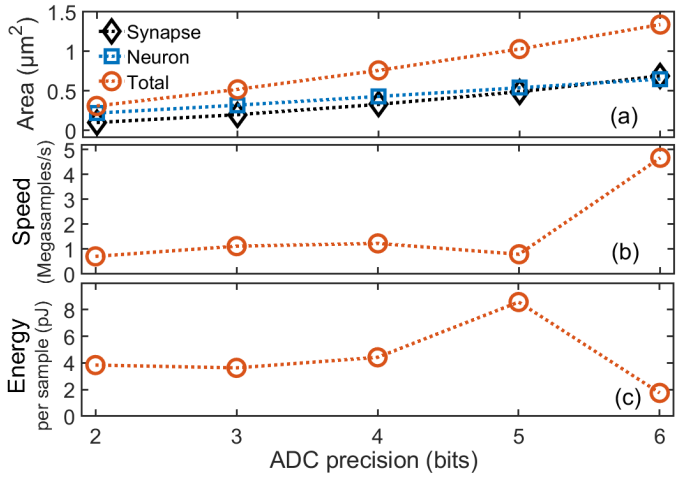

Fig. 6. Performance metrics of the proposed ADC: (a) area, (b) speed and (c) energy.

TABLE III
AREA OCCUPIED BY NEURONS AND SYNAPSES

No. of bits	Neuron area (μm²)	Synapse area (μm²)
2	0.22	0.10
3	0.32	0.20
4	0.43	0.33
5	0.54	0.49
6	0.65	0.69

TABLE IV
POWER CONSUMED BY NEURONS AND SYNAPSES

No. of bits	Neuron power (μW)	Synapse power (pW)
2	2.72	0.76
3	4.08	3.37
4	5.44	8.99
5	6.80	11.9
6	8.16	153

a comprehensive survey [30].

A. Area

The area of the proposed ADC with different output-bit precision was obtained from the layouts using the 7-nm technology PDK from ARM. The baseline FinFET from the PDK was utilized for representing Fe-FinFETs in the layout. The total area of the proposed ADC for different output-bit precision are reported in Table II. Furthermore, the contribution of the neurons and synaptic elements in the areal landscape is also shown in Table III. The area occupied by the synapses increases quadratically with increasing output-bit precision, while the area occupied by the neurons increases linearly. Also, the synapses dominate the areal landscape for the proposed ADC with higher output-bit precision ($>$ 5-bit) as shown in Fig. 6(a). Therefore, utilization of highly scalable and ultra-compact Fe-FinFETs as synaptic elements provides an inherent scaling-benefit. Moreover, the silicon footprint for the proposed Fe-FinFET based LTNN ADC with a 6-bit precision is 1.34 μm^2, which is significantly smaller as compared to the conventional ADC [31] with lowest area (580 μm^2) reported in the comprehensive survey of ADCs [30].

B. Speed

We also investigated the speed (in terms of the number of input voltage samples that can be processed per unit time) of the proposed ADC with different output bit precision as shown in Fig. 6(b). We observe that the speed of the proposed ADC increases significantly as the output-bit precision increases from 5-bit to 6-bit. This is attributed to the technique used for mapping the required Fe-FinFET synaptic resisances for the LTNN ADC. According to equation (5), the resistances corresponding to the synapses in the LTNN ADC should be tuned in the ratio $1 : 2 : \ldots : 2^{n-1}$. While tuning the polarization-states of the Fe-FinFETs to realize the synaptic resistances that fit best to this particular ratio for 6-bit ADC, we found that majority of the Fe-FinFET synapses exhibit a lower resistance value. This results in a lower time constant (RC) and a sharp increase in the speed for 6-bit ADC. Whereas for the 5-bit ADC design, after tuning the polarization-states for Fe-FinFETs to fit the required resistance ratio, we found that most of the synapses exhibit higher resistances leading to a reduced speed.

C. Power Consumption

The power consumed by the neurons and synapses of the proposed Fe-FinFET based LTNN ADC with different output-

bit precision are shown in Table IV. Although the power consumed by the synaptic elements increases quadratically with increasing output-bit precision of the ADC, it is considerably small as compared to the power consumed by the neuron circuitry (which increases linearly with output-bit precision). The extremely high energy-efficiency of the Fe-FinFET synapses is attributed to the low voltage drop across them during the conversion operation. Moreover, similar to the ADC speed, there is a steep increase in the power consumption of the synapses (11.9 pW to 153 pW) as the output-bit precision increases from 5-bit to 6-bit. As explained in section IV-B, majority of Fe-FinFET synapses are tuned to the low resistance-state for output-bit precision of 6-bits leading to a higher power consumption.

The energy consumed (per input sample) by the proposed ADC exhibits a non-monotonic behavior with the output-bit precision as shown in Fig. 6(c). While the power consumed by the neuron circuit which dominates the energy landscape of the proposed ADC increases linearly with the output-bit precision, the speed of the ADC also increases leading to a reduced conversion time per sample with increasing output-bit precision. The simultaneous increase in the power consumption and reduction in the conversion time results in a non-monotonic behavior of the energy consumed by the proposed ADC. Compared to the state-of-the-art ADCs from the survey [30], the proposed 6-bit Fe-FinFET based LTNN ADC has a similar energy consumption per sample as [32], but outperforms it in terms of both area and speed: 2 mm^2 and 100 kilosamples/s for [32] versus 1.34 μm^2 and 4.67 megasamples/s for the proposed 6-bit ADC.

V. Conclusion

In this work, we have designed an ultra-compact and highly scalable low-to-medium precision neural network based ADC with Fe-FinFETs as synaptic elements. Our extensive analysis indicates that the proposed ADC consumes 5.44 μW of power and 1.03 μm^2 of area while operating at a speed of 1.23 megasamples per second for a 4-bit precision and could be a lucrative alternative to the conventional ADCs specifically for neuromorphic processing engines and neuro-optimization circuits based on cross-point array of emerging non-volatile memories.

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