A VCII Based Tunable Positive and Negative Impedance Simulator and Impedance Multiplier (2022)

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Abstract

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***Abstract*— This paper presents a novel CMOS tunable positive and negative active inductor simulator (AIs), positive capacitance and resistance multiplier and negative capacitance and resistance simulator. The proposed design use only one second-generation voltage-mode conveyor (VCII) and three passive elements. Applications to the proposed design in the design of different types of tunable filters are also presented. The functionality of the designs is confirmed using Tanner Tspice in 0.18µm TSMC CMOS technology.**

***Index Terms*—Active inductor, Impedance multiplier, Integrated circuits, Negative impedance simulator, Filters, Compensation.**

I. INTRODUCTION

Impedance simulators and multipliers are widely used in integrated circuits design where large values passive components are not visible for integration [1-10]. Inductors are essentials in many analog and mixed signal circuits such as filters, oscillators and phase shifters. Simulated inductor and impedance multiplier are more preferable. There are many designs in the open literature and the widely used active blocks are the current conveyor and its modified versions. The design in [1] uses two optical amplifiers and one buffer. The design in [2] consists of a pair of differential voltage current conveyor (DVCC) and three grounded passive elements. In [3], current follower (CF) and a second-generation current conveyor (CCII) are used to simulate grounded inductor. The design in [4-5] used commercially available device and floating capacitor to simulate active inductor. The design in [5] used floating capacitor and commercially available ICs. In [6] a Z-copy current follower current controlled conveyor (CFCCC) and one grounded capacitor are used to realize positive active inductor. The internal structure of this design is complex. The design in [7] used floating capacitor and commercially available IC. In reference [8], one VCII+ and one VCII- in addition to three passive component are used to realize AI. The design in [9] used two negative impedance converter and three passive elements. The design in [10] used one modified VCII± to realize a positive active inductor. The drawback of this design are the restriction on the equality of resistors used and two passive elements are floating.

Recently, a new voltage-Mode active building block called second-generation voltage conveyor is used in the implementation of high-performance grounded immittance-function simulators. This new block is the dual circuit of the more famous second-generation current conveyor (CCII). The difference between CCII and VCII is that, unlike VCII, CCII lacks a low-impedance voltage output port. This feature enables VCII-based circuits to benefit from advantages of processing signals in the current domain while producing output signals in voltage form.

In this paper, a single VCII and three passive elements are used to develop a novel design to realize positive and negative active inductor, negative capacitance and resistance simulator ,and capacitance and resistance multiplier. The rest of the paper s organized as follows: the proposed design is presented in section II. The simulation results and discussions are presented in section III. The paper conclusion is presented in section VI.

II. PROPOSED DESIGN

A modified version of the voltage-mode conveyor is shown in Fig 1 [11]. The relationship between voltage and currents terminals of the VCII- are represented as:

$$\begin{bmatrix} i_{y1} \\ i_x \\ v_y \\ v_z \end{bmatrix} = \begin{bmatrix} -\beta & 0 \\ -\beta & 0 \\ 0 & 0 \\ 0 & \alpha \end{bmatrix} \begin{bmatrix} i_y \\ v_x \end{bmatrix} \quad , \quad i_{zo} = -i_z \tag{1}$$

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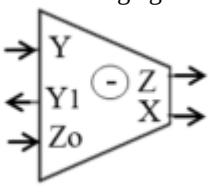
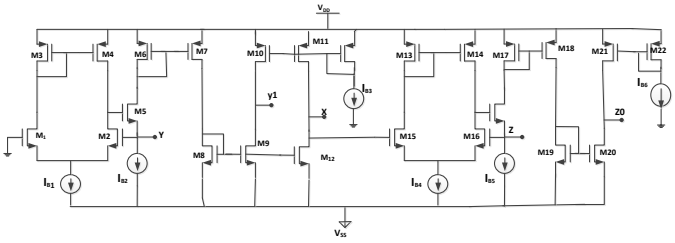
where β and α are current voltage gain respectively.



(a) VCII- Block diagram



(b) Circuit diagram

Fig. 1. Voltage-mode conveyor (VCII-) [11]

The VCII- shown in Fig.2 is powered from ±0.9V DC supply. The aspect ratios for the NMOS and PMOS transistors are respectively chosen as 13.5µm/0.54µm and 40.5µm/0.54µm. The current sources are having the same values (25µA) and designed using simple current mirrors. The terminal characteristic of the VCII- are shown in Table 1.

Table 1. The proposed VCII parameters

R_Y, R_Z	R_X,R_{Y1},Rzo	C_Z	C_x	α	β
47 Ω	245 kΩ	211 fF	15fF	0.96	1.06

The proposed design shown in Figure 2 implements positive active inductor simulator and capacitance and resistance multiplier as follows:

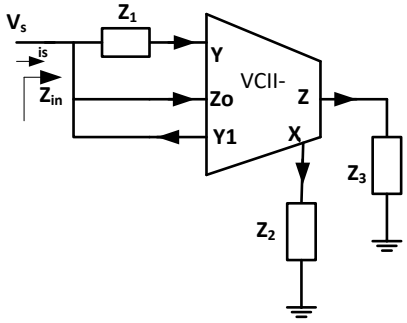


Fig.2. Circuit diagram of the proposed design

with reference to Fig 2, the input impedance is given by:

$$Z_{in} = \frac{V_s}{i_s} = \frac{V_s}{i_y + i_{zo} - i_y} = \frac{V_s}{-i_z} \quad (2)$$

$$i_z = \frac{V_z}{Z_3} = i_x Z_2 / Z_3 = -i_y Z_2 / Z_3 \quad (3)$$

But, $i_y = V_s/Z_1$, then the input impedance is written as:

$$Z_{in} = \frac{Z_1 Z_3}{Z_2} \quad (4)$$

Equation 4 can implements a positive AIs and capacitance and resistance multipliers follows:

1. *Active inductor simulator*

If $Z_1 = R_1, Z_2 = \frac{1}{sC_2}$ *and* $Z_3 = R_3$, the input impedance is given by:

$$Z_{in} = sC_2R_1R_3 = sL \quad (5)$$

where $L = C_2R_1R_2$

Equation (5) implements a tunable active inductor and the value of the inductance is controlled using R_1, R_2 and C_2

2. *Capacitance multiplier*

If $Z_1 = \frac{1}{sC_1}$, $Z_2 = R_2$, and $Z_3 = R_3$ then the input impedance is given by:

$$Z_{in} = \frac{1}{sC_1\frac{R_2}{R_3}} \quad (6)$$

Equation 6 implements a capacitance multiplier in which the original capacitance C_1 is multiplied by $(R_2 \,/\, R_3)$.

3. *Resistance multiplier*

If $Z_1 = R_1$ (the resistance to be scaled up), $Z_2 = R_2$, and $Z_3 = R_3$ then the input impedance is given by:

$$Z_{in} = R_1\frac{R_3}{R_2} \quad (7)$$

From equation 7, $R_1$is the resistance to be scaled using the ratio $\frac{R_3}{R_2}$. To implement a tunable negative impedance simulator, the proposed design in Fig 2 is modified such that $i_{zo} = i_z$ as shown in Fig 3.

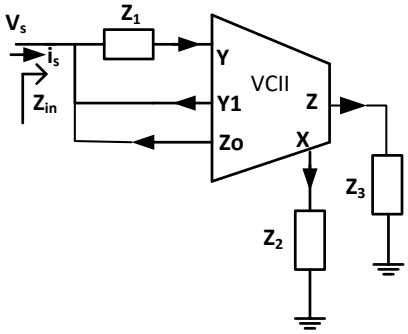


Fig.3. Circuit diagram for negative impedance simulator

with reference to Fig 3, the input impedance Z_{in} is given by:

$$Z_{in} = -\frac{Z_1 Z_3}{Z_2} \quad (8)$$

4. *Negative active inductor simulator*

If $Z_1 = R_1$, $Z_2 = \frac{1}{sC_2}$ and $Z_3 = R_3$, then a negative active inductor is obtained and is given by:

$$Z_{in} = -sC_2R_1R_3 \quad (9)$$

5. *Negative capacitance simulator*

If $Z_1 = \frac{1}{sC_1}$, $Z_2 = R_2$, and $Z_3 = R_3$ then the input impedance is given by:

$$Z_{in} = -\frac{1}{sC_1\frac{R_2}{R_3}} \quad (10)$$

Equation 10 implements a negative and tunable capacitance simulator.

6. *Negative resistance simulator*

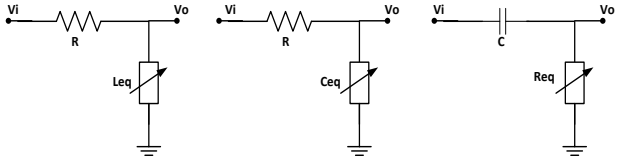
If $Z_1 = R_1$ (the resistance to be scaled up), $Z_2 = R_2$, and $Z_3 = R_3$ then the input impedance is given by:

$$Z_{in=} -R_1 \frac{R_3}{R_2} \quad (11)$$

III. SIMULATION RESULTS

i) Positive impedances

To confirm the functionality of the proposed designs, the active inductor and the capacitor multiplier are used in the design of high pass and low pass filters respectively while the resistance multiplier is used in the design of high pass filter as shown in Fig 4.



(a) HPF (b) LPF c)HPF

Fig. 4. Filters used to confirm the functionality of the proposed design.

a. Active inductor simulator

The proposed AIS is used in the design of high pass filter shown in Fig 4a with R = 1kΩ and the AIS parameters are: R_1 = 0.5kΩ, R_3 is varied from 0.5kΩ to 9.5kΩ and C_2=1nF. Plots of the frequency response of the high pass filter are shown in Fig 5. It is clear from the plots that proposed AIS is working properly and the -3dB frequencies are close to the calculated values with a maximum error 1.6%

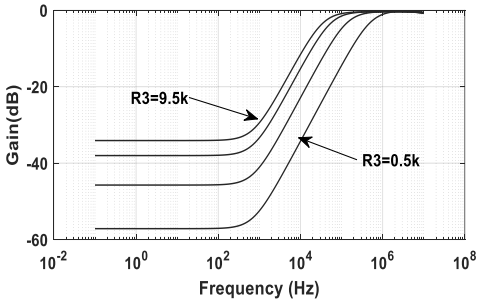


Fig.5. Plots of the frequency response of the high pass filter using AIS

Ideal and simulated inductance frequency reposes are shown in Fig 6 for L=0.5mH. It is clear from the plot that there is small deviation and that it is due to parasitic effects in the low frequency side.

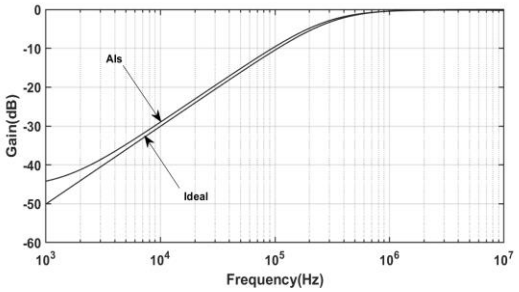


Fig. 6. Plots for high pass filter using AIS and ideal inductor

b. Capacitance Multiplier

The capacitance multiplier is used in the design of the low pass filter shown in Fig 4b with R=10kΩ, C_1=10pF, R_3=10k and R_2 varies from 2kΩ to 10kΩ. Plots of the frequency response are shown in Fig 7. It is clear that the filter is working properly.

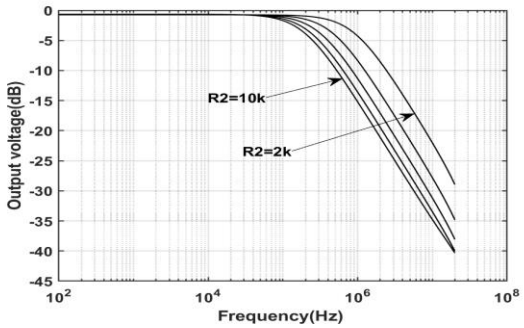


Fig. 7. Plot of the frequency response of the low pass filter using capacitance multiplier

c. Resistance Multiplier

To scale a 100Ω resistance to 50kΩ, use R_1=100Ω (resistance to be scaled), R_2=10Ω and R_3=5kΩ. The resistance multiplier is used in the design of a high pass filter with C=50pF. Plot of the frequency response of the filter is shown in Fig 8.

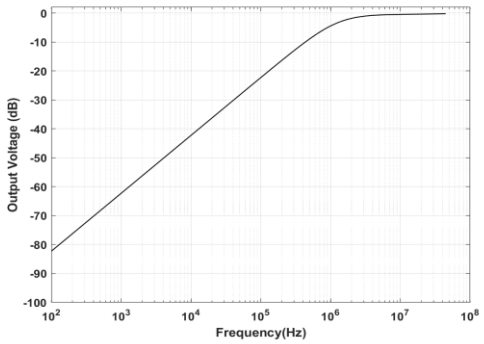


Fig.8. Plot of the frequency response of the high pass filter using resistance multiplier

i) Negative inductance simulator

To confirm the functionality of the negative impedance simulator, the realized components are used in different applications as follows:

a) Negative active inductor

Transient analysis for the circuit shown in Fig 9 is used to confirm the functionality of the negative active inductor. The parameters used are AI=-2.5µH, L=2.5µH and R=1kΩ. Plots of the input signal and the voltage across the inductors, V_x are shown in Fig 10. It is clear from the figure that the negative active inductor canceled the effect of the positive one and the total impedance is zero ad hence act as short circuit forcing V_x to be zero.

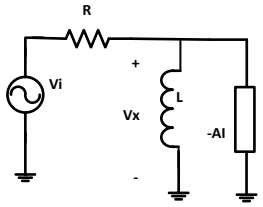


Fig 9. The circuit used to confirm the functionality of the proposed negative active inductance simulator

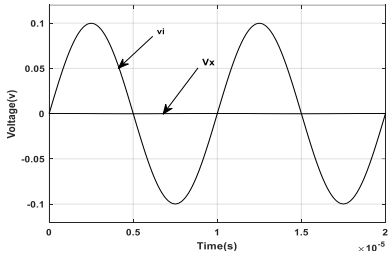


Fig. 10. Plot of the effect of the simulated negative inductance in compensation.

b) Negative capacitance simulator

The circuit shown in Fig. 11 is used to confirm the functionality of the design with simulated capacitance C= -100pF to compensate for100pF and R=100.

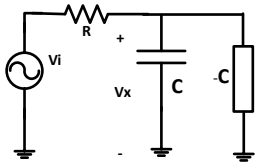


Fig.11. The circuit used to confirm the functionality of the proposed negative capacitance simulator

Plot of the transient response is shown in Fig 12. It is clear from the plot that the output voltage V_x is perfectly following the input, which indicates that the negative capacitance perfectly compensate the effect of the parasitic capacitance

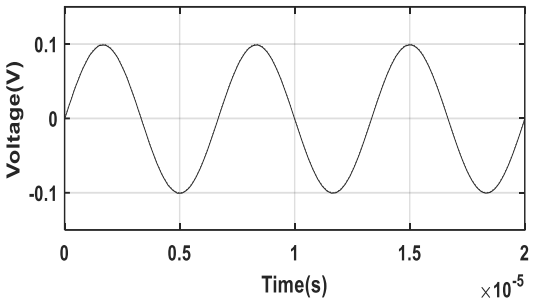


Fig.12. Simulation for compensation using negative capacitance

None ideal analysis

The none-ideal model for VCII is shown in Fig 13 and the parameters values are given in table 1. r. C_x As an example, for the active inductor, it is clear that the effect of C_x and R_x will contribute to the error

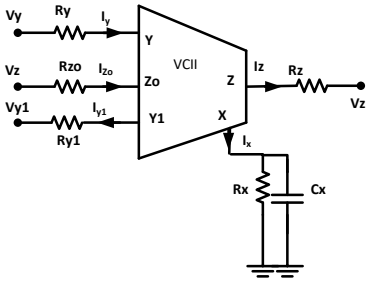


Fig.13. VCII circuit with parasitic included

.The input impedance is given by:

$$Z_{in} = \frac{R_3(R_1+R_y)}{R_x} + \frac{R_3(R_1+R_y)}{R_x} \times sC_2R_x \qquad (12)$$

From 12, if $R_3(R_1 + R_y) \ll R_x$, and if $R_1 \gg R_y$, equation 12 can be written as:

$Z_{in} = sC_2R_3R_1$, which is the same as equation 5

The performance of the proposed design is compared with the recent published works and it was found superior to all in terms of compactness, power consumption, frequency range and novelty.

IV. CONCLUSION

A new VCII based novel, tunable positive and negative impedance simulator and impedance multiplier was developed. The functionality of the designs are confirmed using different applications. The design is compact and will be suitable for many integrated circuit applications in different frequency ranges.

ACKNOWLEDGMENT

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REFERENCES

[1] B. Maundy, S. Gift, "Active Grounded Inductor Circuit,", Int. J. of Electronics, Vol. 98, pp. 555–567, 2011.
[2] A. Hamad, M. Ibrahim , " Grounded Generalized Impedance Converter Based on Differential Voltage Current Conveyor (DVCC) and Its Applications," ZANCO J. Pure Appl. Sci., Vol. 29, pp. 118–127, 2017.
[3] E. Yüce, S. Minaei, " On the Realization of Simulated Inductors with Reduced Parasitic Impedance Effects," Circuits System and Signal Processing, DOI: 10.1007/s00034-008-9093-0
[4] E.Yuce, "Novel Lossless and Lossy Grounded Inductor Simulators Consisting of a Canonical Number of Components,", Analog Integrated Circuits and Signal Processing, Vol. 59, pp. 77-82, 2009.
[5] E. Yuce, S. Minaei, , " Commercially Available Active Device Based Grounded Inductor Simulator and Universal Filter with Improved Low Frequency Performances,". J. Circuits Systems and Computations, doi.org/10.1142/S0218126617500529
[6] A. Singh, P. Kumar, and R. Senani, " Electronically Tunable Grounded/Oating Inductance Simulators Using Z-Copy CFCCC,", Turk. J.Electr. Eng. Comput. Sci., Vol.28, pp.1041-1055, 2018.
[7] S. Siripongdee, W. Jaikla, , " Electronically Controllable Grounded Inductance Simulators Using Single Commercially Available IC LT1228,", AEU—Int. J. Electron. Commun, Vol. 76, pp.1-10, 2017.
[8] L. Safari, E. Yuce, S. Minaei, G. Ferri, G andV. Stornelli, , "A Second-Generation Voltage Conveyor (VCII)–Based Simulated Grounded Inductor,", Int. J. Circuit Theory Appl, Vo. 48, pp.1180-1193, 2020.
[9] E. Yuce, H. Alpaslan, S. Minaei, S, U. Ayten, " A new simulated grounded inductor based on two NICs, two resistors and a grounded capacitor,", Circuits System and Signal Processing, Vol.40, pp. 5847-5863, 2021.
[10] Y.Erkan, S. Leila, S. Minaei , F. Giuseppe , B. Gianluca and S. Vincenzo "A New Simulated Inductor with Reduced Series Resistor Using a Single VCII± ,"Electronics, Vo.10, 2021.
[11] S. Al-Shahrani and M. Al-Absi, "Efficient Inverse Filters based on Second-generation Voltage Conveyors (VCII)," Arab Journal Sci Eng (2021), doi.org/10.1007/s13369-021-05775-5