A Novel Hybrid RF-DC Converter using CMOS n-Well Process

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Abstract

It is well known that CMOS Cross-coupled Differential Drive (CCDD) is the commonly used approach in the design of RF-DC converters. However, multistage designs are usually used to produce higher DC output voltage. This in turn will lead to using the twin-well CMOS process for fabrication since the NMOS source will be at higher potential in the next and consequent stages. The twin-well process technology is expensive compared to the n-well process. On the other hand, the DC output of these designs will saturate when higher voltage is required using multistage. This brief presents a new CMOS n-well process RF-DC converter. The design is hybrid in which the first stage is designed using CCDD since the NMOS source is grounded and the second and consequent stages are designed using only PMOS transistors. The functionality of the proposed design is confirmed using CADENCE in 0.18µm TSMC CMOS technology. Simulation results show that the design is working properly and achieves linear DC output voltage with the number of stages and an input power range of 33dB for PCE >20%.

A Novel Hybrid RF-DC Converter using CMOS n-Well Process

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ABSTRACT It is well known that CMOS Cross-coupled Differential Drive (CCDD) is the commonly used approach in the design of RF-DC converters. However, multistage designs are usually used to produce higher DC output voltage. This in turn will lead to using the twin-well CMOS process for fabrication since the NMOS source will be at higher potential in the next and consequent stages. The twin-well process technology is expensive compared to the n-well process. On the other hand, the DC output of these designs will saturate when higher voltage is required using multistage. This brief presents a new CMOS n-well process RF-DC converter. The design is hybrid in which the first stage is designed using CCDD since the NMOS source is grounded and the second and consequent stages are designed using only PMOS transistors. The functionality of the proposed design is confirmed using CADENCE in 0.18µm TSMC CMOS technology. Simulation results show that the design is working properly and achieves linear DC output voltage with the number of stages and an input power range of 33dB for PCE >20%.

INDEX TERMS Energy harvesting, Efficiency, Dynamic range, Rectifier.

I. INTRODUCTION

CMOS rectifiers are the core block in any RF-DC converter. There are two prominent topologies: Cross- Coupled Differential-Drive (CCDD) and Dickson rectifiers in CMOS technology [1-10]. Most of the designs reported in the literature use the CCDD approach. These designs will be fabricated in a twin well CMOS process whenever multistage cells are required to have a higher DC output voltage. This process is expensive compared to the n-well process.

This work presents a new design in which only an n-well process is used. The first stage will be a normal CCDD (consists of NMOS and PMOS transistors). In this stage the source and the bulk of the NMOS are connected to ground. The consequent stages are designed using PMOS only and connected in a different way. The rest of the paper is organized as follows: The proposed design is presented in section II. Section III reports the simulation results. The paper conclusion is presented in section IV.

II. PROPOSED DESIGN

The proposed RF-DC converter is shown in Figure1. In this design, it is assumed that the RF input is applied to a matching network and then to a balun. The balun acts like a center-tape transformer with two 180° phase shift output as shown in Figure 1.

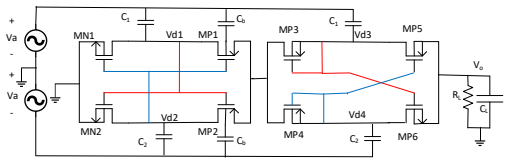

FIGURE 1. The circuit diagram of the proposed hybrid RF-DC converter.

The first stage is formed using the well-known CCDD because the NMOS has lower threshold. The body terminal of the PMOS is connected to either RF+ or RF− signal via coupling capacitors to control the threshold voltage during the ON and the OFF states.

The second and the consequent stages are designed using PMOS only and connected in a different way as shown in Figure 1. Hence an n-well process instead of the twin-well is used to fabricate these types of rectifiers. Consequently, less area and less cost will be the main achievement. In addition, the DC output increases almost linearly with the number of stages and can produce higher output voltage.

The rectifier operation is as follows: the first stage is normal CCDD, and during the negative half of the cycle, transistors MN1 and MP2 will be ON, and hence C_1 will charge to Va-V_{DS1} and the charge in C_2 is pumped to the output. The opposite will happen in the positive half of the cycle. The same will happen for next PMOS stage where C_1 will charge through MP3 and the charge in C_2 will be pumped to the output via MP6

III. SIMULATION RESULTS

The proposed design is implemented in 0.18µm TSMC CMOS process technology and verified using Cadence Virtuoso environment. The aspect ratios of transistors are chosen for CCDD to be MN1=MN2=20µm/.18µm and MP1=MP2=100µm /0.18µm. For the second and consequent stages the size for all transistors is 20µm/0.18µm. The flying capacitors C_1 = C_2 = C_b= 1pF, and C_L = 2pF. The frequency of the signal is 920MHz.

The first two hybrid stage design was simulated for different loads namely (5kΩ, 10kΩ, 50kΩ). Plots of the DC output voltages are shown in figure 2. It is clear from the figure that increasing the load will increase the output voltage. However, it was noted that increasing the load beyond 100kΩ will not make a significant increase in the output voltage.

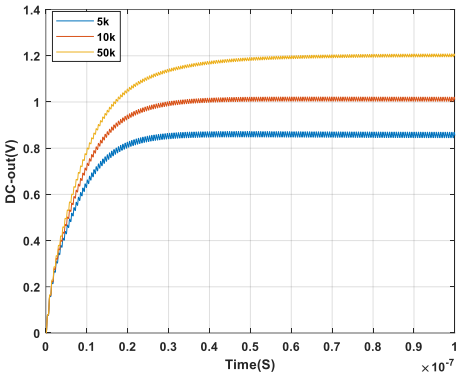

FIGURE 2. Plots of the DC output voltage for different loads.

To achieve a higher DC output voltage, one can cascade the stages without adding any capacitors between stages as shown in figure 3. Plot of the simulated DC output voltage as a function of the number of stages is shown in Figure 4. It is clear from the plot that DC output increases almost linearly with the number of stages. The DC output reaches 8V when cascading 21 stage.

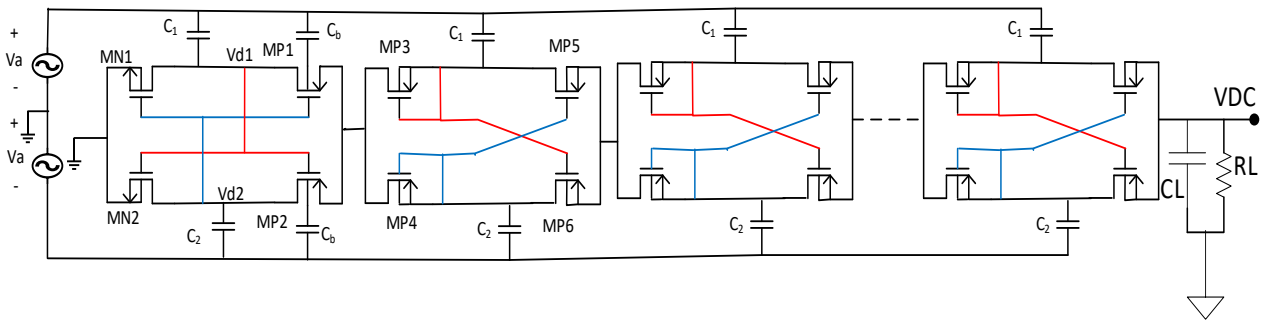

FIGURE 3. Connection for cascading stages

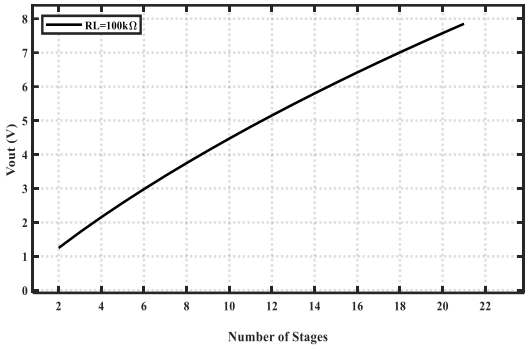

FIGURE 4. **Plot of the output voltage vs the number of stages.**

Plots of the efficiency of the rectifier for different loads are shown in figure 5. It can be seen that the PDR is 33dB.

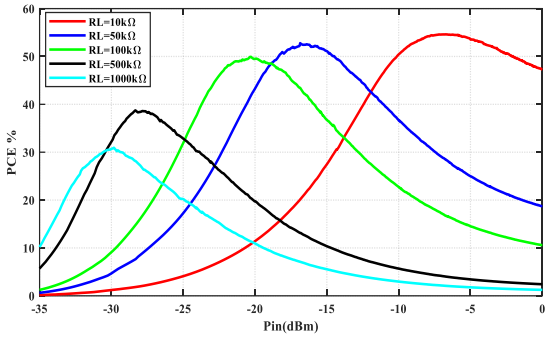

FIGURE 5. **Plots of efficiency vs the input power for different loads.**

IV. CONCLUSION

A new n-well process RF-DC converter is developed. The design uses CCDD as a first stage and the next stages are all designed using PMOS transistors. The proposed design provides a linear DC output voltage with the number of stages and achieves excellent input power range for PCE >20%. We believe that there is a chance to improve the efficiency and make this hybrid design the most efficient in all aspects.

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